APS12627 and APS12628

2D Low Latency Hall-Effect Speed and Direction Sensors

FEATURES AND BENEFITS

- Flexible and easy-to-use sensor for motors/encoders
- ISO 26262 / ASIL B functional safety compliance
- Fault pin provides additional safety by indicating certain fault conditions
- 2D magnetic sensing via planar and vertical Hall elements
  - □ Quadrature independent of magnet pole pitch and air gap—no target optimization required
  - □ Works in almost any orientation to the target (XY, XZ, and ZY options)
- Two signal paths eliminate sampling delay
- Output update rate of 4.0 µs, 10× faster than previous generation—ideal for applications requiring fast response times
- Reduces accumulation of lost counts/pulses
  - □ System can restore correct state after power-cycling (-P option)
- Dual outputs of quadrature or speed/direction signals
- High magnetic sensitivity
- Optimized for applications with regulated power rails
  - □ Operation from 2.8 to 5.5 V

Continued on the next page…

PACKAGE

5-Pin SOT23-W
(Suffix LH)

Not to scale

DESCRIPTION

The APS12627 and APS12628 integrated circuits are dual ultrasensitive Hall-effect latches optimized for use with ring magnets. They feature both vertical and planar Hall elements with sensing axes that are orthogonal to one another, providing 90° of phase separation. This phase separation is inherently independent of magnet pole spacing and air gap. No target optimization is required, making them extremely flexible and easy to use.

For example, the ring magnet pole-pitch can be changed without having to modify the sensor position or other mechanical design details. Additionally, XY, XZ, and ZY options are available to work in almost any orientation to the target. The APS12627 features Speed and Direction outputs, while the APS12628 has quadrature outputs (Channel A/B).

A unique feature allows the host system to restore the correct state after power-cycling the device (-P option). This reduces the potential accumulation of lost counts/pulses when the device wakes up with one or more sensors in its hysteresis region.

Continued on the next page…

TYPICAL APPLICATIONS

- Automotive
  - □ Power closures/actuators
  - □ Electronic power steering
  - □ Seat/window/sunroof motors
  - □ Trunk/door/liftgate motors
- Industrial motors/encoders
- Garage door openers
- Motorized window blinds
- White goods

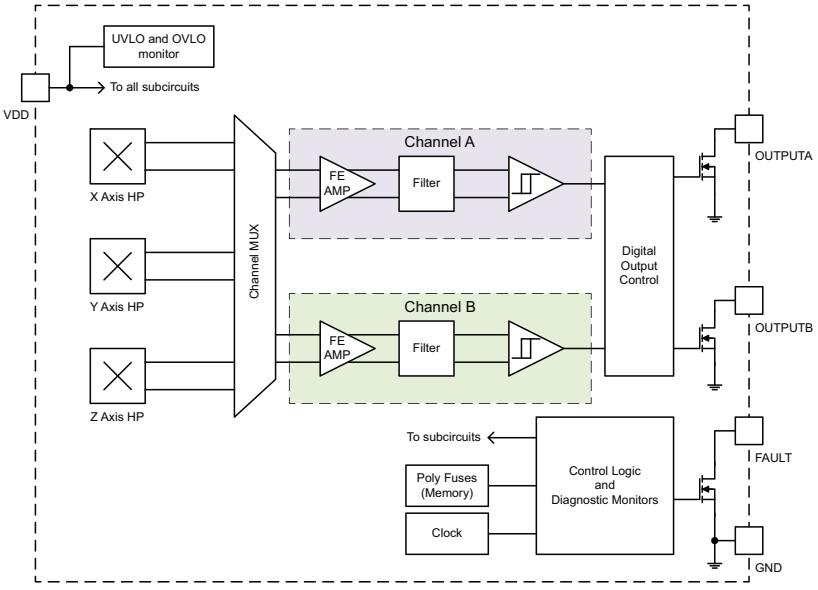


Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Automotive grade/qualified per AEC-Q100
  - □ T_J up to 175°C
  - □ Output short-circuit protection
  - □ Resistant to physical stress
- Small size

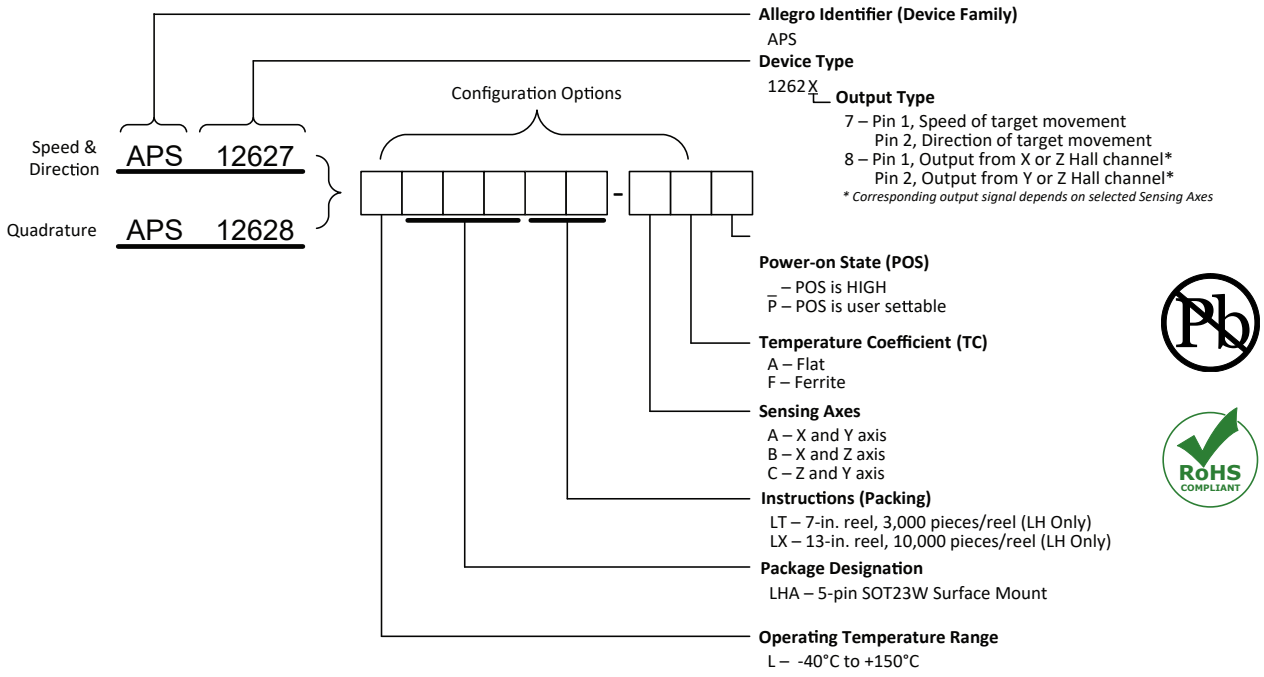
DESCRIPTION (continued)

On a single silicon chip, these devices include: three Hall plates (one planar and two vertical), two small-signal amplifiers, chopper stabilization, a Schmitt trigger, and two NMOS output transistors which can sink up to 10 mA continuously. They operate from a regulated supply voltage of 2.8 to 5.5 V and have been qualified beyond the requirements of AEC-Q100 grade 0 for operation up to 175°C junction temperature.

The small geometries of the BiCMOS process allow these devices to be offered in an ultrasmall package. Package designator "LH" indicates a modified SOT23-W surface-mount package. This package is RoHS compliant and lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

Complete Part Number Format



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SELECTION GUIDE

Part Number [1]	Packaging [2]	Mounting	Output Type	Sensing Axes	Temperature Coefficient (TC)	Power-On State (POS)
APS12627LLHALT-AAP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	A (XY)	A (Flat)	P (User Settable)
APS12627LLHALX-AAP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	A (XY)	A (Flat)	P (User Settable)
APS12627LLHALT-BAP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	B (XZ)	A (Flat)	P (User Settable)
APS12627LLHALX-BAP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	B (XZ)	A (Flat)	P (User Settable)
APS12627LLHALT-CAP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	C (ZY)	A (Flat)	P (User Settable)
APS12627LLHALX-CAP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	7 (Speed & Direction)	C (ZY)	A (Flat)	P (User Settable)
APS12628LLHALT-AAP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	A (XY)	A (Flat)	P (User Settable)
APS12628LLHALX-AAP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	A (XY)	A (Flat)	P (User Settable)
APS12628LLHALT-BAP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	B (XZ)	A (Flat)	P (User Settable)
APS12628LLHALX-BAP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	B (XZ)	A (Flat)	P (User Settable)
APS12628LLHALT-CFP	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	C (ZY)	F (Ferrite)	P (User Settable)
APS12628LLHALX-CFP	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	8 (Quadrature)	C (ZY)	F (Ferrite)	P (User Settable)

[1] Contact Allegro MicroSystems for options not listed in the selection guide.
[2] Contact Allegro MicroSystems for additional packing options.

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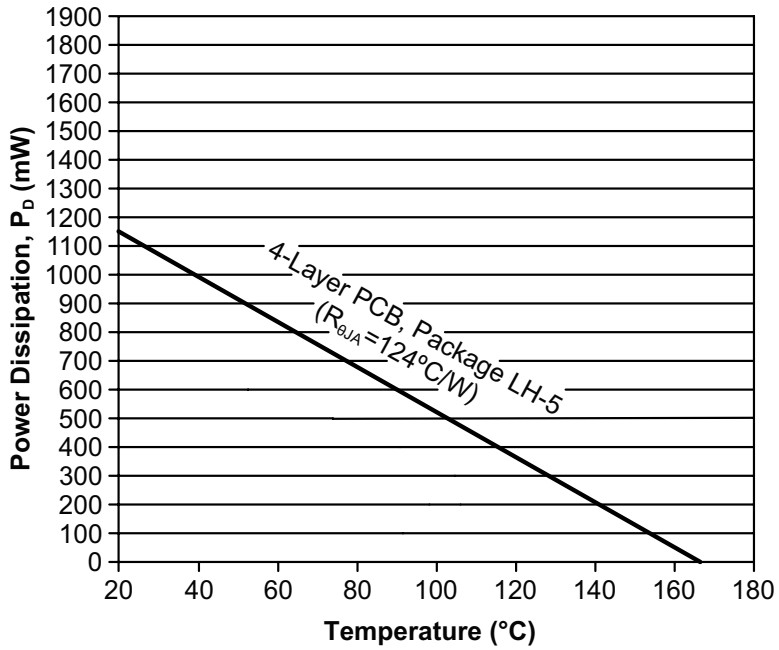
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{DD}		6	V
Reverse Supply Voltage	V_{RDD}		–0.1	V
Magnetic Flux Density	B		Unlimited	G
Output Off Forward Voltage	V_{OUTF}		6	V
Output Off Reverse Voltage	V_{OUTR}	Output Tr is off, gate to ground	–0.1	V
Fault Off Forward Voltage	V_{FAULTF}	Fault Tr is off, gate to ground	20	V
Fault Off Reverse Voltage	V_{FAULTR}	Fault Tr is off, gate to ground	–0.1	V
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
		For 500 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH-5 4-layer board based on the JEDEC standard JESD51-7	124	°C/W

* Additional thermal information available on the Allegro website.



Power Dissipation versus Ambient Temperature

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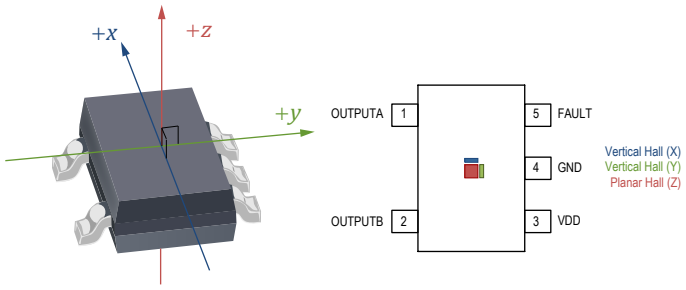
PINOUT DIAGRAMS, TERMINAL LIST, OUTPUT OPTION TABLES, AND APPLICATION CIRCUIT



Package LH, 5-Pin SOT23-W

Terminal List Table

Number	Symbol	Description
1	OUTPUTA	*See output option table*
2	OUTPUTB	*See output option table*
3	VDD	Connects power supply to chip
4	GND	Ground
5	FAULT	Diagnostic Output Signal

Output Option Table

Device	Order Option [1]	Sensing Axes	OUTPUT A (Pin 1)	OUTPUTB (Pin 2)
APS12627	A	XY	XOR speed of target movement	Direction of target movement
	B	XZ		
	C	ZY		
APS12628	A	XY	X channel output	Y channel output
	B	XZ	X channel output	Z channel output
	C	ZY	Z channel output	Y channel output

[1] See Selection Guide.

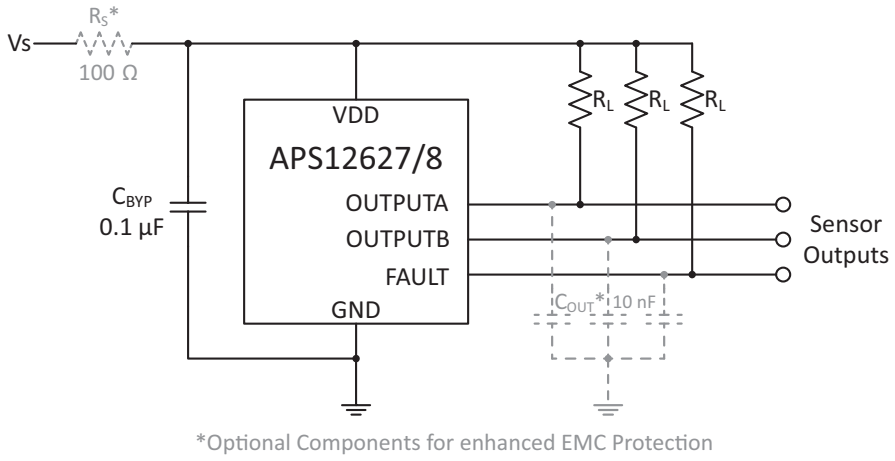


Figure 2: Recommended Application Circuit

For more application information, see the Applications section below.

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature range T_A = –40°C to 150°C, unless otherwise specified [4]

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL SUPPLY CHARACTERISTICS						
Supply Voltage	V_{DD}	Operating, $T_J \le 165°C$	2.8	–	5.5	V
Supply Current	I_{DD}		–	5	8	mA
ELECTRICAL PROTECTION CHARACTERISTICS						
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	$I_{DD} = I_{DD(MAX)} + 1$ mA	6	–	–	V
Reverse Supply Zener Clamp Voltage	$V_{RZSUPPLY}$	I_{DD} = –1 mA	–	–	–0.1	V
Output Zener Clamp Voltage (OUTPUTA, OUTPUTB)	V_{ZOUT}	Voltage applied directly to OUTPUTA or OUTPUTB, I_{OUT} = 0.1 mA	6	–	–	V
Fault Pin Voltage Protection	V_{ZFAULT}	Voltage applied directly to Fault, I_{OUT} = 0.1 mA	20	–	–	V
POWER-ON STATE CHARACTERISTICS						
Power-On Time [2]	t_{ON}	Both outputs	–	50	100	µs
Power-On State External Input	t_{POS_input}	Duration of external POS setting signal, *-P* option only	100	–	–	µs
Power-On State, Output A and B	POS			High		–
OUTPUT CHARACTERISTICS						
Output On Voltage (OUTPUTA, OUTPUTB)	$V_{OUT(SAT)}$	I_{OUT} = 2 mA; output under test in on state, all other outputs in off state	–	180	500	mV
Output Off Voltage (OUTPUTA, OUTPUTB)	$V_{OUT(OFF)}$	OUTPUTA and OUTPUTB are open-drain; application sets output off voltage	–	–	5.5	V
POS External Input Low Level [2]	$V_{IN(LOW)}$	Valid for -P option only	0	–	0.8	V
POS External Input High Level [2]	$V_{IN(HIGH)}$	Valid for -P option only	2.0	–	V_{DD}	V
Fault Output Voltage	$V_{FAULT(LOW)}$	FAULT is present; I_{OUT} = 2 mA, OUTPUTA and OUTPUTB in off state	–	180	500	mV
	$V_{FAULT(HI)}$	FAULT is present; FAULT pin is open-drain; application sets $V_{FAULT(HI)}$ output voltage	–	–	5.5	V
	$V_{FAULT(PULSE)}$	Fault pin pulses between $V_{FAULT(LOW)}$ and $V_{FAULT(HI)}$ when no FAULT is present	$V_{FAULT(LOW)}$	–	$V_{FAULT(HI)}$	V
Fault Output Pulse Frequency [2]	f_{FAULT}	Duty cycle = 50%	5.5	6.5	8.5	kHz
Output Leakage Current (OUTPUTA, OUTPUTB, FAULT)	I_{OUTOFF}	V_{OUT} = 5.5 V	–	–	10	µA
Output Sink Current (OUTPUTA, OUTPUTB, FAULT)	$I_{OUTPUT(SINK)}$	Application sets output sink current	–	–	10	mA
Output Short-Circuit Current Limit (OUTPUTA, OUTPUTB, FAULT)	I_{OM}	V_{DD} = 5.5 V, $T_J \le T_J$(max)	15	–	45	mA
Output Update Rate [2]	t_{update}		–	4	–	µs
Output Rise Time [2][3]	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.2	–	µs
Output Fall Time [2][3]	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.2	–	µs

Continued on next page...

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ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature range T_A = –40°C to 150°C, unless otherwise specified [4]

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Delay Between Direction and Speed Pin Update [2]	$t_{dir\text{-}to\text{-}speed}$	Only valid for APS12627	2.8	4.0	8	µs

[1] Typical data are at T_A = 25°C and V_{DD} = 4 V.
[2] Rise time, fall time, fault pin pulse frequency, POS External Input Low Level, POS External Input High Level, and delay between direction and speed pin update are guaranteed through device characterization.
[3] C_{LOAD} = oscilloscope probe capacitance.
[4] Tested during production at T_A = 25°C. Electrical characteristics verified by design and characterization over full operating voltage and ambient temperature range unless otherwise specified.

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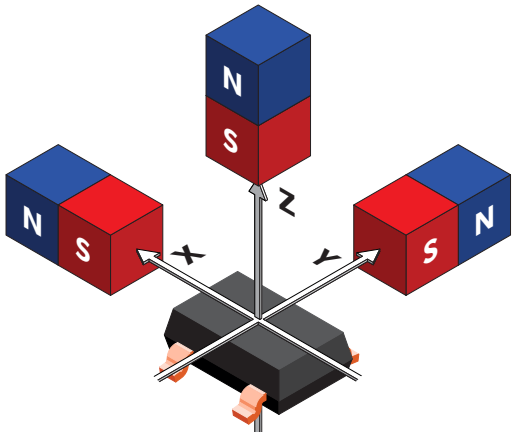
MAGNETIC CHARACTERISTICS: **Valid over full operating voltage and ambient temperature range T_A = –40°C to 150°C, unless otherwise specified [4]**

Characteristics	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit [2]
Operate Point [3] (Channel A, Channel B)	$B_{OP(A)}$, $B_{OP(B)}$	TC = 0	T_A = –40°C	12	27.8	44	G
			T_A = 25°C	11	25.0	41	G
			T_A = 150°C	1	19.7	39	G
		TC = 1		1	21	40	G
Release Point [3] (Channel A, Channel B)	$B_{RP(A)}$, $B_{RP(B)}$	TC = 0	T_A = –40°C	–44	–27.8	–12	G
			T_A = 25°C	–41	–25.0	–11	G
			T_A = 150°C	–39	–19.7	–1	G
		TC = 1		–40	–21	–1	G
Hysteresis [3] (Channel A, Channel B) $B_{OP(A)} – B_{RP(A)}$, $B_{OP(B)} – B_{RP(B)}$	$B_{HYS(A)}$, $B_{HYS(B)}$	TC = 0	T_A = –40°C	38	55.5	72	G
			T_A = 25°C	35	50.0	66	G
			T_A = 150°C	25	39.4	54	G
		TC = 1		25	42	65	G
Symmetry (Channel A, Channel B) $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	$B_{SYM(A)}$, $B_{SYM(B)}$			–35	–	35	G
Operate Symmetry: $B_{OP(A)} – B_{OP(B)}$	$B_{SYM(AB,OP)}$			–15	–	15	G
Release Symmetry: $B_{RP(A)} – B_{RP(B)}$	$B_{SYM(AB,RP)}$			–15	–	15	G
Temperature Coefficient	TC	TC = 0, APS12627-F, APS12628-F		–	–0.17	–	%/°C
		TC = 1, APS12627, APS12628		–	0	–	%/°C

[1] Typical data are at T_A = 25°C and V_{DD} = 4 V, and are for initial design estimations only.
[2] 1 G (gauss) = 0.1 mT (millitesla)
[3] Applicable to all directions (X, Y, and Z).
[4] Tested during production at T_A = 25°C. Magnetic characteristics verified by design and characterization over full operating voltage and ambient temperature range unless otherwise specified.

South polarity magnetic fields, in the orientations illustrated (right), are considered positive fields.



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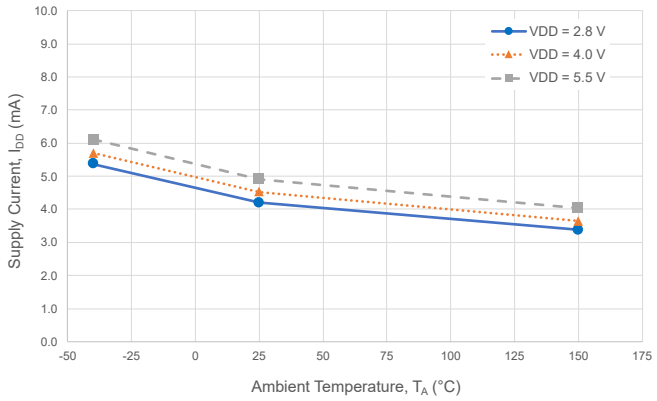
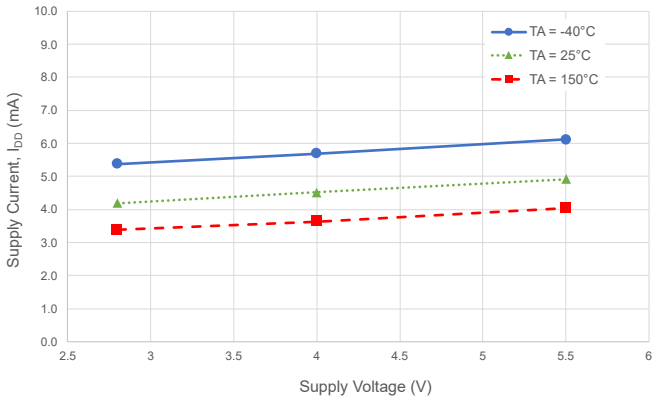
CHARACTERISTIC DATA

Electrical Characteristics

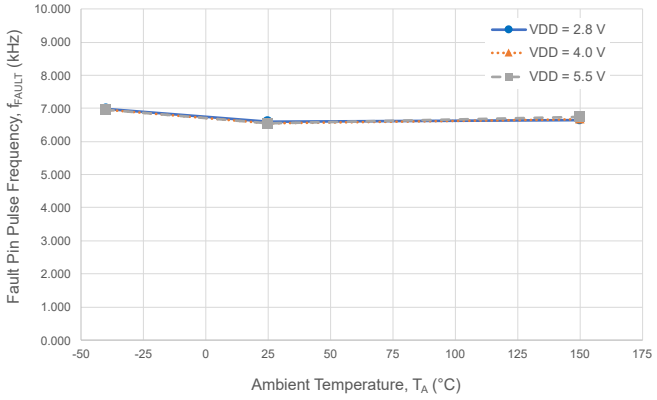
Supply Current vs. Temperature



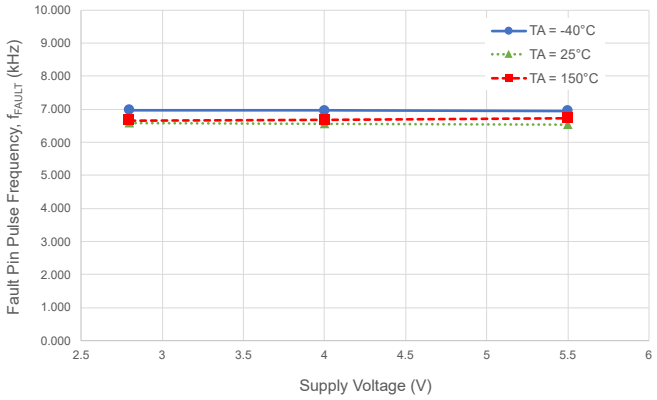
Supply Current vs. Supply Voltage



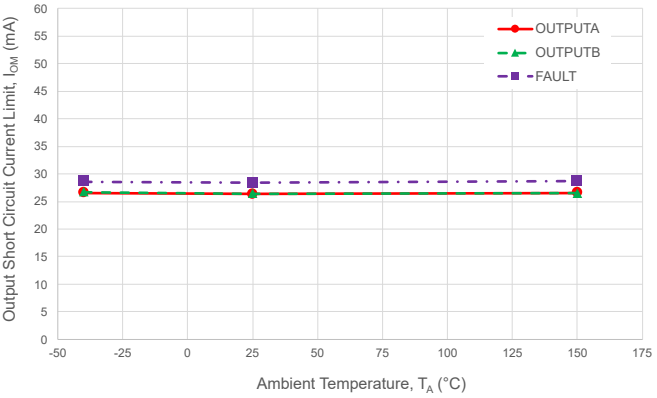
Fault Pin Pulse Frequency vs. Temperature



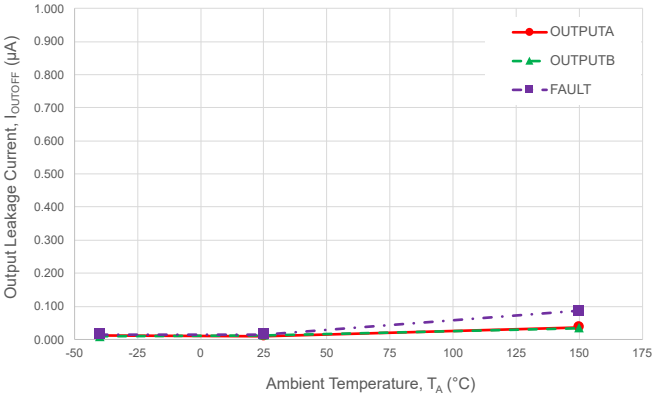
Fault Pin Pulse Frequency vs. Supply Voltage



Output Short Circuit Current Limit vs. Temperature, V_{DD} = 5.5 V



Output Leakage Current vs. Temperature, V_{DD} = 5.5 V



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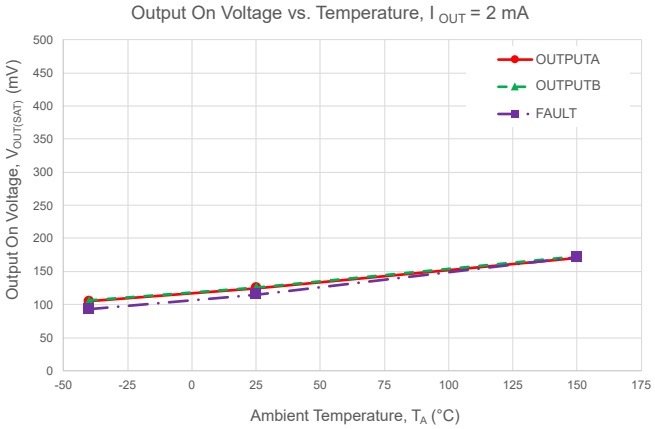
CHARACTERISTIC DATA

Electrical Characteristics (continued)



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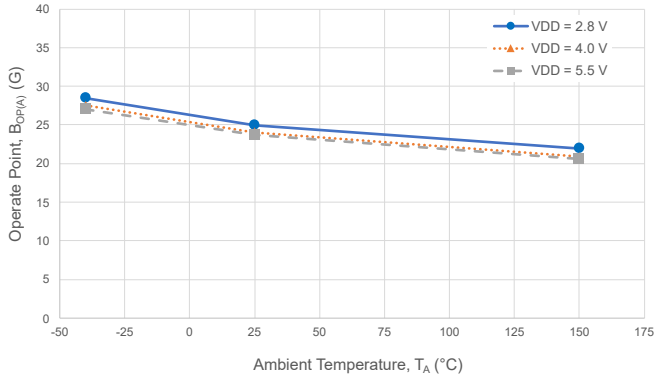
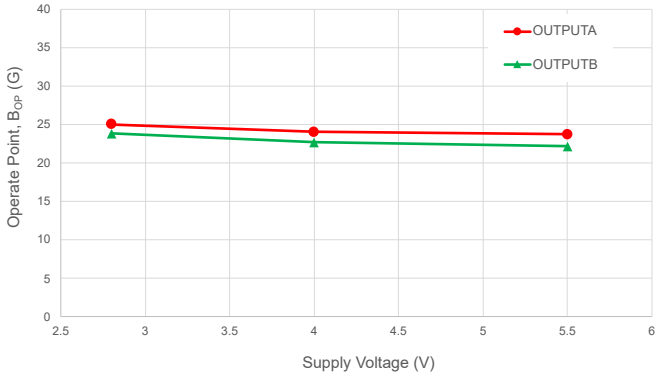
CHARACTERISTIC DATA

Magnetic Characteristics
Option C (ZY) with TC option F (ferrite)

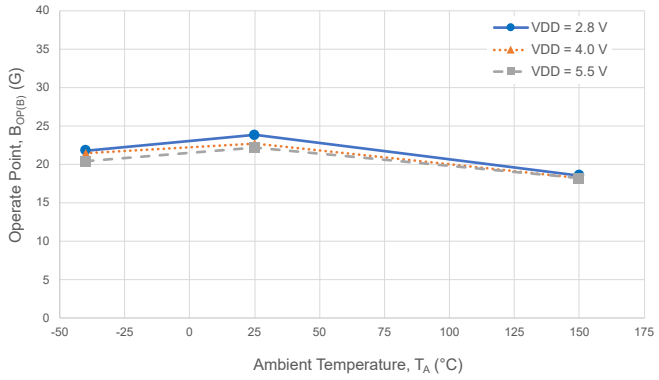
Operate Point (Channel A) vs. Temperature



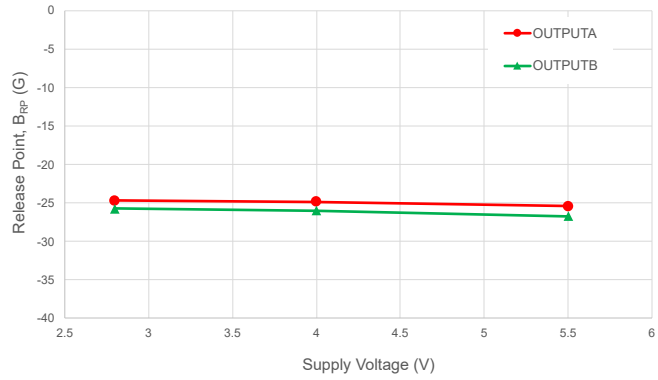
Operate Point vs. Supply Voltage, T_A = 25°C



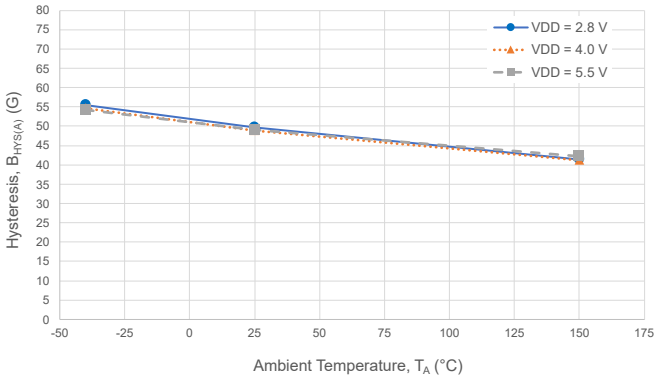
Operate Point (Channel B) vs. Temperature



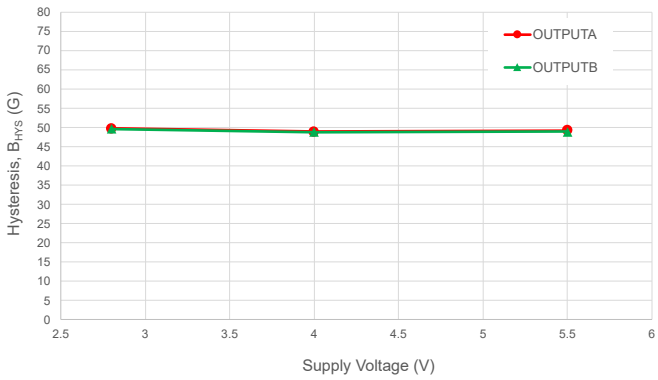
Release Point vs. Supply Voltage, T_A = 25°C



Hysteresis (Channel A) vs. Temperature



Hysteresis vs. Supply Voltage, T_A = 25°C



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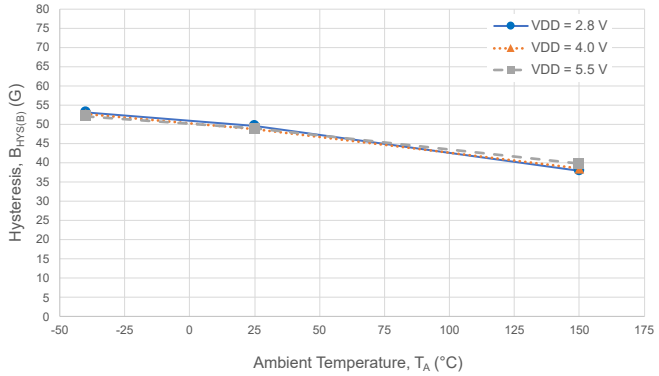
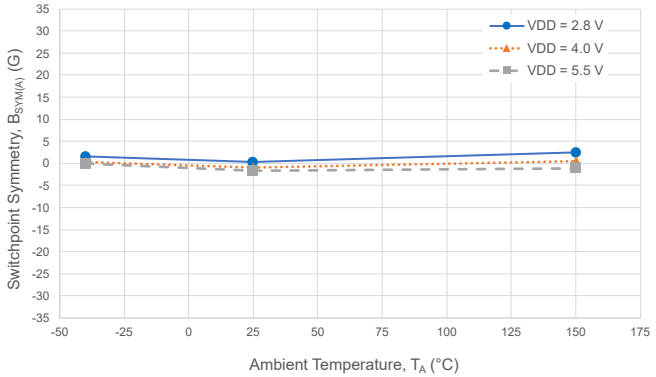
CHARACTERISTIC DATA

Magnetic Characteristics (continued)
Option C (ZY) with TC option F (ferrite) (continued)

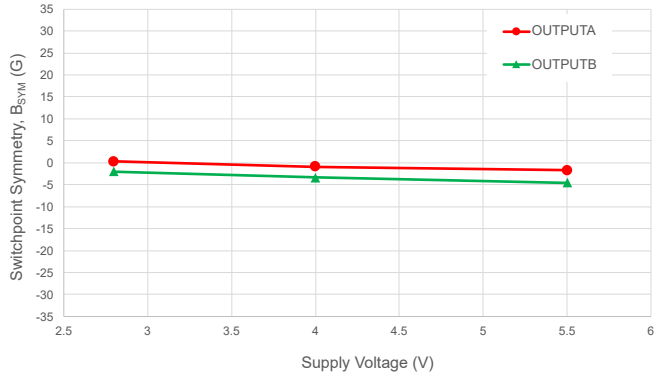
Hysteresis (Channel B) vs. Temperature



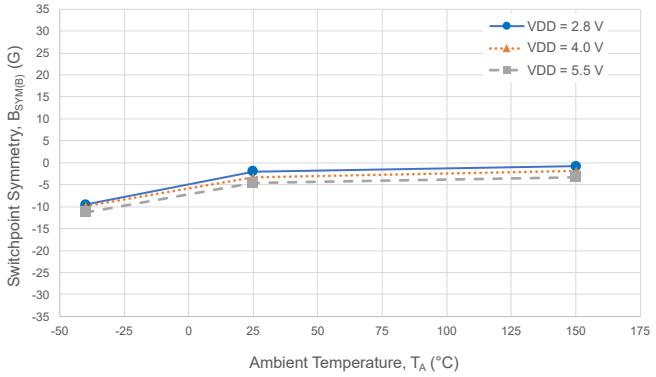
Symmetry (Channel A) vs. Temperature



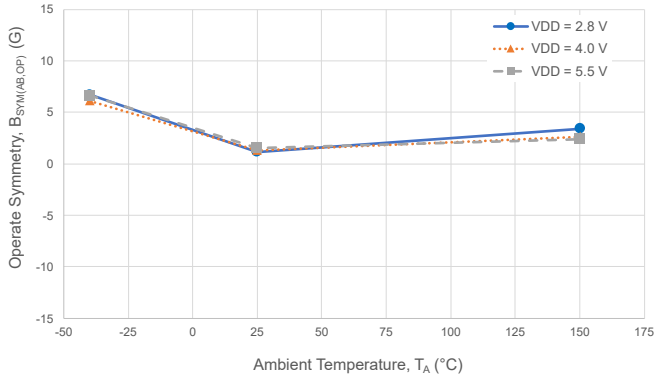
Symmetry vs. Supply Voltage, T_A = 25°C



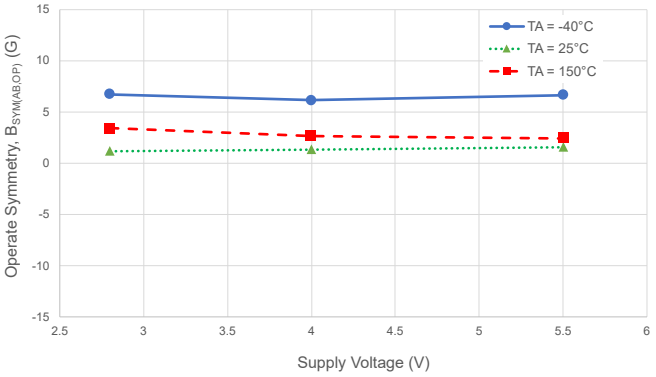
Symmetry (Channel B) vs. Temperature



Operate Symmetry vs. Temperature



Operate Symmetry vs. Supply Voltage, T_A = 25°C



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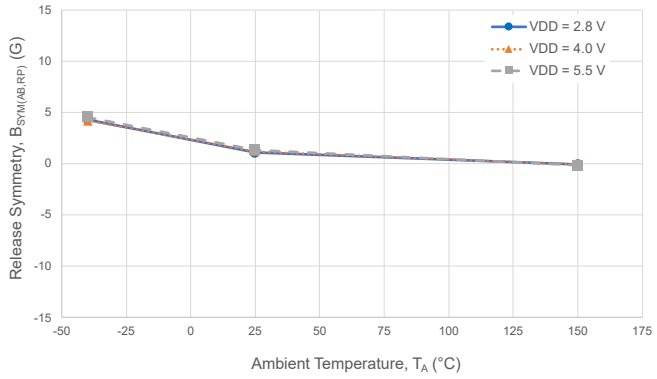
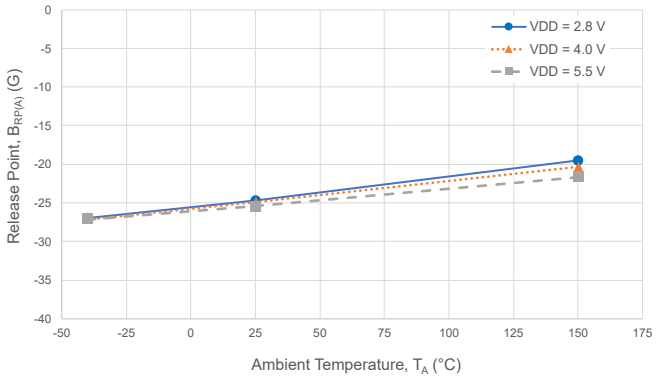
CHARACTERISTIC DATA

Magnetic Characteristics (continued)
Option C (ZY) with TC option F (ferrite) (continued)

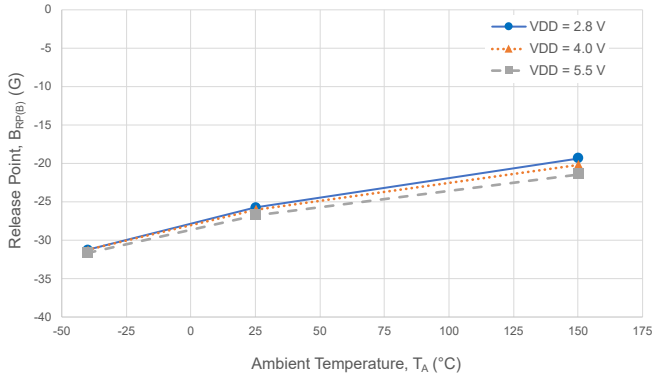
Release Symmetry vs. Temperature



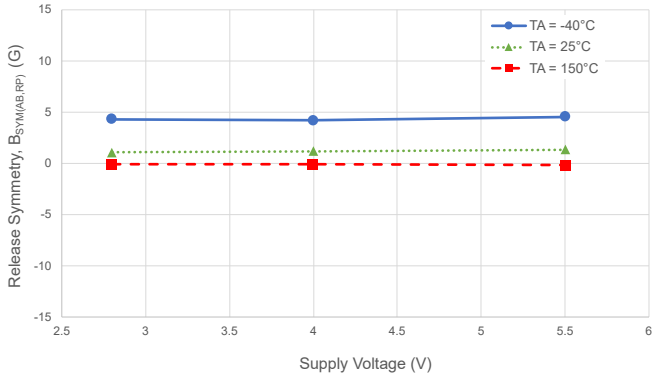
Release Point (Channel A) vs. Temperature



Release Point (Channel B) vs. Temperature



Release Symmetry vs. Supply Voltage, T_A = 25°C



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FUNCTIONAL DESCRIPTION

Quadrature/Direction Detection

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall spacing (distance) in order to have the two channels to be in quadrature, or 90 degrees out of phase. With the APS12627/8, which uses one planar and one vertical Hall-effect sensing element, or two vertical Hall-effect sensing elements perpendicular to one another, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles, therefore the two channels will inherently be in quadrature, irrespective of the ring-magnet pole spacing. The same is true in the dual-vertical Hall configuration, with the vertical Hall element facing the magnet poles sensing the magnet directly and the other vertical Hall element sensing the transitions between poles. The quadrature relationship allows for the direction signal to be appropriately updated.

Outputs

SPEED AND DIRECTION

Internal logic circuitry of the APS12627 provides outputs representing the speed and direction of the magnetic field across the package.

The Speed (SPD) output is the XOR of the output of the two active Hall elements, providing two times the resolution of a single channel, while the direction (DIR) output provides the direction of the target. The direction output, DIR, is always updated before SPD, according to tdir-to-speed. SPD is updated on every transition of either Hall sensor, allowing the use of up-down counters without loss of pulses.

QUADRATURE

The APS12628 offers individual outputs of the two active Hall sensors, referred to here as Channel A and Channel B. The Output Option Table indicates which Hall sensing element corresponds to “Channel A” and “Channel B” in each configuration.

The Channel A and Channel B outputs of the APS12628 switch low (turn on) when the corresponding Hall element is presented with a perpendicular south magnetic field of sufficient strength ($>B_{OP}$). The device outputs switch high (turn off) when the strength of a perpendicular north magnetic field exceeds the release point (B_{RP}). The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. See Figure 3.

Removal of the magnetic field will leave the device output latched on if the last crossed switch point is B_{OP} or latched off if the last crossed switch point is B_{RP}.

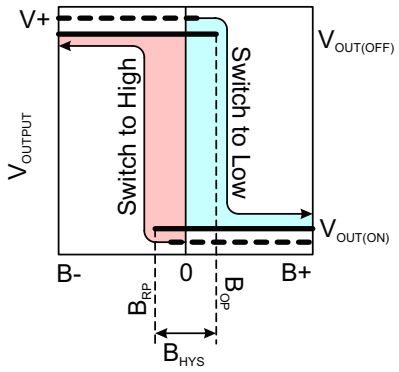

Figure 3: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity)

This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The device will power-on in the high output state even when powering-on in the hysteresis region between B_{OP} and B_{RP}.

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FAULT OUTPUT

Both the APS12627 and APS12628 include a fault detection feature. When the device is operating without a 'FAULT' condition, there will be a pulsed signal on the fault pin as seen in Figure 4. The pulsed-fault signal will have a 50% duty cycle and a frequency of 6.5 kHz.

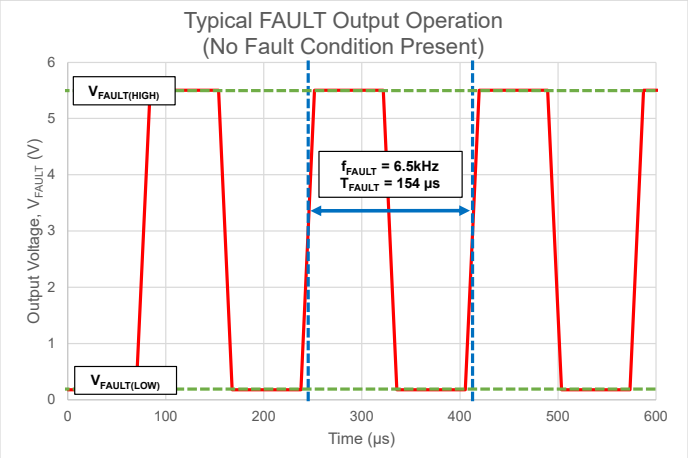

Figure 4: Fault Pin Output – No Fault Present

When a 'FAULT' condition is present, the Fault pin output will be latched 'HIGH' or 'LOW.' Depending on the latched output state, the following faults could be present:

Fault Pin Output – 'HIGH'

- Broken VDD bond wire or pin (see node 1)
- Broken GND bond wire or pin (see node 2)
- Broken Fault bond wire or pin (see node 4)
- Fault shorted to VDD (internally or externally)
- Power Supply UVLO [1]

Fault Pin Output – 'LOW'

- Loss of Power Supply (see node 3)
- Shorted VDD and GND (internally or externally)
- Fault shorted to GND (internally or externally)
- IC-Level Fault Detected
- Digital Faults
  - □ Reset Monitor Fault
  - □ Test Mode Monitor Fault
  - □ Fuse Parity Monitor
- Analog Faults
  - □ Main Oscillator Clock Fault Monitor
  - □ Digital Supply Fault
  - □ Power Supply OVLO [1]

The fault pin will remain latched as long as the 'FAULT' condition is present. When the 'FAULT' condition is removed, the fault pin will return to a pulsed output.

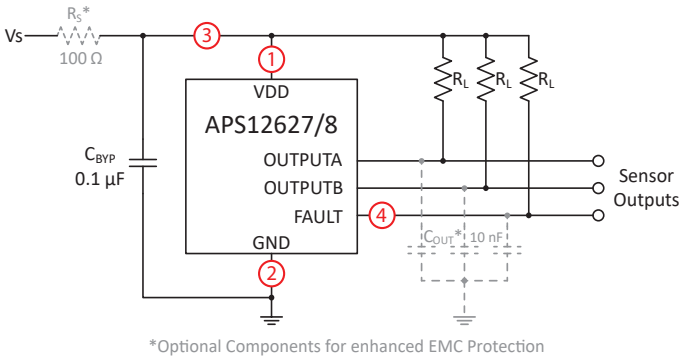

Figure 5: Cut Wires Creating a Fault Condition

[1] Not to be used as safety monitoring mechanism.

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Operation

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall spacing (distance) for the outputs of the two latches to be in quadrature or 90 degrees out of phase. With the APS12627 and APS12628, which uses one planar and one vertical Hall-effect sensing element, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles; therefore, the two channels will inherently be in quadrature, regardless of the ring-magnet pole spacing.

Figure 6 shows a ring magnet optimized for the E1-to-E2 spacing of a dual-planar sensor, resulting in quadrature, or 90 degrees phase separation between channels. This same target also results in quadrature for the 2D sensing APS12627/8. However, when a different ring magnet is used which is not optimized for the E1-to-E2 spacing, the dual-planar sensor exhibits diminished phase separation, making signal processing the outputs into speed and direction less robust. Using a different ring-magnet geometry has no effect on the APS12627/8, and the two channels remain in quadrature (see Figure 7). The relationship of the various signals and the typical system timing is shown in Figure 8.

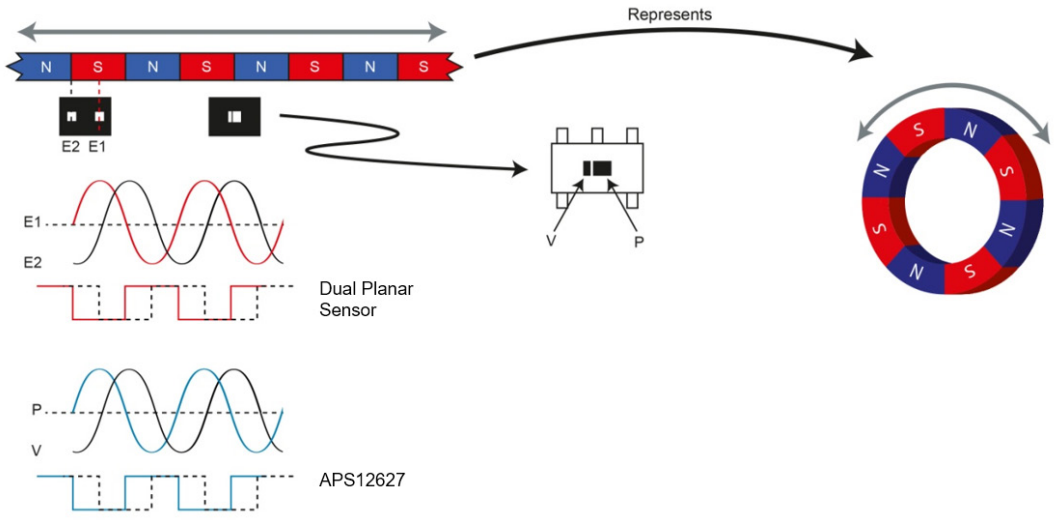

Figure 6: Ring magnet optimized for a dual-planar Hall-effect sensor resulting in output quadrature also results in quadrature for the APS12627/8.

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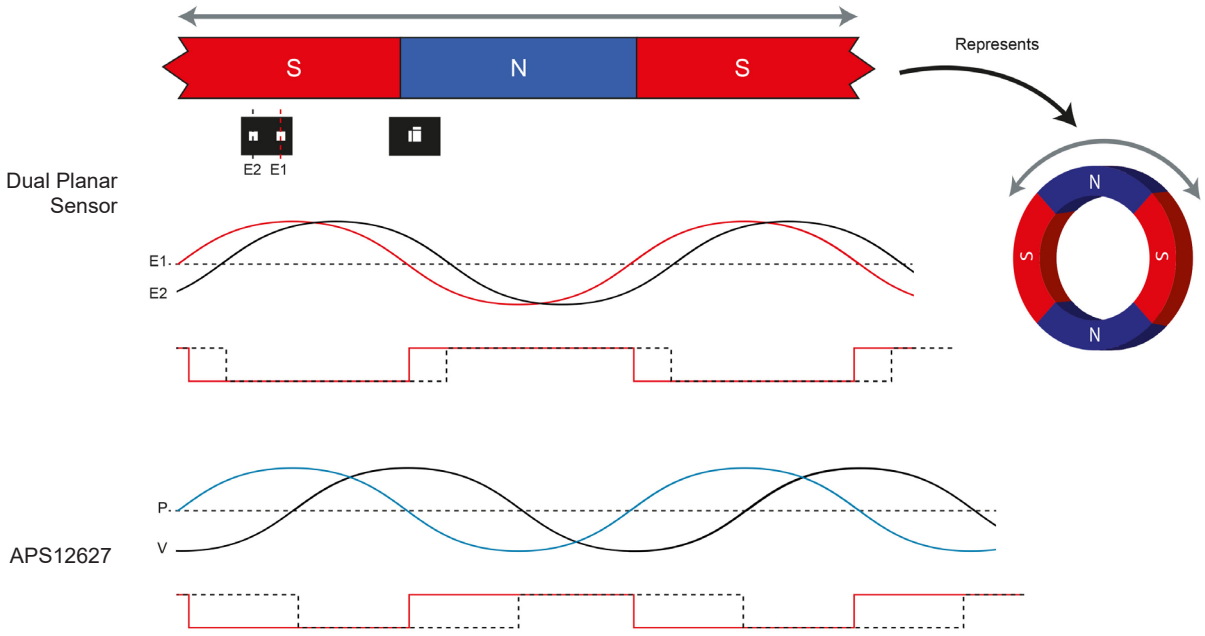

Figure 7: Ring magnet not optimized for a dual-planar Hall-effect sensor resulting in significantly reduced output phase separation, however still results in quadrature for the APS12627/8.

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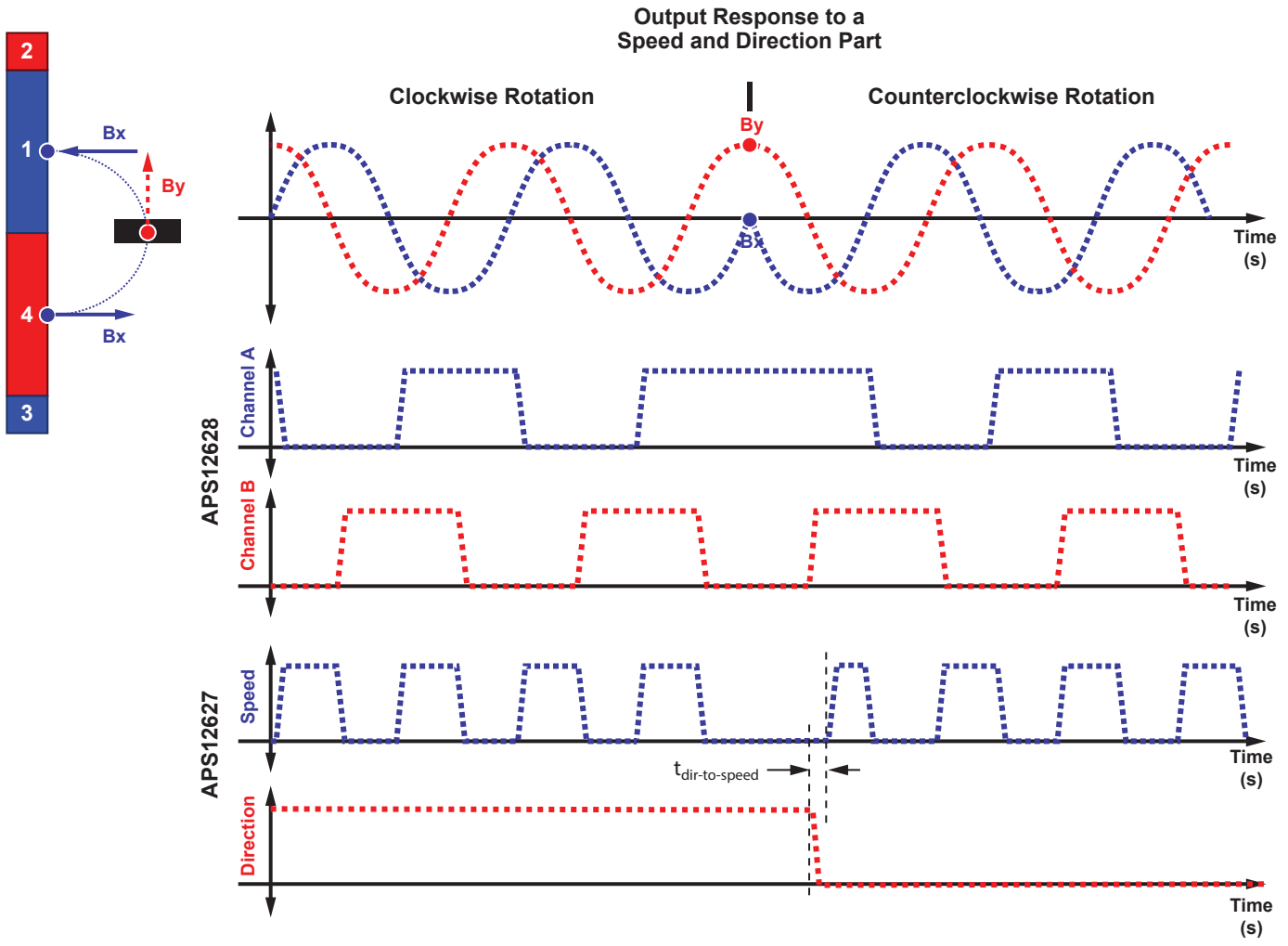

Figure 8: Typical System Timing

The two active Hall signals represent the magnetic input signal, which is converted to the device outputs, OUTPUTA and OUTPUTB, respectively for the Quadrature Output configuration. If the Speed and Direction option is selected, the outputs will reflect direction and speed. The Direction output will update before Speed output by $t_{dir\text{-}to\text{-}speed}$. Only one case is shown above; however, the Direction output will indicate a direction change after any one channel has two consecutive output transitions without the other channel having any output transitions.

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APS12627/8 Sensor and Relationship to Target

The APS12627/8 devices are available in three different sensing configurations, with X-axis vertical Hall and Y-axis vertical Hall active, with Z-axis planar Hall and the X-axis vertical Hall active, or with the Z-axis planar Hall and the Y-axis vertical Hall active. This offers incredible flexibility for positioning the IC within various applications.

Axes option A (X-Y) supports having the IC positioned with the face of the package in-plane with the ring magnet from either the leadless (Figure 9a) or leaded (Figure 9b) sides of the package.

Axes option B (X-Z) supports having the IC positioned with the face of the package facing the ring magnet, and the axis of rotation (Figure 10a) lengthwise along the package body, or with either of the non-leaded sides of the package facing the ring magnet (Figure 10b).

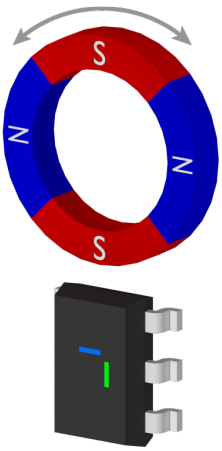

Figure 9a

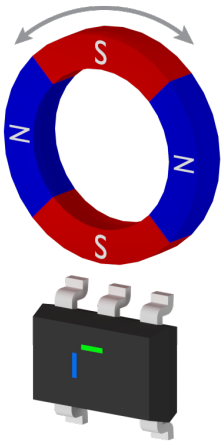

Figure 9b

Axes option C (Z-Y) supports the traditional configuration with the face of the package facing the ring magnet (Figure 11a), with the axis of rotation going across the leads, or with either of the leaded sides of the package facing the ring magnet (Figure 11b).

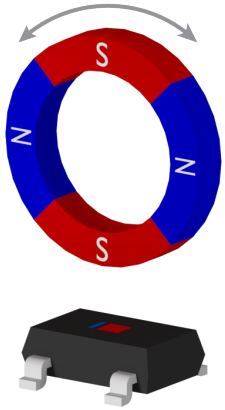

Figure 10a

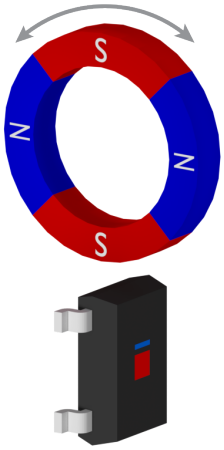

Figure 10b

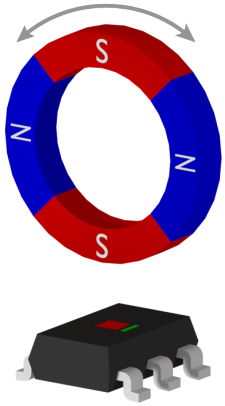

Figure 11a

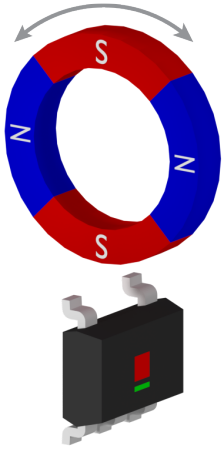

Figure 11b

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Table 1 : APS12627 Sensor and Relationship to Target

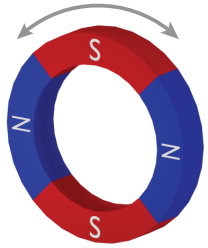
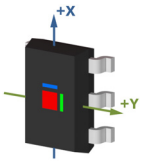
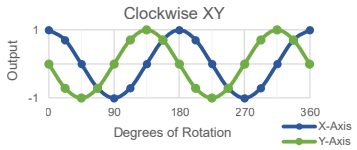
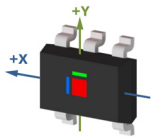
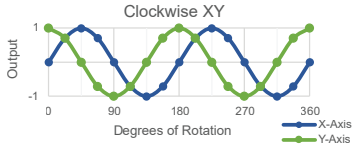
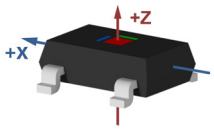
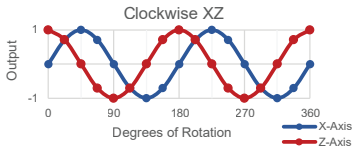
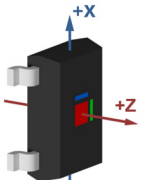
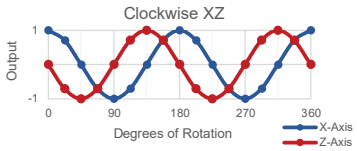
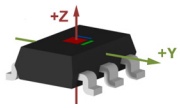
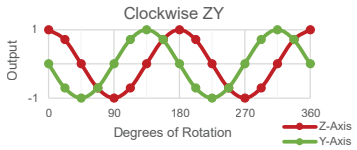
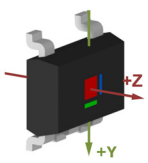
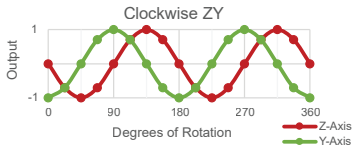
	IC and Relationship to Target	Active Axis Over 360 Clockwise Rotation	State of Direction Output	
Target			**Clockwise**	**Counterclockwise (anticlockwise)**
XY			High	Low
			High	Low
XZ			High	Low
			High	Low
ZY			High	Low
			High	Low

Table 1 above indicates the direction output polarity for the different orientations relative to the rotation of the ring magnet.

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Power-On Sequence and Timing

NON-*P* OPTION

The default power-on state has been achieved when the supply voltage is within the specified operating range ($V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 12: Power-On Sequence and Timing for an illustration of the power-on sequence.

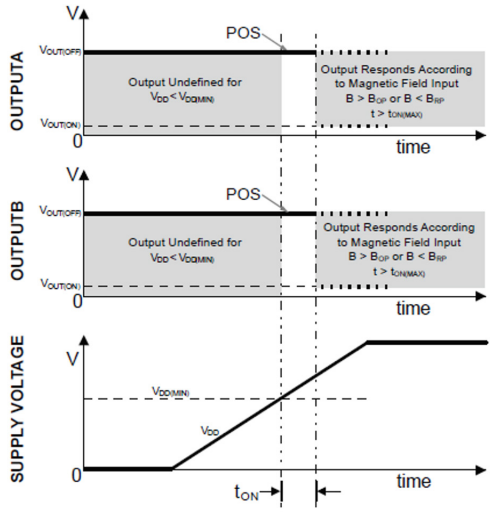

Figure 12: Power-On Sequence and Timing

Once the supply voltage is within the operational range, the outputs will be in the high state (power-on state), regardless of the magnetic field. The outputs will remain high until the sensor is fully powered on ($t > t_{ON}$)—note that the vertical Hall channel typically responds before the planar Hall channel.

-*P* OPTION

For the –*P* option device (user/externally set power-on state), the power-on sequence is similar to the default with the exception that if either of the outputs have input field in the hysteresis band, the output state can be externally set low with a low setting pulse.

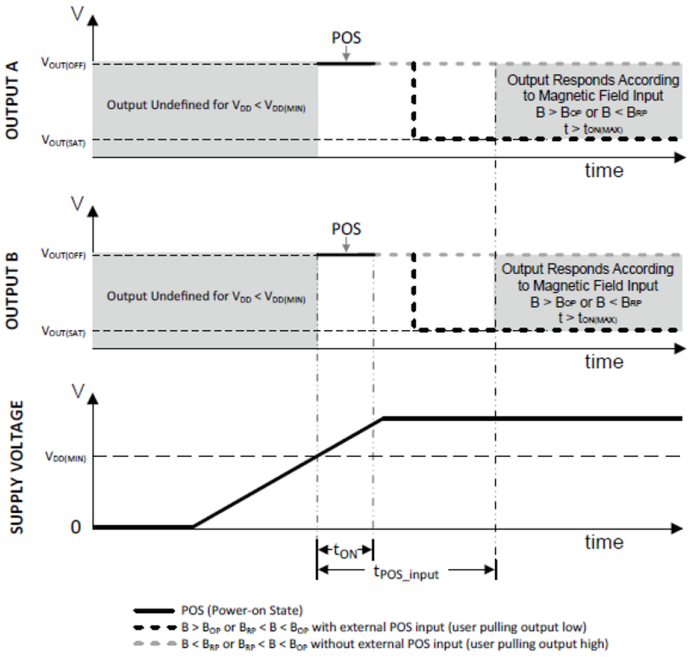

Figure 13: Power-On Sequence and Timing, -P option

If the desired power-on state is high, the user should *not* input a power-on state pulse. The outputs will default to the high state until the device is fully powered on (if $B > B_{OP}$, the respective output will switch low after t_{ON}).

If the desired power-on state is low, the user should input a low output state setting pulse for t_{POS_input}. The output will switch low after t_{ON} if the field level is within the hysteresis band ($B_{RP} < B < B_{OP}$).

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Setting the Power-On State (-P option only)

The power-on state can be set by the host so that when the sensor is being power-cycled for power savings, the outputs can be restored to the desired state. The start-up flow for quadrature outputs is shown in Figure 14, and the flow for speed and direction outputs is shown in Figure 15.

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When the sensor powers on, each channel assumes an output state based on the input magnetic field present at the time, unless the field level is within the hysteresis band. In that case (field within hysteresis band), the output can be forced low externally during the time where no conclusive field is seen by the sensor.

The forcing signal needs to be provided for more than 100 µs, the minimum Power-On State External Input time (t_{POS_input}). The state of each channel will be copied by the sensor.

This allows setting a wake-up state that is consistent with the shutdown state, thus avoiding errors in the total pulse count. If the target starts moving before $t > t_{POS\_input}$, the desired wake-up state may not be correctly set. The sensor will exit POS mode once either of the output channels has an output transition (i.e. sufficient target movement).

Channels A and B are set independently of one another.

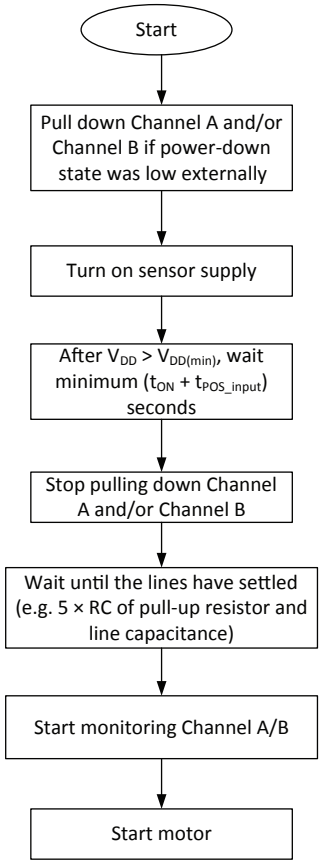

Figure 14: Output setting at power-on, dual quadrature outputs

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APS12627

For the Speed and Direction option (APS12627), when the sensor powers-on, the Speed output is set as A XOR B, and Direction is in the high state until a transition on internal channels A or B has been seen.

If one of the channels wakes up with the magnetic input field in the hysteresis band, then it is possible to set the speed pin value to be consistent with the state at shutdown. A default value of high will be assumed by the sensor, unless a low state-setting pulse is seen during t_{POS_input}. If the target starts moving before $t > t_{POS\_input}$, the desired wake-up state may not be correctly set. The forcing signal needs to be provided for more than 100 µs, the minimum Power-On State External Input time (t_{POS_input}). The sensor will exit POS mode once either of the output channels has an output transition (i.e. sufficient target movement).

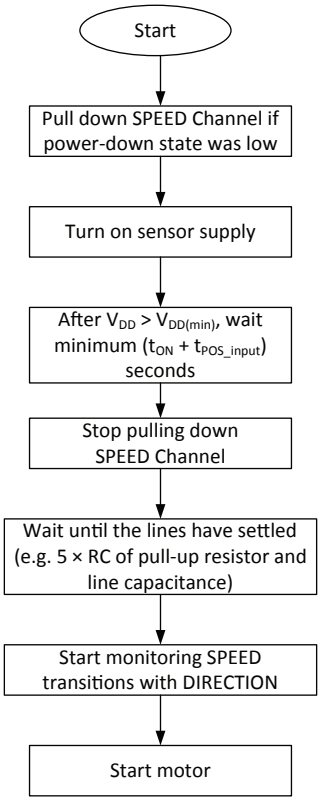

Figure 15: Output setting at power-on, Speed and Direction

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Functional Safety

The APS12627/8 was designed in accordance with the international standard for automotive functional safety, ISO 26262. This product achieves an ASIL (Automotive Safety Integrity Level) rating of ASIL B according to the standard. The APS12627/8 is classified as a SEOoC (Safety Element Out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. Contact your local FAE for A²-SIL™ documentation: www.allegromicro.com/ASIL.

The APS12627/8 has internal diagnostics to check the voltage supply (an undervoltage lockout regulator) and to detect overtemperature conditions. See the Diagnostics section for more information (pending).

Applications

An external bypass capacitor must be connected (in close proximity to the Hall sensor) between the supply and ground of the device to guarantee correct performance and to reduce noise from internal circuitry. As shown in Figure 16, a 0.1 µF capacitor is typical. If the application requires additional EMC protection, additional components are suggested in gray in the same figure.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices, AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*
- *Air-Gap-Independent Speed and Direction Sensing Using the Allegro A1262, AN296124*
- *Improved Speed and Direction Sensing Using Vertical Hall Technology, AN296130*

All are provided on the Allegro website:

www.allegromicro.com

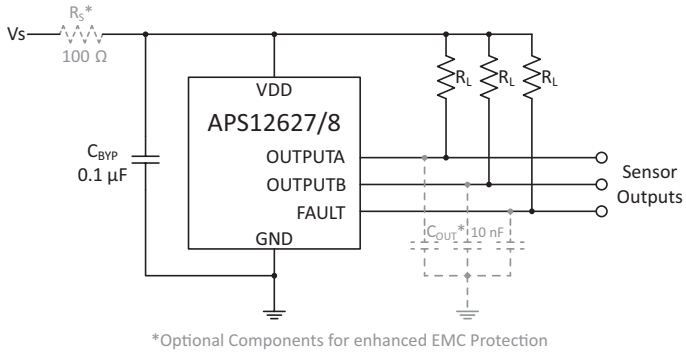

Figure 16: Typical Application Circuit

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a proven approach used to minimize Hall offset on the chip.

The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetic-field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic signal then can pass through a low-pass filter, while the modulated DC offset is suppressed.

The chopper stabilization technique uses a high frequency clock, generally at hundreds of kilohertz. A sample-and-hold technique is used for demodulation, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

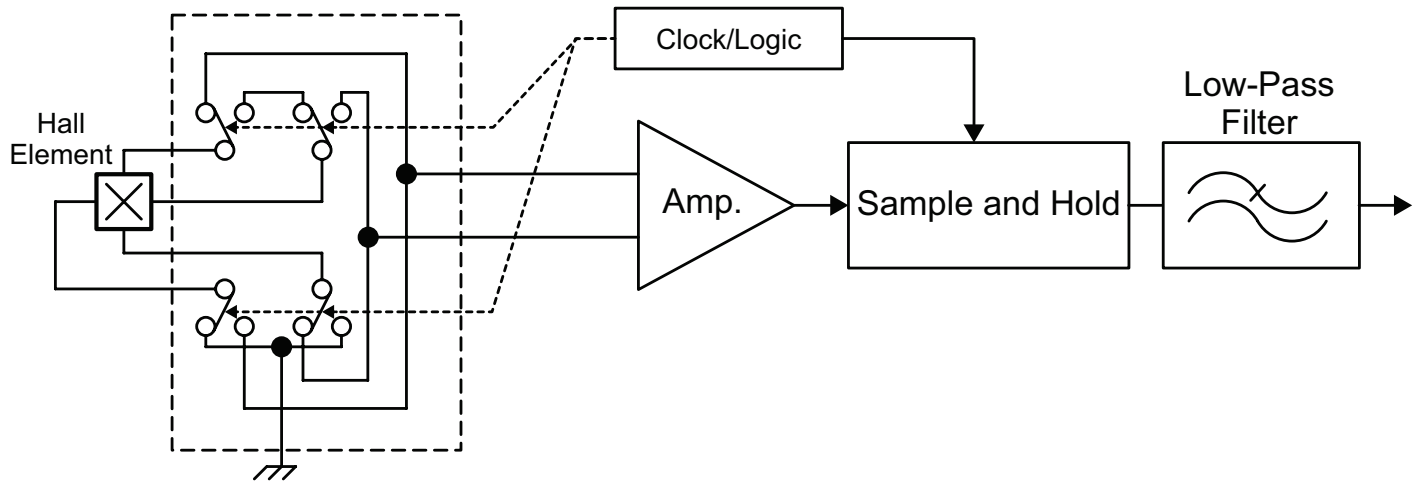

Figure 17: Model of Chopper Stabilization Technique

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A = 25°C, V_{DD} = 5 V, I_{DD} = 5 mA, and $R_{\theta JA}$ = 124°C/W for the LH-5 package, then:

$$P_D = V_{DD} \times I_{DD} = 5\ V \times 5\ mA = 25\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 25\ mW \times 124°C/W = 3.1°C$$

$$T_J = T_A + \Delta T = 25°C + 3.1°C = 28.1°C$$

A worst-case estimate ($P_{D(max)}$) represents the maximum allowable power level ($V_{DD(max)}$, $I_{DD(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{DD} at T_A = 150°C, package LH-5, using low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 124°C/W, $T_{J(max)}$ = 165°C, $V_{DD(max)}$ = 5.5 V, and $I_{DD(max)}$ = 8 mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 124°C/W = 121\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{DD(est)} = P_{D(max)} \div I_{DD(max)}$$

$$V_{DD(est)} = 121\ mW \div 8\ mA$$

$$V_{DD(est)} = 15.1\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{DD(est)}$.

Compare $V_{DD(est)}$ to $V_{DD(max)}$. If $V_{DD(est)} \leq V_{DD(max)}$, then reliable operation between $V_{DD(est)}$ and $V_{DD(max)}$ requires enhanced $R_{\theta JA}$. If $V_{DD(est)} \geq V_{DD(max)}$, then operation between $V_{DD(est)}$ and $V_{DD(max)}$ is reliable under these conditions.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000628, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

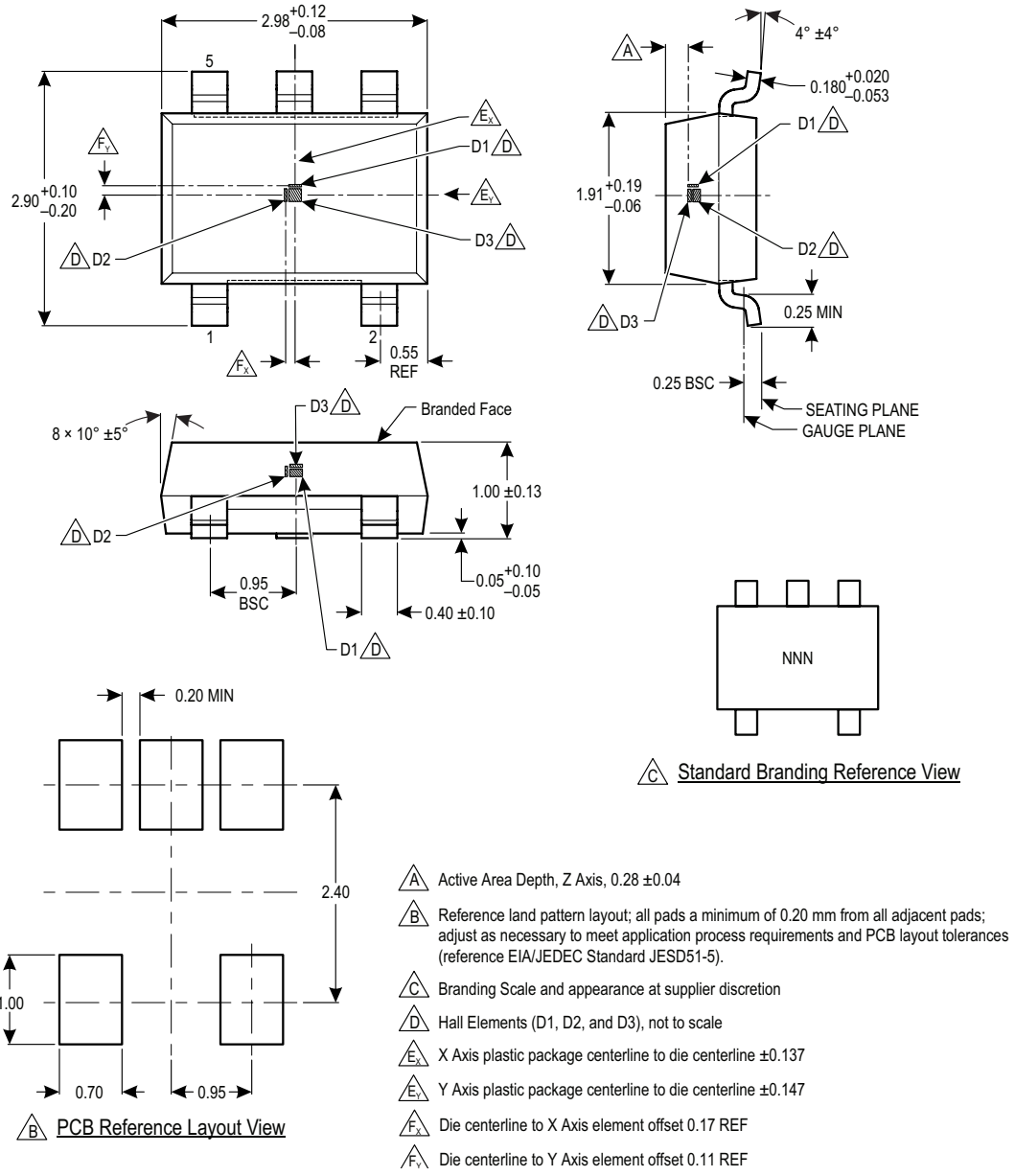

Figure 18: Package LH, 5-Pin SOT23-W

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Revision History

Number	Date	Description
–	August 30, 2022	Initial release
1	December 1, 2022	Updated selection guide (page 2), updated electrical characteristics table (page 6)

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