



A Standard Branding Reference View

N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

For reference only, not for tooling use (reference Allegro DWG-0000382, Rev. 2 except for fused current path)

Dimensions in millimeters

Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Fused sensed current path

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed current path and terminals

E Branding scale and appearance at supplier discretion