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TECHNIQUES FOR MITIGATING INTERFERENCE WHILE MEASURING HIGH FREQUENCY, HIGH CURRENT TRANSIENT RESPONSES

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ABSTRACT

This application note will demonstrate techniques on how to avoid coupling the field from high-current transients onto the signal and power lines of current sensors in order to avoid a perceived distortion of the output. Along with creating transient fields, the circuitry used to create current steps can change its power draw quickly, which may disrupt power to a device. The related Power-On Reset event and the waveforms that indicate this event will be explored.

INTRODUCTION

When taking measurements in a laboratory with switching equipment, it is important to take care so that high frequency signals do not couple field onto signal or power wires. Wires that run close to switching circuitry or high current traces, especially if in a loop, are often places of concern where magnetic fields may couple and cause measurement error. This can lead to ground bounce, changes in supply voltage, current injection, and other phenomena which may change the apparent performance of a device.

Switching equipment is used to create an input current step to test the response time or sensitivity of current sensing devices. Coupling is a concern when working with current steps created by large capacitor banks. When they begin to charge or discharge, the capacitor banks can instantaneously spike their current draw, which can temporarily change the voltage at the V_{CC} or Gnd node. If for any reason the supply voltage to the part is reduced enough, the part may reset. Detecting this behavior is difficult. The reset can appear on either edge of the current step and the output may not discharge immediately, depending on the load capacitance.

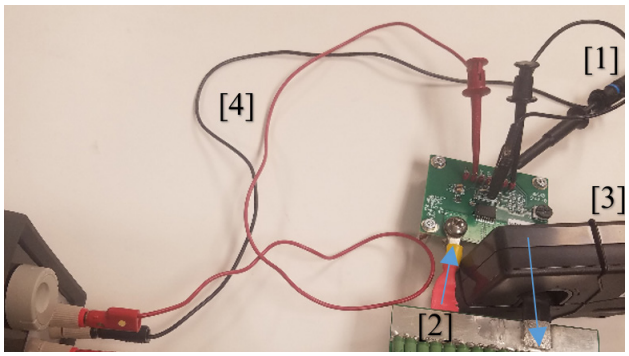

Figure 1: Poor setup allowing coupling onto V_{CC}
[1]: Scope Probe
[2]: Current Injection Board (arrows indicate current direction)
[3]: Current Monitor Probe
[4]: V_{CC} and Gnd Leads

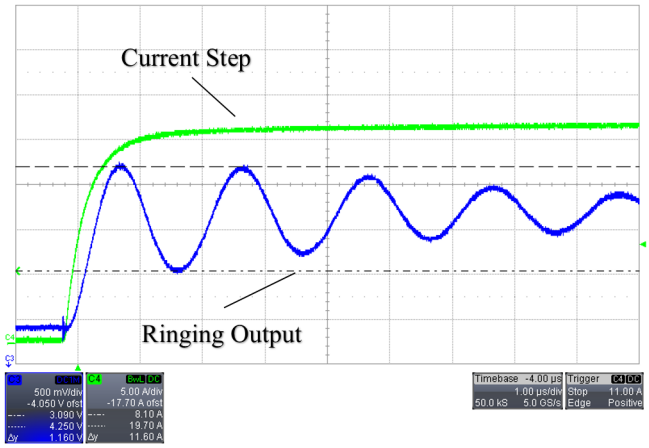

Figure 2: Poor setup output ringing

Lab conditions can be cramped, often with little room to separate equipment and devices being tested. It is important to take care to distance switching equipment from test leads as well as devices while taking measurements. Running the power leads away from the switching of the current injection board eliminated the ringing on the output of the device in this experiment. Figure 3 shows the leads taped away from the current injection board and Figure 4 shows the resulting clean signal overlaid upon the ringing signal.

The small change made by moving the wires away from the current injection board completely eliminated the ringing. Allegro recommends twisting together V_{CC} and Gnd away from any power circuitry to reduce inductance and avoid coupling.

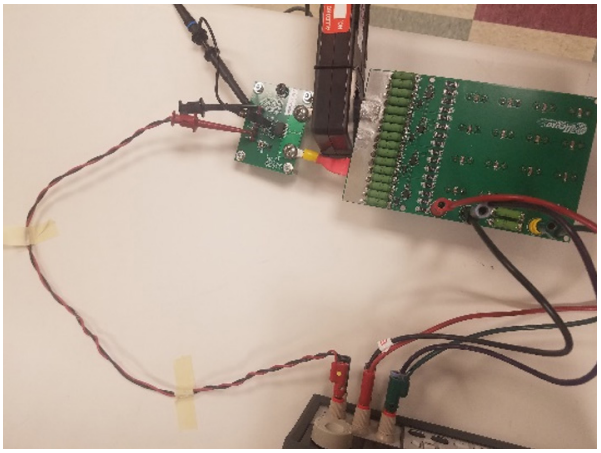

Figure 3: Clean setup minimizing coupling onto power wires of the device

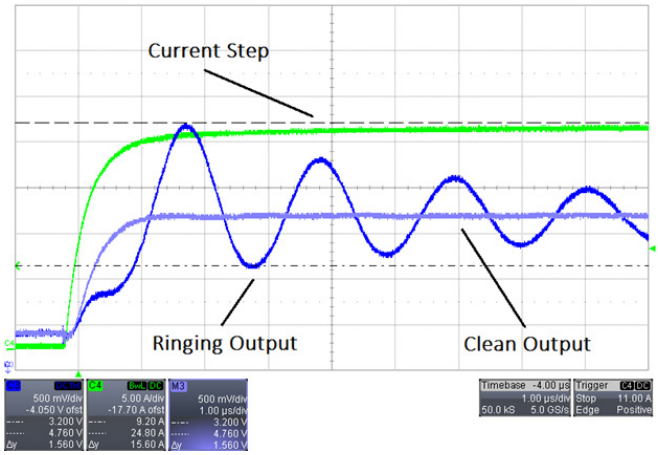

Figure 4: Clean trace overlaid with ringing trace

Output Undershoot Due to Current Transients

In the second laboratory setup, a single inline package (SIP) device was used to demonstrate an undershoot condition. The device was placed inside of a concentrator with a bus bar running through it. The current running through the bus bar creates a magnetic field which is steered by the concentrator orthogonally into the Hall plate. The signal pins and test leads sit near where the magnetic field is being steered, allowing it to couple onto them.

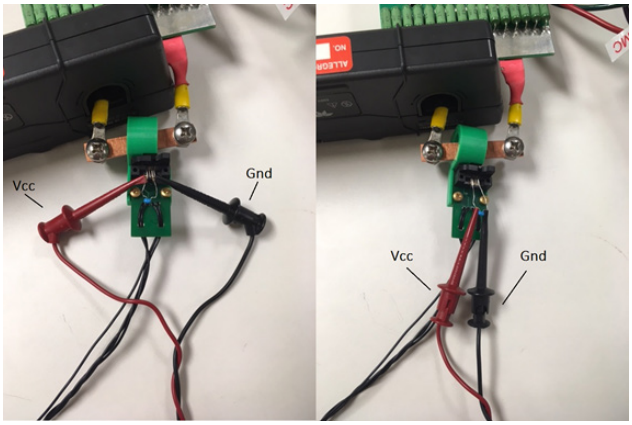

Figure 5: A1367 high coupling setup (left) and low coupling (right)

When the Gnd and V_{CC} clips were connected parallel to the bus bar, as shown in the picture on the left in Figure 5, it allowed for the maximum coupling of magnetic field onto the clips. The picture on the right in Figure 5 shows the clips perpendicular to the bus bar, which minimized field coupling. A dramatic difference was observed on the output after this change was made. Bringing the clips perpendicular not only mitigated this undershoot seen in Figure 6, but Figure 7 shows that ringing has also been removed. Note that neither the gain of the device nor the scope scaling was changed between Figure 6 and Figure 7, only the offset to capture the whole undershoot.

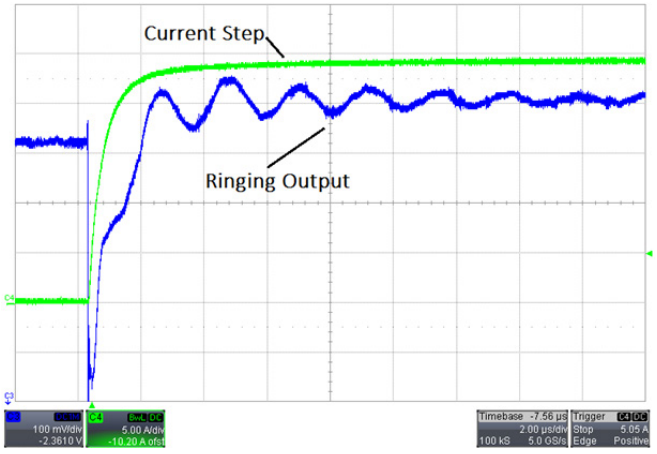

Figure 6: Parallel setup with significant undershoot and ringing

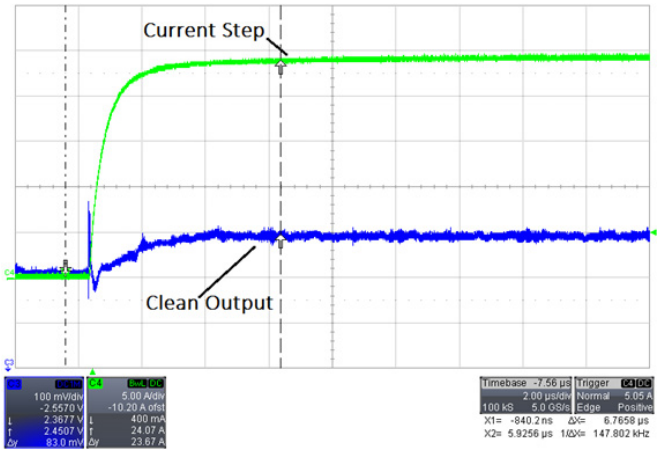

Figure 7: Perpendicular setup with minimal undershoot and ringing

Power-On Reset events due to V_{CC} Chopping

A third experiment highlights a scenario involving fast switching of capacitors to generate a high-speed current transient. These high-current transients have been seen to couple onto the system's supply voltages and create disturbances on sensors and microprocessors. This can cause V_{CC} and Gnd to fluctuate, which will disrupt the device, as seen in Figure 8. Extreme situations may cause V_{CC} to drop low enough to cause a Power-On Reset (POR) condition; the device will repower due to V_{CC} dropping too low for too long. This VCC disturbance can be fast—less than 100 ns—and still cause a reset condition. Bypass capacitors help prevent V_{CC} from fluctuating quickly; however, this is a result of the setup or layout chopping V_{CC}, not an issue with the part reacting to a step response.

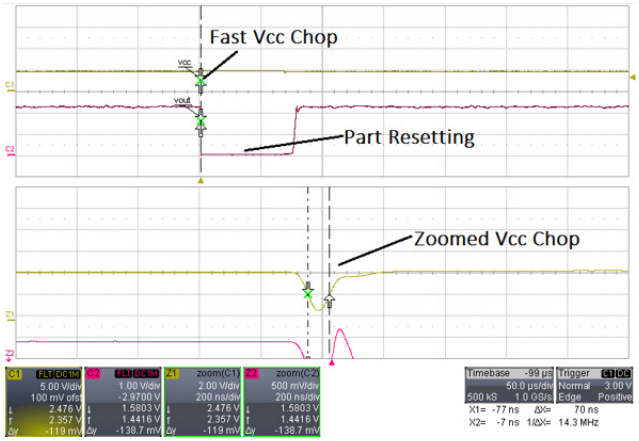

Figure 8: Device resets from V_{CC} pulled low briefly

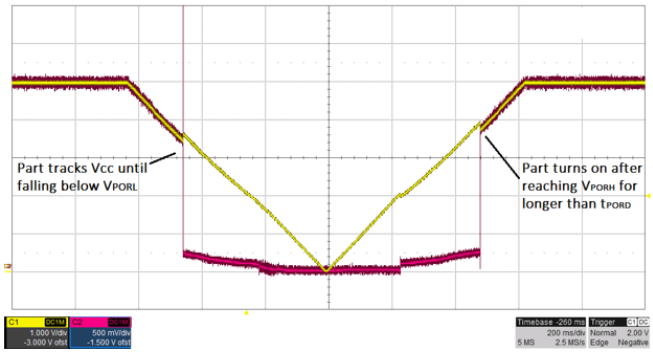

Figure 9: Part output during slow V_{CC} ramp

While the part resets, the output enters high-impedance mode. The datasheet for an individual part will specify the Power-On Reset thresholds. POR has two thresholds: rising V_{CC} (V_{PORH}) and falling V_{CC} (V_{PORL}). Figure 9 shows the output of a part responding to these thresholds, first becoming underpowered when V_{CC} falls below V_{PORL}, and then powering back on as V_{CC} rises above V_{PORH}.

If a load capacitor is used, the output may appear to slowly settle when the device enters high-impedance mode. This strange behavior can appear to be unrelated to the switching, happening on the down stroke of the current input. In Figure 10, the discharge of the device with and without load capacitors is shown in a V_{CC} chop event. The output quickly drops to ground without a load capactitor, whereas with a 1 nF capacitor, the output only discharges halfway. These two waveforms are indicative of a Power-On Reset event. The output is pulled low when the device begins to turn on.

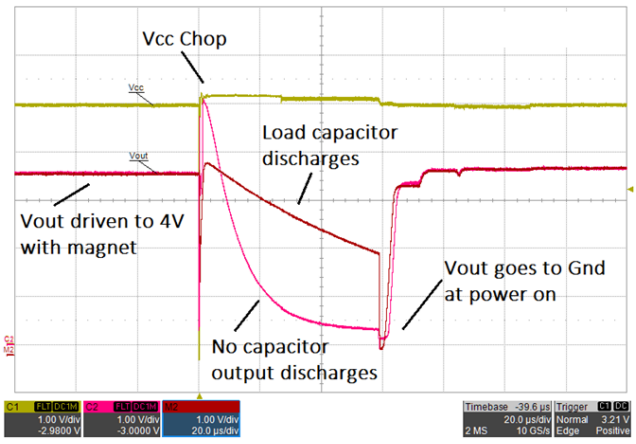

Figure 10: Capacitor discharge as part resets

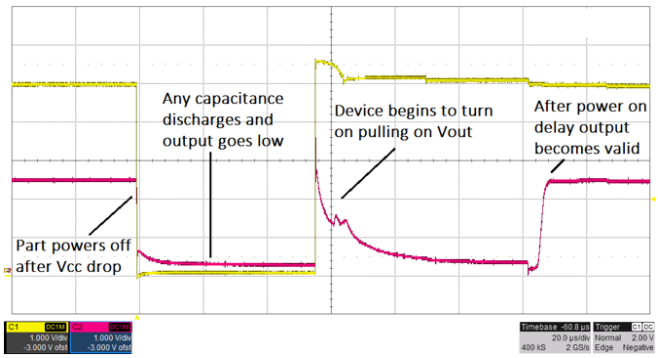

Figure 11: Normal power on and power off functionality

These profiles match with a normal power on and off condition, like those seen in Figure 11. First, any charge stored on the capacitance of the output pin discharges. The output then spikes high when power is restored to the part. Finally, the output pulls low before rising to normal operation.

Conclusion

There are many situations in which an inadequate test setup may cause perceived measurement errors that would not be seen in a true PCB application. While these can seem like functionality problems with the device output or other downstream circuitry, these errors can be minimized with proper setup techniques. Keeping scope leads, signal leads, and power leads perpendicular to high current traces and away from switching circuitry, as well as keeping signal pins isolated from primary pins, which may cause V_{CC} to chop, will help mitigate these problems.

Revision History

Number	Date	Description	Responsibility
–	April 22, 2019	Initial release	M. McNally

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