VIAS-IN-PAD IMPROVES THERMAL PERFORMANCE FOR ALLEGRO CURRENT SENSORS

INTRODUCTION

This application note discusses the effectiveness of using vias-in-pad and other additional printed circuit board (PCB) layout techniques to improve heat dissipation for current sensors with integrated conductors. Optimal heat sinking is necessary to protect the IC from exceeding its maximum junction temperature of 165°C.

BACKGROUND

Integrated Allegro Current Sensor Packages

The Allegro current sensor IC families are fully-integrated current sensing solutions and are leading the industry in power density. Current enters the package through the integrated conductor leads (IP+, IP-) and the resistance of that conductor generates heat that must be dissipated in order to maintain an IC temperature below 165°C. Without any active heat sinking, the main source of passive heat sinking is into the PCB itself. The more metal there is directly connected to the integrated conductor, then the more effective the heat sinking will be. The goal of this application note is to illustrate how to maximize the passive heat sinking into the PCB.

See Table 1 below for a summary of integrated current sensor packages included in this application note. Figure 1 below is a comparison of the die heating from 25°C versus sensed current applied to the package, for various Allegro current sensor packages. Figure 2 below is a comparison of the die heating from 125°C versus sensed current applied to the package.

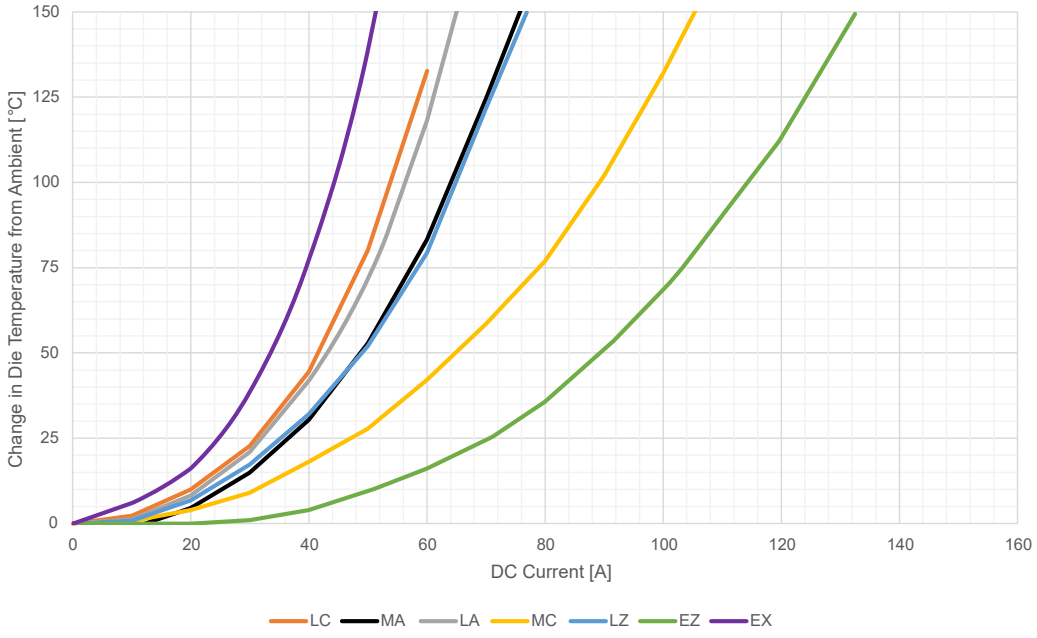


Figure 1: Vias-in-Pad Allegro Lab Results, 125°C

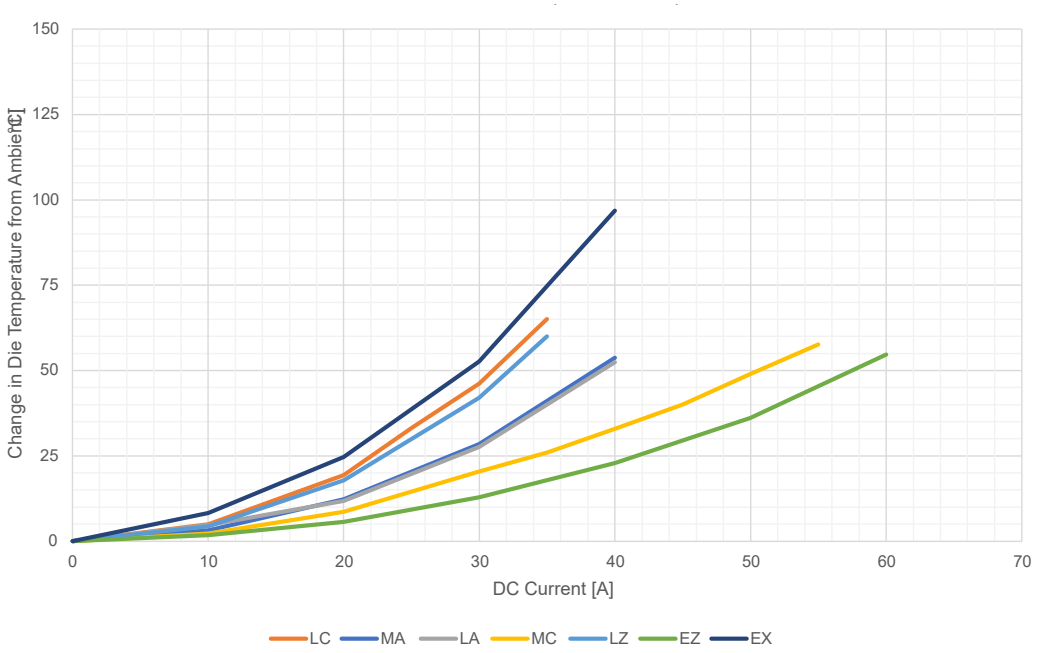
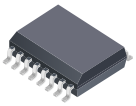
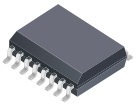
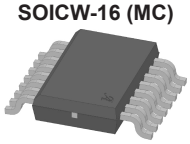


Figure 2: Vias-in-Pad Allegro Lab Results, 125 °C

Table 1: Summary of Allegro Integrated Current Sensor Packages

Package	Primary Conductor Resistance [mΩ]	Size [1] [mm³]	Working Voltage for Functional Isolation [V_{RMS}]	Working Voltage for Basic Isolation [V_{PK}]	Working Voltage for Reinforced Isolation [V_{PK}]	Thermal Characteristics [3][4]	
						Junction to Ambient, $R_{\theta JA}$ [°C/W]	Junction to Top, Ψ_{JT} [°C/W]
6-Pin SOIC (LZ) [2] 	0.68	4.89 × 3.9 × 1.47	–	1188	594	19	0.5
SOIC-8 (LC) 	1.2	4.9 × 6 × 1.62	–	420	—	20	0.8
SOICW-16 (MA) 	0.85	10.3 × 10.3 × 2.65	—	1550	800	20	2.4
SOICW-16 (LA) 	1	10.3 × 10.3 × 2.65	—	870	—	16	–1.7
SOICW-16 (MC) 	0.27	11.3 × 13 × 3.01	—	1618	809	19	2.4
7-Pin QFN (EZ) 	0.1	4 × 4 × 1.45	100	—	—	55	7.5
QFN (EX) 	0.6	3 × 3 × 0.75	100	—	—	18	0.8

[1] PCB layout recommendations can be found in the Appendix section below.
[2] Certification is pending.
[3] $R_{\theta JA}$ is a system-level thermal resistance to heat flow from power dissipated in the package between the circuitry on the chip (Junction) and ambient environment. $R_{\theta JA}$ is commonly based on a 2-layer PCB layout as specified in JESD51. In the case of current sensors, the JEDEC standard board is inadequate as it is unable to handle high currents. $R_{\theta JA}$, as defined here, is based on the Allegro application boards mentioned in this application note, which is optimized for carrying high currents. $R_{\theta JA}$ is highly dependent on the PCB and environment and is good for rough estimation of thermal performance of a package and for comparison between packages.
[4] Ψ_{JT} is a thermal metric for power dissipated in the package defined as the difference between the junction temperature and the maximum temperature at the top of the package. It is a useful shorthand way to determine junction temperature by measuring the temperature on the top of the package. This metric is highly dependent on the PCB and environment. Technically, it is not a resistance and can be negative. This is because unlike most IC packages, the primary heat source (the integrated current loop) is not in the same location as the die, which can result in negative numbers when the top of the package is hotter than the junction.

BENEFITS OF VIAS IN-PAD

The via-in-pad technique implements a via directly under a surface mount component pad connecting the inner layers to the top layer. When using vias-in-pad, the vias should be filled so the solder does not get sucked into the hole, reducing the solder joint quality. The most common via filling material is non-conductive. The via can be also filled with electrically and thermally conductive material, which tends to be more expensive than non-conductive material, and provides marginal improvements over non-conductive fill material. See Figure 3 and Figure 4 showing vias under the copper pads of the LZ package versus no vias under the copper pads.

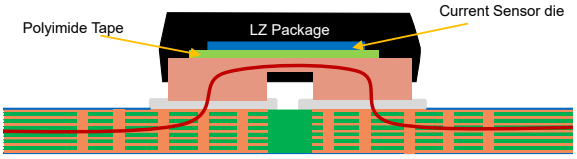


Figure 3: Vias Under Copper Pads, using LZ package in example

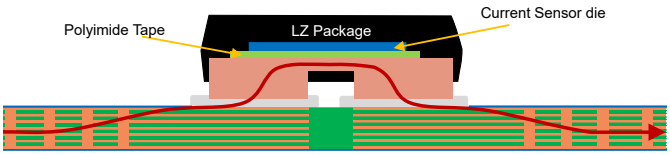


Figure 4: No Vias Under Copper Pads, using LZ package in example

Vias-in-pad are commonly used for thermal performance, space saving, and reduction in electrical resistance:

1. Thermal Performance: By placing the vias directly under the integrated conductor leads, the PCB pad acts as both a current conductor and thermal relief, as shown in Figure 3. In this way, the heat generated by the component can be more efficiently dissipated through the board to the inner metal layers, where the heat can spread more efficiently away from the part.
2. Saving Space: Placing the via directly in the pad can be useful in some designs where space is at a premium, allowing components to be placed closer together. However, in the case where the vias are used to dissipate heat, additional components near the integrated conductor should be minimized to maximize the amount of unbroken metal planes for heat conduction.
3. Reduced PCB Trace Resistance: Because the vias directly connect multiple layers in parallel in the PCB, the resistance from the current source to the integrated conductor leads can be minimized on the PCB, as shown in Figure 3. Resistance in the current carrying layers around the IC will create heat in the PCB (see Figure 7). This will raise the temperature of the PCB around the IC, reducing the temperature gradient for the heat to flow away from the IC.

RESULTS OF IN-PAD VIAS VERSUS NO IN-PAD VIAS

Allegro MicroSystems offers evaluation boards with optimized heat sinking for quickly evaluating Allegro current sensors in a lab environment (shown in Figure 7 below). These boards were used for the following comparisons. Two identical evaluation boards were used for data collection, with the only difference that one used vias-in-pad, while the other only had vias outside of the pads (See Figure 5 and Figure 6 showing the two evaluation boards used for the evaluation of the LC/LZ package. For all other package layout reference views showing vias-in-pad, see the Appendix section below. Not these figures are not to scale). The size of the vias that are used on the vias-in-pad are 0.5mm. The via type is IPC-4761 Type VII: Filled & Capped Via. Non-conductive via fill material was used. These boards have 6 layers, each being 2 oz copper weight.

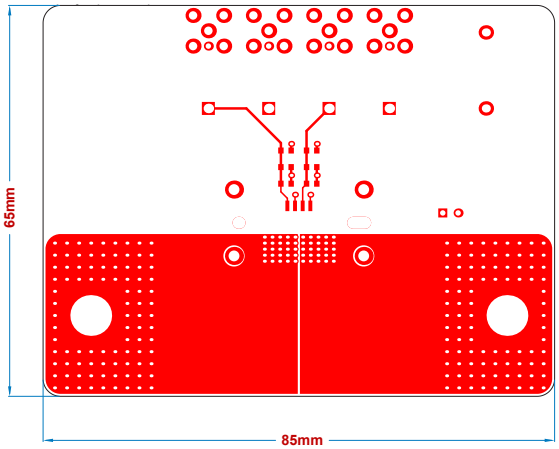


Figure 5: LC/LZ PCB Layout Reference View With Vias-in-Pad

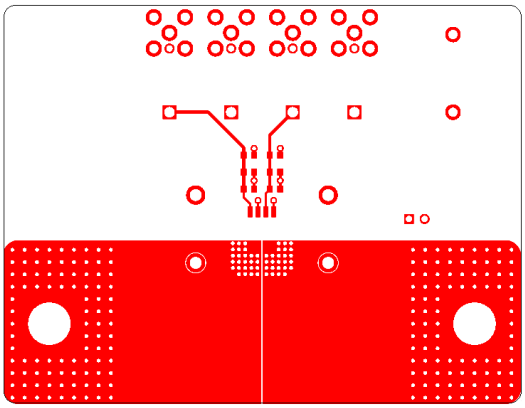


Figure 6: LC/LZ PCB Layout Reference View Without Vias-in-Pad

Testing was conducted at 25°C and 125°C ambient temperatures. The current was conducted to the PCB through 2AWG gauge cables. DC current was then sent through the integrated conductor leads of the device. Die temperature was measured by using the on-chip temperature sensor located after it came to thermal equilibrium. (Note: the on-chip temperature sensor is not available to customers). The change in die temperature was determined by subtracting the measured ambient temperature from the measured die temperature.

Comparison of the thermal performance with and without vias in pad for all the packages can be seen in the plots below. Additionally, comparison of the thermal performance for 25°C vs. 125°C can be seen in the plots below. Note that only the via in pad evaluation boards were used for testing at 125°C. As mentioned, the die temperature should not exceed 165°C, or a rise of 140°C from room temperature (140°C + 25°C = 165°C).

The data demonstrates that using vias-in-pads provides a smaller increase in die temperature than not using vias-in-pads and is recommended by Allegro for all current sensors with integrated conductors.

Allegro recommends that the parts be put through a standard reflow process instead of hand-soldering for the most accurate results. Too much or not enough solder can affect the results. This is especially true for QFN type packages (EZ and EX) where solder voiding is not visible under the part and can significantly affect the heat sinking to the PCB.

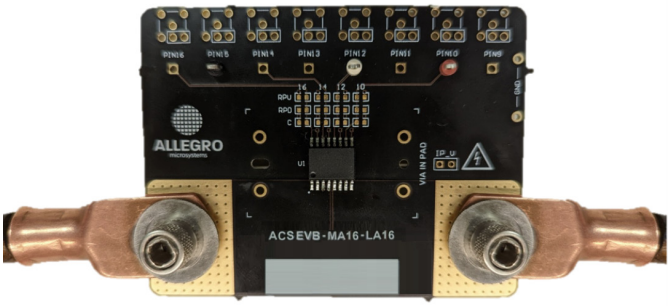


Figure 7: Connection between evaluation board and current carrying cables

LZ Package

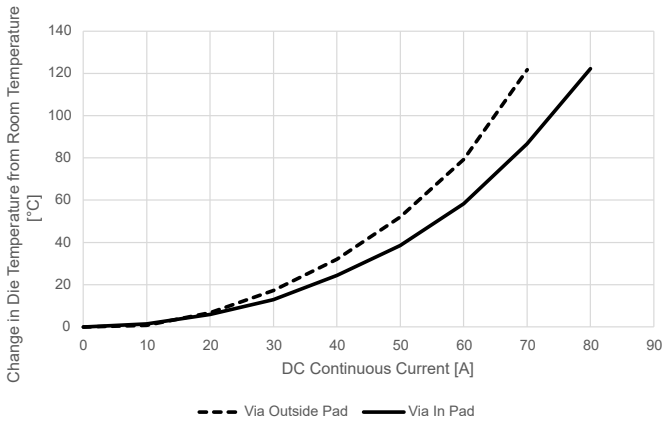


Figure 8: LZ Package Comparison with and without In-Pad Vias

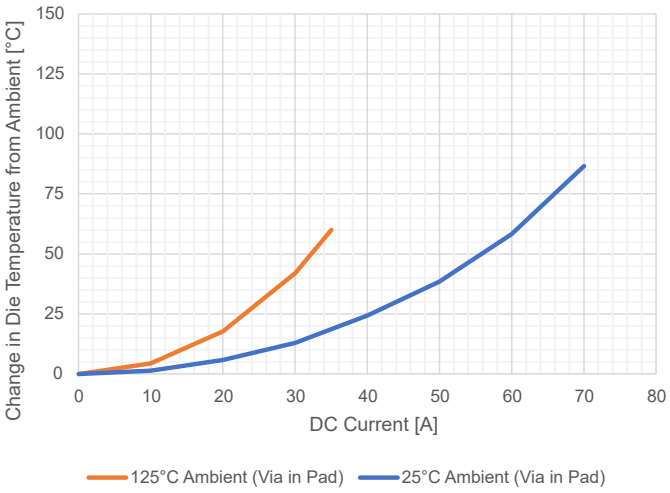


Figure 9: LZ Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

LC Package

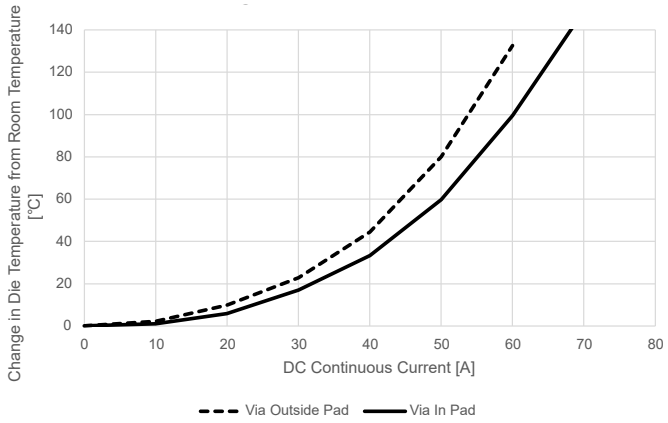


Figure 10: LC Package Comparison with and without In-Pad Vias

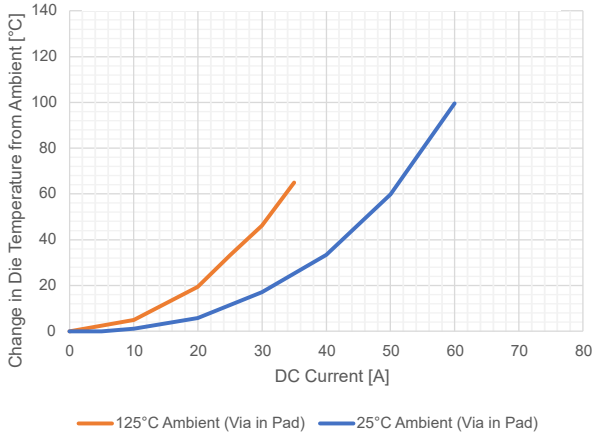


Figure 11: LC Package Comparison 25°C and 125 °C ambient temperatures with In-Pad Vias

MA Package

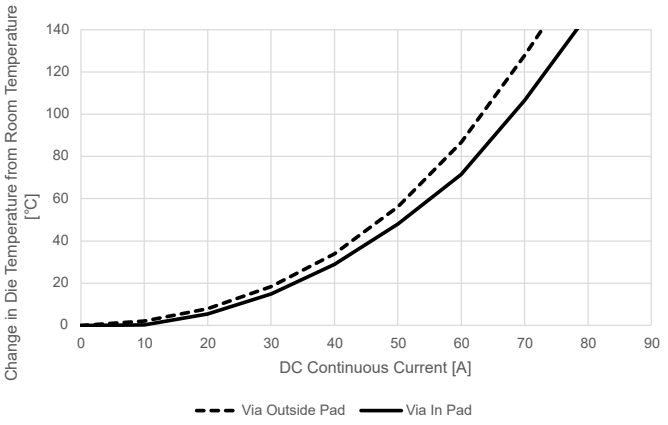


Figure 12: MA Package Comparison with and without In-Pad Vias

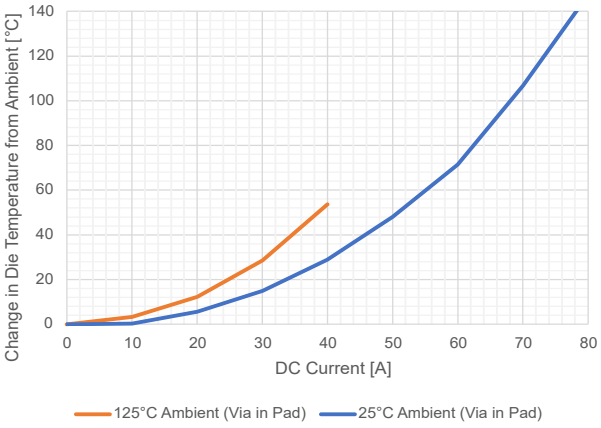


Figure 13: MA Package Comparison 25°C and 125 °C ambient temperatures with In-Pad Vias

LA Package

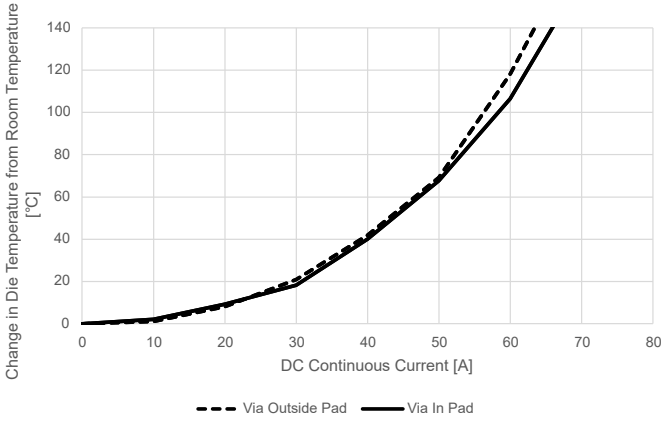


Figure 14: LA Package Comparison with and without In-Pad Vias

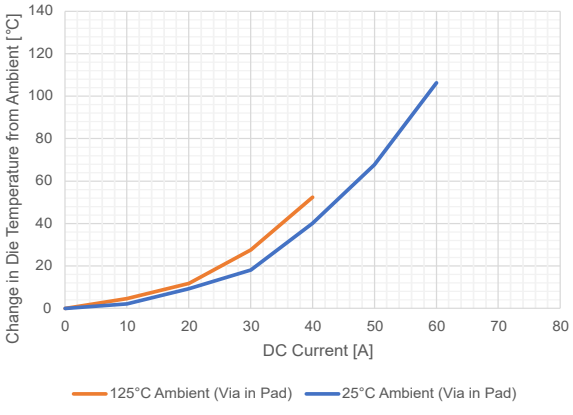


Figure 15: LA Package Comparison 25°C and 125 °C ambient temperatures with In-Pad Vias

MC Package

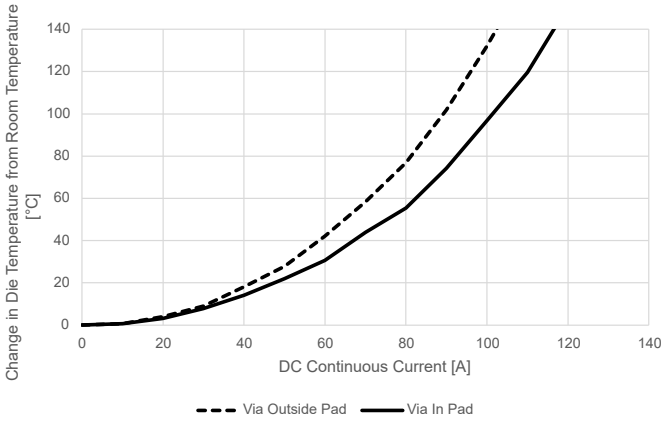


Figure 16: MC Package Comparison with and without In-Pad Vias

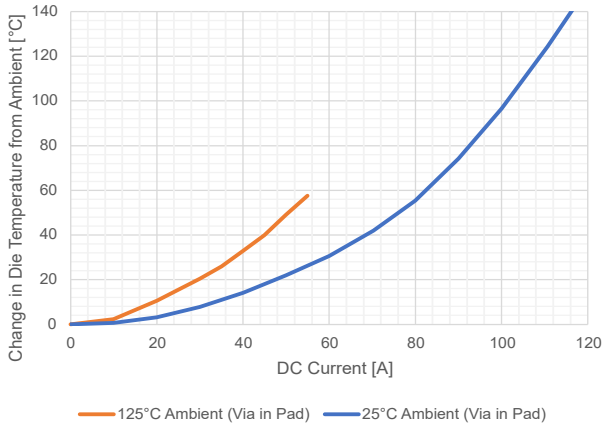


Figure 17: MC Package Comparison 25°C and 125 °C ambient temperatures with In-Pad Vias

EZ Package

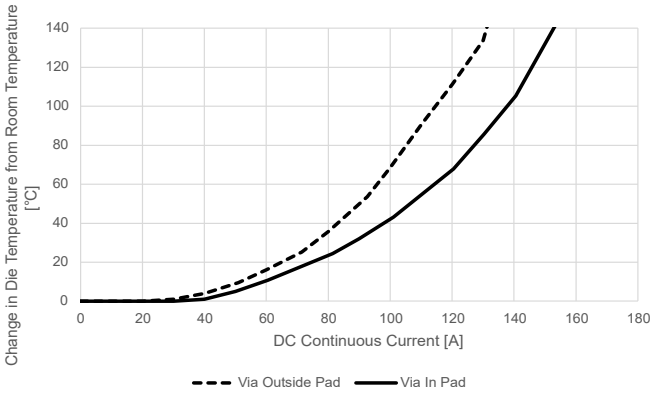


Figure 18: EZ Package Comparison with and without In-Pad Vias

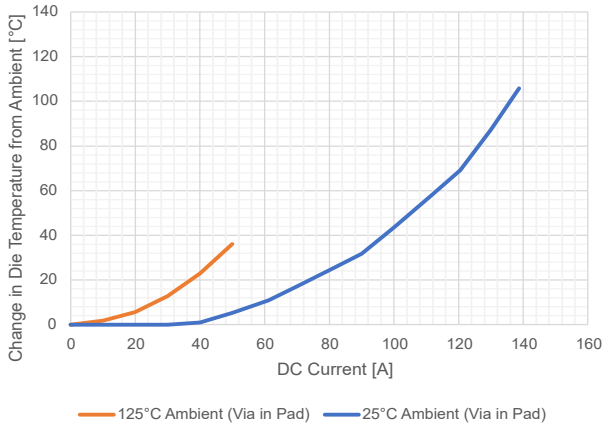


Figure 19: EZ Package Comparison 25°C and 125 °C ambient temperatures with In-Pad Vias

EX Package

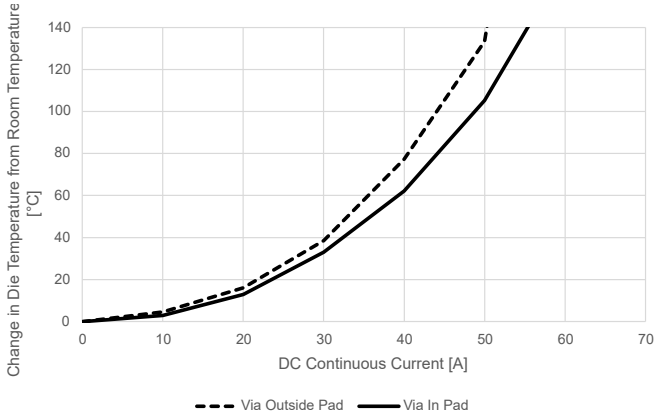


Figure 20: EX Package Comparison with and without In-Pad Vias

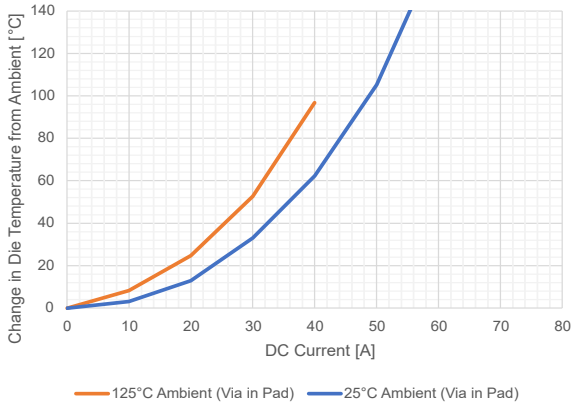


Figure 21: EX Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

Impact of the Temperature Coefficient of Cu

The internal conductor is a copper alloy made up of primarily copper with small amounts of other metals, and for thermal behavior can be considered as pure copper. Copper has a positive resistive temperature coefficient (+0.393 percent per degree C), which means that as the temperature of the conductor increases, its resistance increases as well. This is an almost 40% increase in the power dissipated in the package for an ambient temperature rise of 100°C with no current applied.

For example, 50 A_{RMS} into the MA package, with a resistance of 0.85 mΩ at 25°C ambient, will generate 2.125 W of power inside the package. At 125°C ambient, the power generated will go up to 2.95 W. This does not account for the temperature rise due to the power dissipated in the conductor when current flows. This positive feedback is further reason to remove heat efficiently from the package, to reduce the chance of thermal runaway.

Additional Board Layout Considerations

There are additional important considerations to consider when designing these evaluation boards:

1. Pad Layout: It is recommended to completely overlap the top copper layer with the primary current pads to optimize thermal performance, leaving only a small gap separating the IP+ from the IP- internal conductor pins. The number and size of vias in the overlapping area should be maximized based on the design rules for the PCB manufacturing process.
2. Thermal Management: Additional passive heat sinking or active cooling techniques at the system level may be necessary to dissipate heat away from the current sensor, allowing the junction temperature to stay below 165°C. For isolated applications, it is not advisable to add heat sinks to the top of the package, because these could compromise the creepage distance of the package, unless proper high-voltage isolation methodologies are followed. Because most dielectric insulating materials are also good thermal insulators, adding isolation between the package and heat sink generally reduces any heating sinking efforts. Passive heat sinking through the top of the package can be problematic, and heating through the PCB is the preferred method.
3. Component Placement: Having other components that generate significant amounts of heat near the current sensor can reduce the temperature gradient that allows heat to flow away from the current sensor. The best design practice is to space out the heat generating components as much as possible.
4. Copper Layers: Thicker copper layers have two benefits: better heat conduction away for the part and lower electrical resistance that creates heat. Maximizing the thickness of each layer and maximizing the number of layers that are in direct contact to the current sensor through vias-in-pad will minimize the die junction temperature.
5. Trace Width: High-current traces must be wide enough to keep voltage drop and inductance to a minimum and wide enough to prevent excessive heating. The largest practical PCB traces and board area usage around the current sensor is recommended.
6. Solder Stencil: Voids in the solder on the large current conductor pads (IP+ to IP-) for the QFN EZ package will increase the resistance of the solder joint and reduce the heatsinking to the PCB. Voids should be minimized in the solder joint under the package. Voids can be created by solder flux outgassing. By giving the outgassing a way to escape from under the package during solder reflow voids can be minimized. Adding a grid in the solder stencil will create a path for outgassing to escape from under the package during the wetting process of the reflow.

CONCLUSION

Placing vias under the copper pads of the Allegro current sensor minimizes the current path resistance and improves heatsinking to the PCB for optimal thermal performance when compared to having vias outside of the pads. Additional standard layout techniques can be implemented to further minimizes die heating in operation of integrated conductor current sensors.

RELATED DOCUMENTATION AND APPLICATION SUPPORT

Documentation	Summary	Location
Allegro MicroSystems Website	Link to Allegro MicroSystems website	https://www.allegromicro.com/en/
Allegro Current Sensor FAQ	Answers to frequently asked questions about Allegro's industry-leading current sensor ICs	https://www.allegromicro.com/en/products/sense/current-sensor-ics/faq
Method for Evaluating Thermal Performance of Allegro Current Sensors in Application	Application notes discussing the thermal performance of Allegro Current Sensor ICs	https://www.allegromicro.com/-/media/files/application-notes/an296236-estimating-junction-temperature.pdf
DC Current Capability and Fuse Characteristics of Current Sensor ICs with 50 to 200 A Measurement Capability		https://www.allegromicro.com/-/media/files/application-notes/an296133-dc-current-capability-fuse-characteristics-current-sensor-ics-50-200-a.pdf
DC and Transient Current Capability/ Fuse Characteristics of Surface Mount Current Sensor ICs		https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/dc-and-transient-current-capability-fuse-characteristics
Current Sensor Thermals Application Note		https://www.allegromicro.com/-/media/files/application-notes/an296190-current-sensor-thermals.pdf
Current Sensing for Power Delivery	This article discusses the advantages of various current sensing methods in power delivery.	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296256-current-sensing-for-power-delivery
Techniques to Minimize Common-Mode Field Interference When Using Allegro Current Sensor ICs (ACS724 and ACS780)	This application note discusses the mechanism of CMR and focus on how to best use this mechanism through optimized circuit board design and layout.	https://www.allegromicro.com/-/media/files/application-notes/an296128-techniques-minimize-common-mode-field-interference.pdf
High-Current Measurement with Allegro Current Sensor IC and Ferromagnetic Core: Impact of Eddy Currents	Application note focusing on the effects of alternating current on current measurement	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296162_a1367_current-sensor-eddy-current-core
Allegro Hall-Effect Sensor ICs	This note provides a basic understanding of the Hall effect and how Allegro designs and implements Hall technology in packaged semiconductor monolithic integrated circuits.	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/allegro-hall-effect-sensor-ics
Hall-Effect Current Sensing in Electric and Hybrid Vehicles	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-electric-and-hybrid-vehicles
Hall-Effect Current Sensing in Hybrid Electric Vehicle (HEV) Applications	Application note providing a greater understanding of hybrid electric vehicles and the contribution of Hall-effect sensing technology	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/hall-effect-current-sensing-in-hybrid-electric-vehicle-hev-applications
Achieving Closed-Loop Accuracy in Open-Loop Current Sensors	Application note regarding current sensor IC solutions that achieve near closed-loop accuracy using open-loop topology	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/achieving-closed-loop-accuracy-in-open-loop-current-sensors
PCB Ground Plane Optimization for Coreless Current Sensor Applications	This application note discusses PCB ground plane optimization for Coreless Current Sensor Applications	https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296277-pcb-ground-plane-optimization-for-coreless-current-sensor-applications

APPENDIX: PCB LAYOUT REFERENCES

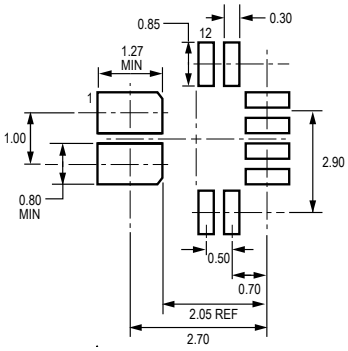


Figure 22: EX PCB Layout Reference View

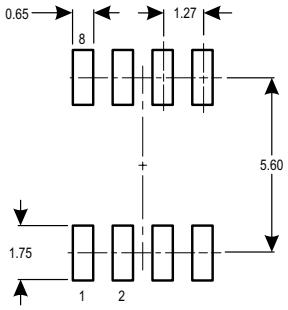


Figure 23: LC PCB Layout Reference View

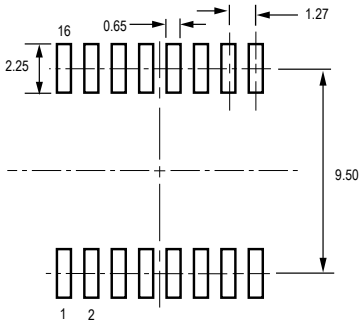


Figure 24: MA/LA PCB Layout Reference View

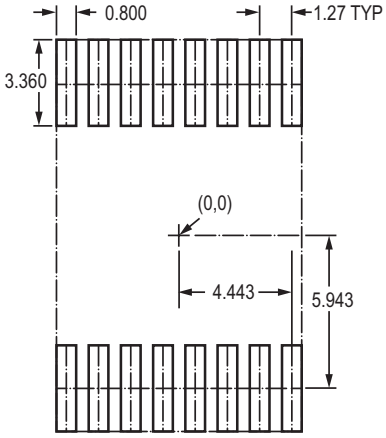


Figure 25: MC PCB Layout Reference View

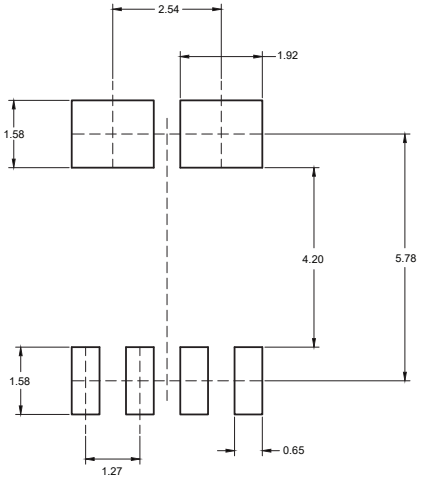


Figure 26: LZ PCB Layout Reference View

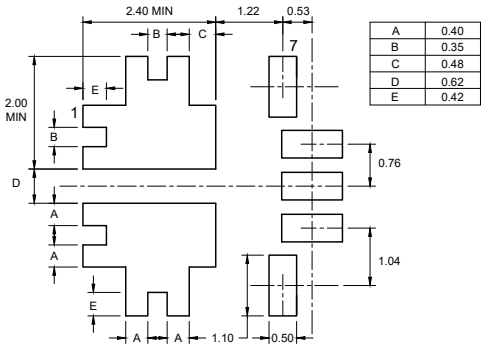


Figure 27: EZ PCB Layout Reference View

APPENDIX: TOP LAYER SHOWING VIA-IN-PAD LAYOUT REFERENCES

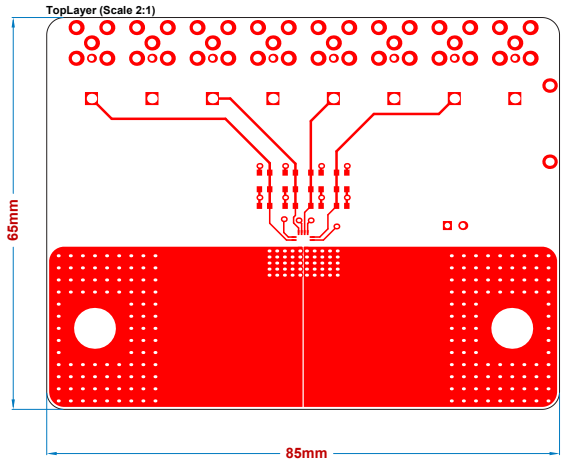


Figure 28: EX PCB Layout Reference View

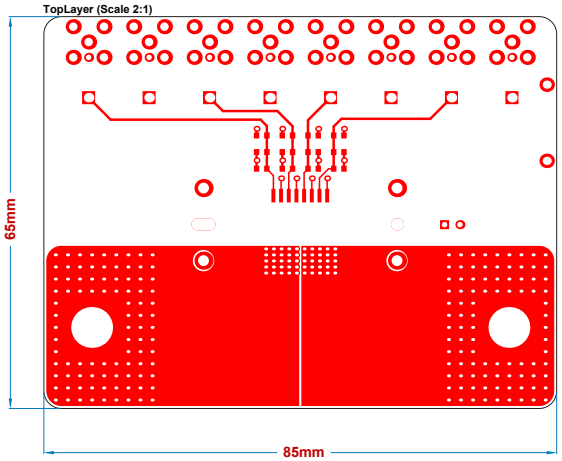


Figure 29: MA/LA PCB Top Layer

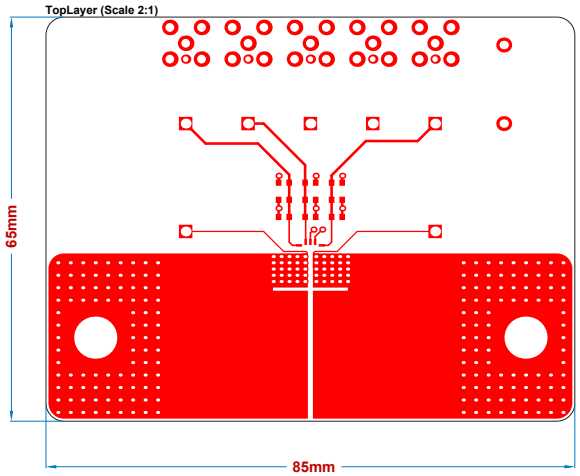


Figure 30: MC PCB Top Layer

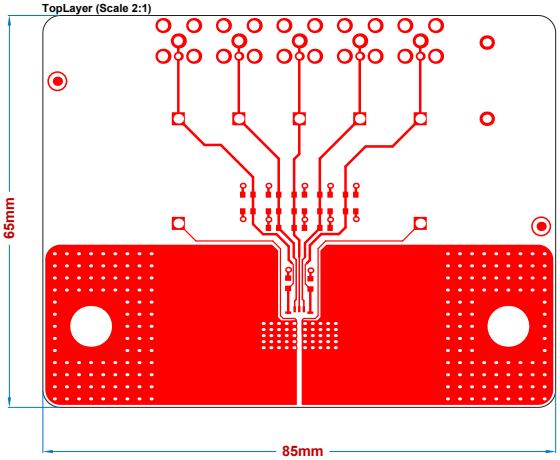


Figure 31: EZ PCB Top Layer

Revision History

Number	Date	Description	Responsibility
–	August 28, 2023	Initial release	K. Hampton
1	October 2, 2023	Added Thermal Characteristic values to Table 1 (page 2); added footnote [3] and [4] to Table 1 (page 2); corrected wire gauge size (page 3); minor editorial updates (all pages)	K. Hampton
2	January 24, 2024	Added 125°C application information (page 2), minor editorial updates (all pages)	K. Hampton

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