A89331

Three-Phase Sensorless Fan Driver

FEATURES AND BENEFITS

- Closed-loop speed control
- Overvoltage protection
- Power loss brake
- Fault mode brake
- Configurable RD or FG output
- Speed curve configuration via EEPROM
- I^2C serial port
- Sinusoidal modulation for reduced audible noise and low vibration
- Sensorless (no Hall sensors required)
- Trapezoidal drive option for high speed
- Low $R_{ds(on)}$ power MOSFETs – 3 A capability
- PWM duty cycle speed input
- FG speed output
- Lock detection
- Soft start
- Shorted load protection

APPLICATIONS

- High-speed 12 V server cooling fans
- Industrial and consumer blowers and fans

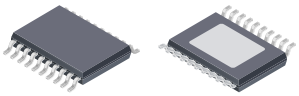
DESCRIPTION

The A89331 three-phase motor driver incorporates sensorless sinusoidal drive to minimize vibration for high-speed server fans. Sensorless control eliminates the requirement for Hall sensors for server fan applications.

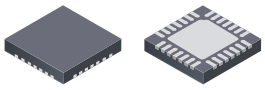
A flexible closed-loop speed control system is integrated into the IC. EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

The A89331 is available in a 28-lead 5 mm × 5 mm QFN with exposed power pad (suffix ET), and a 20-lead TSSOP with exposed power pad (suffix LP).

PACKAGES:



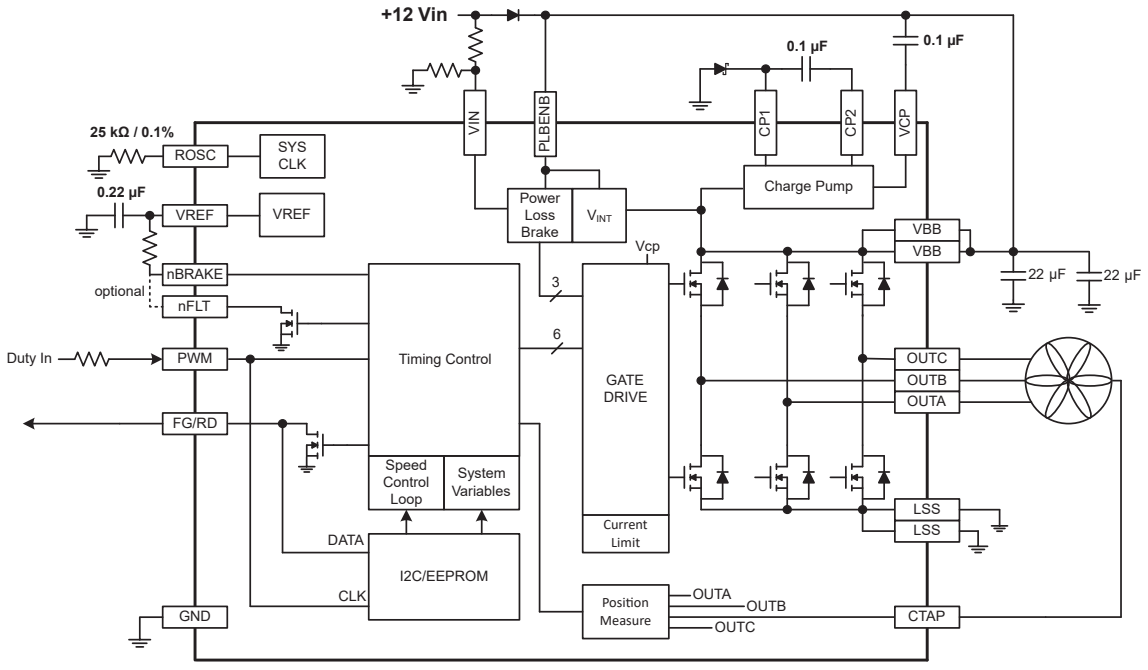
20-lead TSSOP with exposed thermal pad (LP package)



28-contact QFN with exposed thermal pad 5 mm × 5 mm × 0.90 mm (ET package)

Not to scale

TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Package	Packing
A89331GETSR	28-pin QFN with exposed thermal pad	6000 pieces per 13-inch reel
A89331GLPTR-T	20-pin TSSOP with exposed power pad	4000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}	DC	–0.3 to 18	V
		t_w < 10 ms	–0.3 to 20	V
Control Input	V_{IN}, V_{PLBENB}	VIN, PLBENB	–0.3 to 18	V
Analog Input	V_{ROSC}	ROSC	4	V
Logic Input Voltage Range	V_{PWM}, V_{nBRAKE}	PWM, nBRAKE	–0.3 to 6	V
Logic Output	$V_{FG/RD}$, V_{nFLT}	FG/RD, nFLT	V_{BB}	V
Output Current	I_{OUT} [1]	DC	Internally Limited	A
		Peak Brake Mode Current; t < 500 ms	6.5	A
Output Voltage	V_{OUT}		V_{BB} + 1	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A		–40 to 105	°C

[1] Power dissipation and thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	ET package, 2-sided PCB with 1 in.^{2} copper	42	°C/W
		LP package, 2-sided PCB with 1 in.^{2} copper	35	°C/W

*Additional thermal information available on the Allegro website.

RECOMMENDED OPERATIONAL RANGE

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{BB}	DC	8	12	15	V
Logic Input Voltage Range	V_{PWM}, V_{nBRAKE}	PWM, nBRAKE	–0.3	–	5.5	V
Motor Current	I_{OUT}	Peak Motor Phase Current - Sinusoidal Running Mode	–	–	3	A

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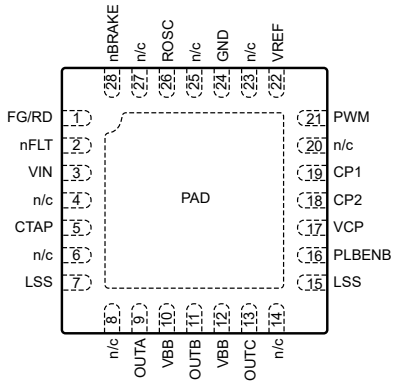
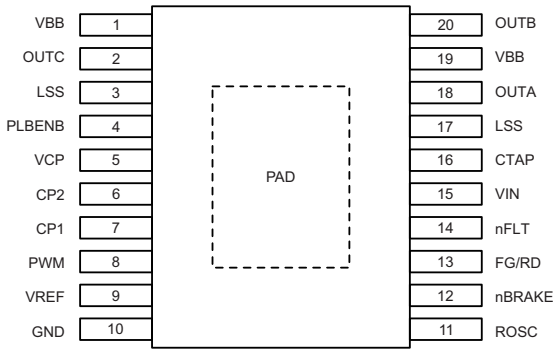
PINOUT DIAGRAMS AND PINOUT LIST



ET-28 Package Pinouts



LP-20 Package Pinouts

Pinout List

Pin Number		Pin Name	Function
ET-28	LP-20		
1	13	FG/RD	Output Signal
2	14	nFLT	Logic Output Signal
3	15	VIN	Power Supply Sense Node
4	–	n/c	No Connect
5	16	CTAP	Motor Terminal
6	–	n/c	No Connect
7	17	LSS	Low Side Source Connection
8	–	n/c	No Connect
9	18	OUTA	Motor Terminal
10	19	VBB	Input Supply
11	20	OUTB	Motor Terminal
12	1	VBB	Input Supply
13	2	OUTC	Motor Terminal
14	–	n/c	No Connect

Pin Number		Pin Name	Function
ET-28	LP-20		
15	3	LSS	Low Side Source Connection
16	4	PLBENB	Logic Input
17	5	VCP	Charge Pump Capacitor
18	6	CP2	Charge Pump Capacitor
19	7	CP1	Charge Pump Capacitor
20	–	n/c	No Connect
21	8	PWM	Logic Input – Speed Demand
22	9	VREF	Reference Voltage Output
23	–	n/c	No Connect
24	10	GND	Ground
25	–	n/c	No Connect
26	11	ROSC	Analog Input
27	–	n/c	No Connect
28	12	nBRAKE	Logic Input

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_J = 25°C, V_{BB} = 5 to 16 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	$V_{IN} > V_{INTH}$, $V_{BB} > V_{BBUVLO}$	–	13.5	16.5	mA
	I_{BB2}	$V_{IN} < V_{INTH}$	–	0.5	1.35	mA
VREF	V_{REF}	I = 0 to 10 mA	2.75	2.85	2.95	V
VCP UVLO	V_{CPUVLO}	Falling	3.6	3.9	4.2	V
		Rising	3.95	4.25	4.55	V
POWER DRIVER						
Total Driver $R_{ds(on)}$ (Sink + Source)	$R_{ds(on)}$	I_{OUT} = 1.5 A, T_J = 25°C, V_{BB} = 12 V	–	210	250	mΩ
		Source driver	–	105	–	mΩ
		Sink driver	–	105	–	mΩ
		I_{OUT} = 1.5 A, T_J = 125°C, V_{BB} = 12 V	–	300	360	mΩ
		Source driver, T_J = 125°C	–	150	–	mΩ
		Sink driver, T_J = 125°C	–	150	–	mΩ
SPEED CONTROL						
PWM Duty Input	f_{PWM}		0.1	–	100	kHz
Duty Cycle On Threshold	DC_{ON}	Relative to target	–0.5	–	0.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to target	–0.5	–	0.5	%
Speed Setpoint	f_{SPD}	T_J = 25°C, R_{OSC} = 25 kΩ	–1.5	–	1.5	%
		T_J = –40°C to 125°C, R_{OSC} = 25 kΩ	–2	–	2	%
System Oscillator	f_{OSC}	T_J = 25°C, R_{OSC} = 25 kΩ	–1	–	1	%
		T_J = –40°C to 125°C, R_{OSC} = 25 kΩ	–1.5	–	1.5	%
PROTECTION CIRCUITS						
Lock Protection	t_{OFF}	Relative to target	–10	–	10	%
Overcurrent Limit	I_{OCL}	$V_{BB} > V_{BBUVLO}$	–25	–	25	%
Overcurrent Protection	I_{OCP}		6.5	–	–	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
VREF UVLO	$V_{REFUVLO}$	V_{REF} rising	2.56	2.63	2.75	V
		V_{REF} falling	2.4	2.48	2.55	V
VREF UVLO Hysteresis	V_{REFHYS}		100	150	200	mV
VBB Overvoltage	V_{BBOVTH}		16.5	17.25	18	V
VBB Overvoltage Hysteresis	V_{BBOHYS}		–	1.5	–	V
VBB UVLO	V_{BBUVLO}	V_{BB} rising	6.5	6.7	6.9	V
VBB UVLO Hysteresis	$V_{BBULOHYS}$		–	500	–	mV
VIN Logic Threshold	V_{INTH}	V_{IN} falling	–	2.5	–	V
VIN Logic Hysteresis	V_{INHYS}		–	400	–	mV
VIN Pulldown Resistor	R_{VINPD}		–	300	–	kΩ
VBB Regulated Boost Voltage	V_{BOOST}	$V_{IN} < V_{INTH}$	4.3	5	5.8	V
VBB Boost Low Threshold	V_{BBTH}		–	1.1	–	V
Boost Switching Frequency	f_{BOOST}		–	41	–	kHz

Continued on next page...

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_J = 25°C, V_{BB} = 5 to 16 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC / IO / I²C						
Logic Input Low Level	V_{IL}		0	–	0.8	V
Logic Input High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mv
Logic Input Current	I_{IN}	PWM, nBRAKE	–10	<1	10	uA
		PLBENB, V_{IN} = 0 V	–	100	–	uA
Output Saturation Voltage (FG/RD, nFLT)	V_{SAT}	I = 5 mA	–	–	0.3	V
Output Leakage (FG/RD, nFLT)	I_O	V = 16 V, switch OFF	–	–	5	µA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		8	–	400	kHz
Bus Free Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	ms

[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A89331 targets high-speed fan applications to meet the objectives of minimal vibration, high efficiency, and ability to customize the IC to the speed control specification.

In typical systems, an MCU is required to meet each application specification. The A89331 integrates the basic closed-loop speed control function, thus allowing elimination of the cost, PCB space, and programming requirements of a custom MCU.

For each specific application, the EEPROM settings can be created with the Allegro EVB and software. Contact Allegro sales to order the custom IC. (Minimum volume requirements will apply).

The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 10-bit number. This “demand” is translated to a speed signal based on settings that are configured via EEPROM.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, overvoltage monitor, and thermal shutdown.

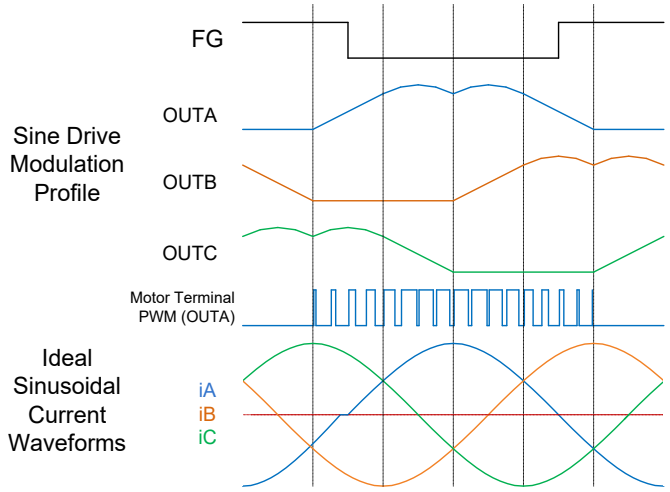

Figure 1: Sinusoidal Drive Sequence for DIR = HI

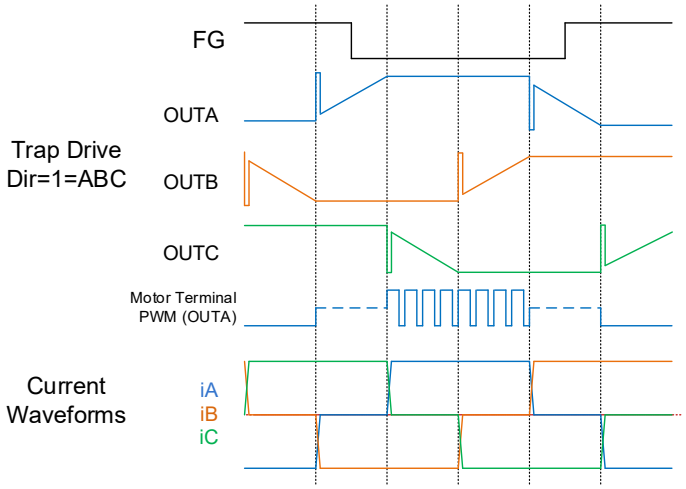

Figure 2: Trapezoidal Drive Sequence for DIR = HI

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FG/RD

Open-drain output, function determined by selection of EEPROM bit FGRD as shown in table below. Additionally, the FG/RD pin serves as the data line (SDA) for I²C communication.

FGRD EEPROM Bit	FG/RD Function
0	FG
1	RD Alarm

PWM

Speed demand input. Duty cycle is measured and translated to target speed request. Additionally, the PWM pin serves as the clock line (SCL) for I²C communication.

CTAP

This analog input is an optional connection for motor common (Wye motors). If not used, as in case of delta wound motor, then pin must be left open circuit.

ROSC

System clock reference. Connect 0.1% 25 kΩ resistor between ROSC and GND pin.

nBRAKE

Active low signal turns on all low-sides for braking function. This pin can be used to prevent coast operation during fault conditions. Brake function overrides speed control input. Brake input is ignored during TSD event or if ($V_{BB} > V_{BBOVLO}$) or ($V_{BB} < V_{BBUVLO}$). Care should be taken to avoid exceeding the maximum ratings of the MOSFETs when braking while motor is running. With braking, the current will be limited by V_{BEMF}/R_{MOTOR}.

PLBENB

Active high control input to enable power loss brake function. Pin should be connected directly to VBB or GND on PCB. If PLBENB function is disabled, the motor will coast when power is disconnected.

VIN

Connect to input power supply at connector to the anode of the required power supply blocking diode. This pin will pull down when power supply is disconnected and trigger the power loss function when voltage drops to V_{INTH}. A series resistor is needed for reverse polarity protection.

Overvoltage Protection

The A89331 will disable the motor outputs when the power supply voltage exceeds V_{BBOVTH}.

Lock Detect

The A89331 will turn off for the programmed time (t_{OFF}) when the rotor is in a locked condition.

OCL

An optional overcurrent limit function can be set to four different levels via EEPROM. Current limit must be enabled via EEROM bit OCLD set low. If enabled, then OCL bits in the EEPROM control the level as follows.

Code	I_{OCL} (A)
00	3.2
01	2.6
10	1.8
11	1

OCLOPT	OCLD	Overcurrent Limit Function
0	0	Source drivers disabled for fixed t_{OFF} when threshold is reached
1	0	Applied duty is reduced when overcurrent threshold is reached
X	1	Disabled

OCP

Overcurrent protection is intended to protect the IC from application conditions of shorted load, motor short to ground, and motor short to battery. The OCP protection monitors the drain to source voltage (V_{DS}) across any source or sink driver when the output is turned on. If the OCP threshold is exceeded for a short blank time, all drivers are shut off. This fault mode can be reset by PWM OFF/ON cycle or power cycle.

Pin shorts to GND (low inductance) on PCB should be avoided. It is possible during startup that the applied duty can be set below the blank time of the OCP circuit. For this scenario, there can be multiple pulses of high current that may overstress the IC before the OCP shutdown can occur.

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FG/RD

The following signals will bring output nFAULT low:

- VBB Undervoltage
- Thermal Shutdown
- Charge Pump UVLO
- VBB Overvoltage
- Output VDS Fault (OCP)
- Loss of synchronization

The fault output can be connected to Brake pin to allow motor brake mode for particular faults as shown in the table below.

Fault	Brake i/p	Fault Action	Latched	Readback Reg. [Bit]
VBB Undervoltage	X	Disable Outputs	N	147[8]
TSD	X	Disable Outputs	N	147[6]
VBB Overvoltage	X	Disable Outputs	N	147[9]
Charge Pump	H	Disable Outputs	N	147[7]
	L	Brake	N	
VDS Fault	H	Disable outputs, Fault reset by PWM off→on command or VBB Undervoltage	Y	147[5:0]
	L	Brake	Y	147[5:0]
Loss of Sync	H	Set Lock detect timeout – motor coasts	N	148[6:0]
	L	Set Lock detect timeout – motor Brake	N	148[6:0]

Charge Pump

An integrated charge pump provides an above VBB supply to drive the gates of the high-side MOSFETS. Connect 0.1 µF / 25 V ceramic capacitors between VCP and VBB and between CP1 and CP2. To prevent negative voltages on CP1 terminal, connect a Schottky diode between GND and CP1 as shown on block diagram.

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Power Loss Brake

If input power is lost to AMT89331, a brake function can be applied to slow down the motor. With a spinning motor, bemf voltage is generated on motor outputs. This voltage will be rectified by the body diodes on output DMOS devices and the VBB power supply capacitor. If adequate voltage can be stored on VBB capacitor, then the low-side DMOS devices can be turned on to provide braking force to the motor. When the motor slows down, the bemf voltage is reduced. At some point there will not be enough voltage on VBB pin to power the low-side drive, so the braking force will not be applied.

The AMT89331 power loss brake circuitry boosts the voltage on VBB line when motor is spinning by pulsing the motor windings off. If motor is rotating, there will be current in the motor winding during the applied brake. This current can be used to charge up VBB line by pulsing off the brake mode for a short time, similar to hysteretic boost converter operation.

VIN	PLBENB	V_{BB}	Mode of Operation	Notes
LOW	VBB	< V_{BBTH}	Coast – No Braking	
LOW	VBB	> V_{BBTH} and < V_{BOOST}	BRAKE PWM	V_{BB} ramps up to V_{BOOST} if motor spinning fast enough.
LOW	VBB	V_{BOOST}	BRAKE - hysteretic boost	V_{BB} regulated to V_{BOOST}.
LOW	VBB	> V_{BOOST}	BRAKE	V_{BB} decays depending on IBB2 and V_{BB} capacitance.
HIGH	X	< V_{BBUVLO}	Coast – No Braking	Power up or power down
HIGH	X	> V_{BBUVLO}	Run Mode	VREF powers up logic; motor starts if PWM signal valid
LOW	GND	X	Coast – No Braking	Connect PLBENB to GND to disable power loss brake

Note: V_{IN} < V_{INTH} = LOW, V_{IN} > V_{INTH} = High

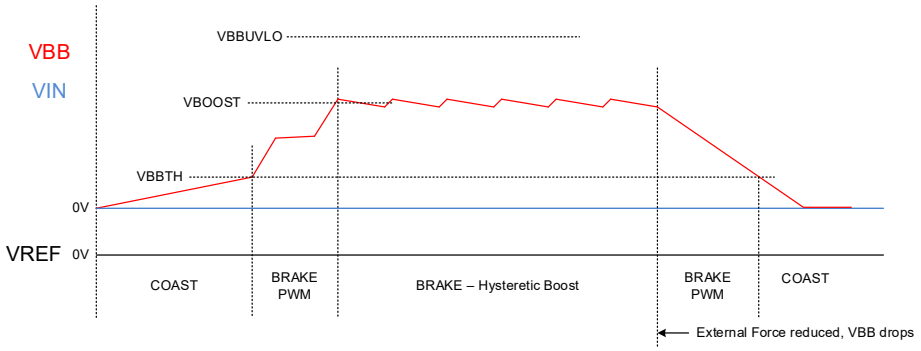

Figure 3: Motor spinning by external force, no power applied to fan module

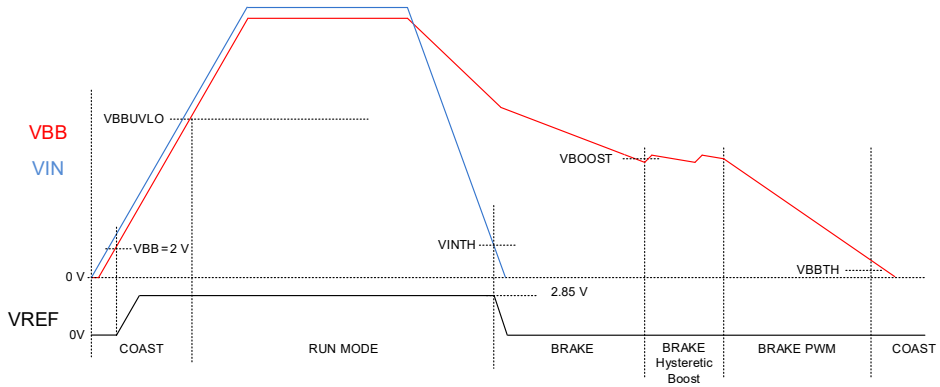

Figure 4: Normal Power Sequence

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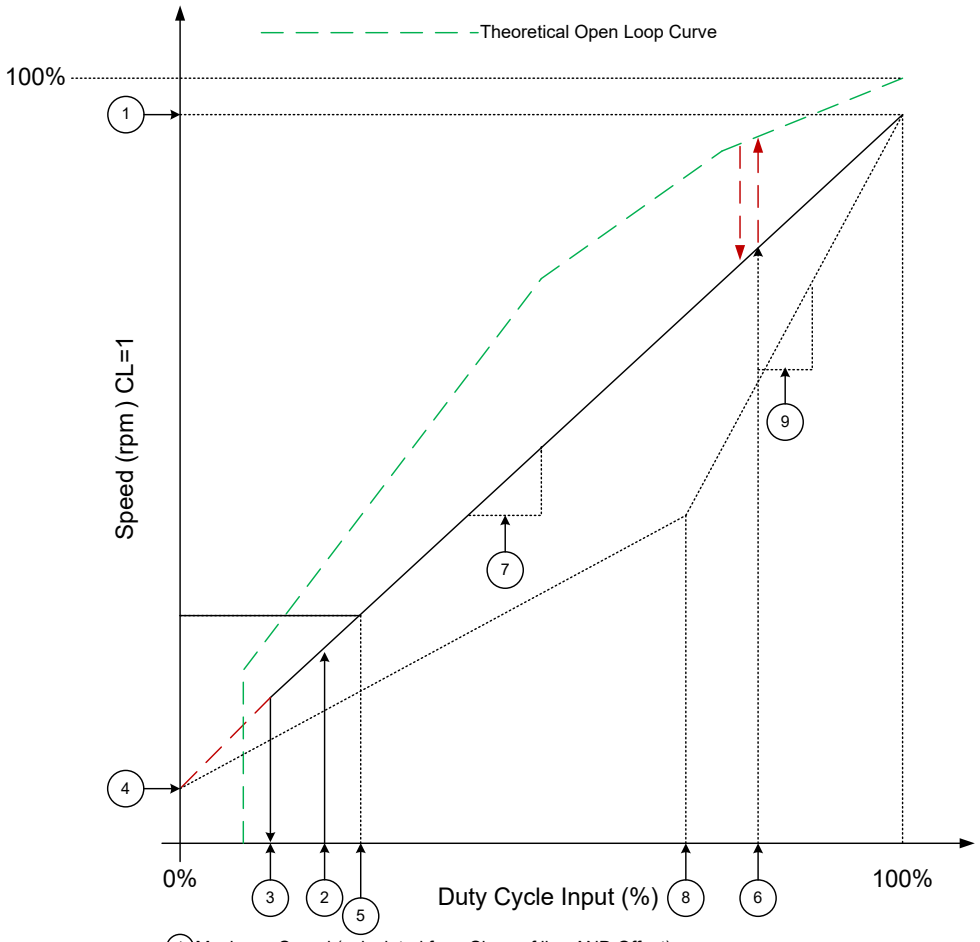

1 Maximum Speed (calculated from Slope of line AND Offset)
2 Duty On (DCON/511)
3 Duty Off (DCOFF/511
4 MINSPD
5 Min Duty Clamp
6 Max Duty Threshold and Hysteresis
7 Slope (based on SPDSLP variable)
8 Slope Switch Duty
9 Slope 2 Option

Figure 5: Speed Curve Parameters

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Speed Curve Parameters (continued)

Refer to Figure 5 for below items.

Minimum Speed Set Point

The minimum speed is defined by the value stored in EEPROM variable MINPWM. The resolution is 1 rpm.

MINPWM (RPM) = 0..4095

Maximum Speed Set Point

The A89331 calculates the maximum speed based on line equation y = mx + B. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable PWMSLP.

PWMSLP = 64 × (Maximum Speed (rpm) – MINPWM) / 1023

Example: Max Speed = 25000, Min Speed = 3000.

PWMSLP = 64 × 22000 / 1023 = 1376

where PWMSLP = 0..8192.

Motor Speed (rpm) = Slope × DutyIN + MINPWM.

where Slope = PWMSLP × 1023 / 64 and DutyIN expressed in %.

Duty In Enable Threshold

EEPROM variable DCON defines the input duty signal that enables the drive. DCON is a 8-bit number with a resolution of 0.2%, which results in a maximum setting of 49.9%.

Duty On (%) = 100 × (DCON × 2) / 1023

If DCON is set to “0”, the motor will turn on with 0% duty cycle input.

Duty In Disable Threshold

EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

Duty Off(%) = DCOFF × 2 / 1023

DCOFF should always be set to a lower number than DCON.

Duty Cycle Invert

To create mirror image of speed curve, set duty cycle invert bit to “1”.

Minimum Duty Clamp

Minimum speed can be clamped to a value to allow the motor to run at defined low-level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

Min Duty Clamp (%) = 100 × MINDTY × 4 / 1023

Therefore, the minimum speed will be defined by:

MinSpeedClamp(RPM) = Slope × MinDutyClamp + MINPWM

Setting MINDTY to 0 disables the function.

MINDTY = 0..127

Maximum Duty Clamp

EEPROM variable DTYMAX defines a duty level at which the motor will change operation from closed-loop curve. The change of operation would depend on MAXDTYOPT setting. If MAXDTYOP = 0, then open-loop operation will result; if MAXDTYOPT = 1, then operation will remain closed loop; however, the speed will be clamped at the value calculated by DTYMAX level.

Four bits are used for this setting at resolution of 1.6% to cover the range 76.5% to 100%.

Maximum Duty (%) = 100 × (511 – MAXDTY × 8) / 511

MAXDTY = 0..15; If MAXDTY = 0 then function is disabled.

Hysteresis is needed to prevent motor from going back and forth between open- and closed-loop mode.

MAXDTYHYS = 0...15

Hys(%) = (MAXDTYHYS + 1) × 0.4

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RD Function

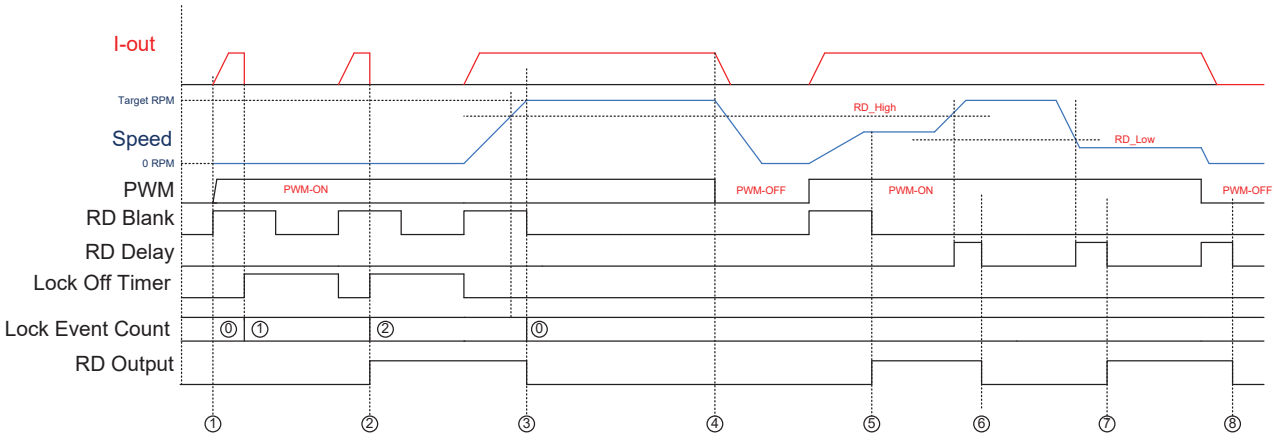
Rotor Detect output RD can be used to indicate that the motor is not running as expected. A high level on RD will indicate a fault.

There are two situations for RD fault:

1. Motor has lock events, enable into lock, or lock while running. There are two different methods for handling lock events, controlled by setting of EEPROM bit LOCKEVT.
2. Motor running at target speed and falls below defined speed thresholds.

   A. Rd signals after RD Delay Timer times out.

Parameter	Range	Resolution	Comment
LOCKEVT	0/1		0 = RD triggered at lock event count of 2 1 = Use RDBLANK for lock events
RD_High (RPM)	0 to 4080 rpm	16 rpm	If set to 0; RD function disabled
RD_Low (RPM)	0 to 4080 rpm	16 rpm	Must be programmed lower than RD_high
RDDLY	0 to 15 seconds	1 second	
RDBLANK	0.1 to 25.4 seconds	100 ms	
T_LOCK_OFF	0.1 to 25.4 seconds	100 ms	



1. Power On with Rotor locked condition
2. Rd is High after 2nd lock event
3. Rd resets Low after RDBLANK if (Speed > RD_high); Lock Event count reset to Zero
4. PWM off – RD is low since normal condition
5. RD is High after RDBLANK if (Speed < RD_High)
6. Rd is Low if (Speed > RD_high) after RDDLY
7. Rd is High if (Speed < RD_Low) after RDDLY
8. PWM off – RD goes low after RDDLY low since normal condition

Figure 6: Rd Timing Diagram (LOCKEVT = 0)

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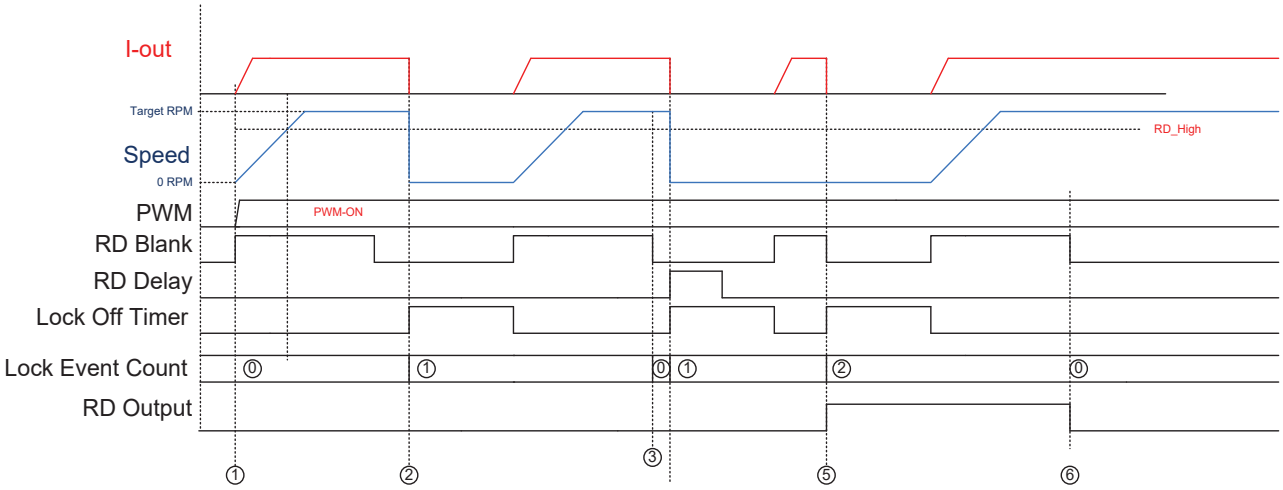

1. Power On with PWM normal Startup
2. Rotor Locked while running – Lock Event counter is One
3. If Speed > RD_high after RDBLANK; Lock Event count reset to Zero
4. Rotor Locked while running – Lock Event counter is One
5. Rd is High after 2nd lock event
6. Rd reset to Low after RD BLANK if (Speed > RD_high); Lock Event count reset to Zero

Figure 7: Rd Timing Diagram (LOCKEVT = 0); lock condition while running

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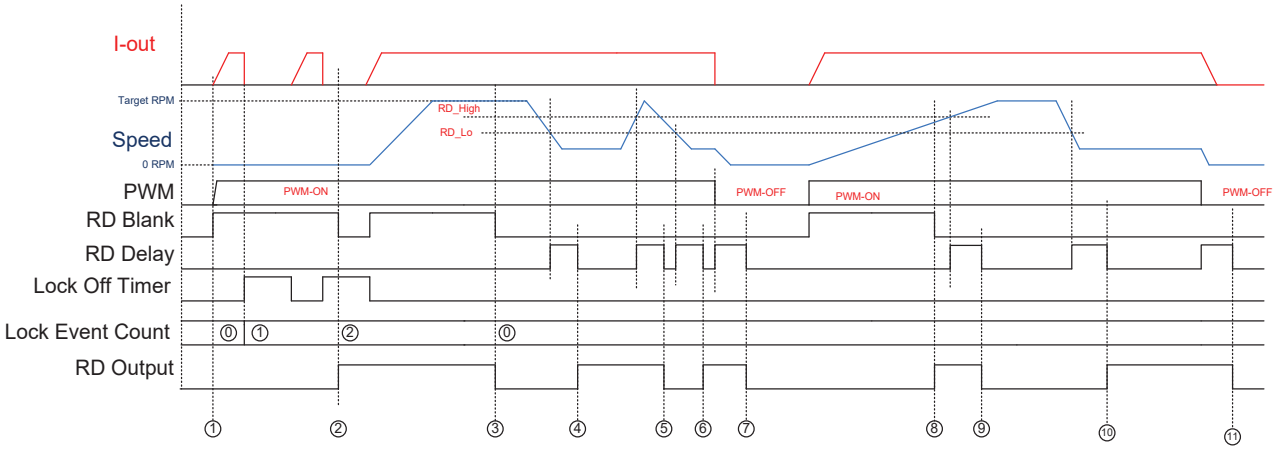

1. Power On with Rotor locked condition
2. Rd is High after RDBLANK if Speed < RD_High
3. Rd resets Low after RDBLANK if (Speed > RD_high)
4. RD changes to HI if speed < RD_low after RDDLY
5. RD changes to LO if speed > RD_high after RDDLY
6. RD changes to HI if speed < Rd_low after RDDLY
7. RD changes to LO when PWM goes off after RDDLY
8. RD changes to HI after RDBLANK is Speed < RD_high (even if > RD_low)
9. RD changes to LO if speed >R_high after RDDLY
10. RD changes to HI if speed < RD_low after RDDLY
11. RD changes to LO when PWM goes off after RDDLY

Note: RDBlank should be programmed longer than the time it takes to accelerate to the RD_high level. Startup time + time to accelerate to RD_high.

Figure 8: Rd Timing Diagram (LOCKEVT = 1)

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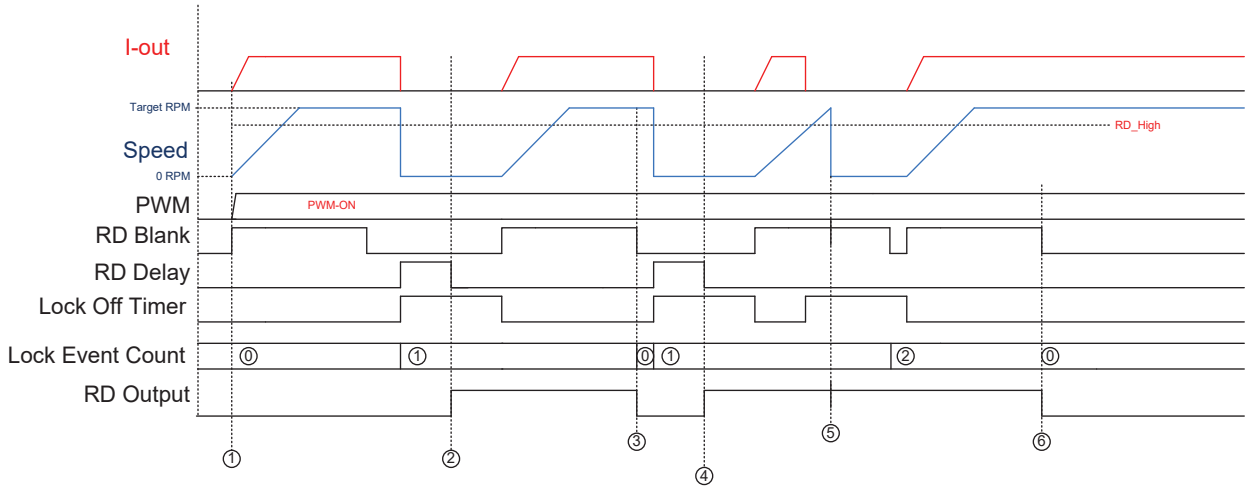

1. Power On with PWM normal Startup
2. Rotor Locked while running – RD changes to HI after RDDLY if Speed < RD_Low
3. RD changes to LO If Speed > RD_high after RDBLANK
4. Rotor Locked while running – RD changes to HI after RDDLY if Speed < RD_Low
5. Rd remains HI, even if speed is OK – since RDBLANK has not timed out
6. Rd reset to Low after RD BLANK if (Speed > RD_high)

Figure 9: Rd Timing Diagram (LOCKEVT = 1) lock condition while running

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EEPROM MAP

Note: refer to application note and user interface for additional detail.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
64	0	15:0	Dev1	Allegro Reserved	n/a
65	1	15:0	Dev1	Allegro Reserved	n/a
66	2	15:0	Dev1	Allegro Reserved	n/a
67	3	15:0	Dev1	Allegro Reserved	n/a
68	4	15:0	Dev1	Allegro Reserved	n/a
69	5	0	DTYIN	0 = Low Freq. < 3.2 kHz 1: High > 2.5 kHz	0x0015
		2:1	REVDMD	0 = 1×, 1 = 1.5×, 2 = 2×, 3 = 2.5×	
		3	FGMSK	0 = Disabled, 1 = Enabled	
		4	FCOLCHK	0 = Enabled, 1 = Disabled	
70	6	15:0	Trim1	Allegro Reserved	n/a
71	7	15:0	Trim2	Allegro Reserved	n/a
72	8	3:0	MAXDTYCLP	Range = 100% to 76.5%, LSB = 1.6%	0x8000
		7:4	MAXDTYHYS	Range = 0 to 5.9%, LSB = 0.4%	
		14:8	MINDTYCLP	Range = 0 to 49.9%, LSB = 0.78%	
		15	CL25	0: Close loop when > target speed, 1: Close Loop at 25% Duty	
73	9	8:0	STRTDMD	LSB = VBBRNG / 511	0xDC26
		15:9	DMDPOST	Range = 0 to 100%, LSB = 0.8%	
74	10	7:0	ALIGNT	Range = 0 to 20.4 seconds, LSB = 100 ms	0xFF06
		15:8	ASLOPE	Range = 160 ms to 40 seconds	
75	11	7:0	STRTF	Range = 0 to 15.94 Hz, LSB = 0.0625 MHz	0xA020
		15:8	ACCEL	Range = 0 to 99.6 Hz/s, LSB = 0.78	
76	12	7:0	ACCELT	Range = 0 to 10.2 seconds, LSB = 40 ms	0x000F
		15:8	MAXOFFDTY	Range = 100% to 76.5%, LSB = 0.4%	
77	13	3:0	DMDRMPAL	Range = 0.9 to 15.3 ms/count, LSB = 0.9	0x6669
		7:4	DMDRMPAH	Range = 0.9 to 15.3 ms/count, LSB = 0.9	
		11:8	DMDRMPDL	Range = 0.9 to 15.3 ms/count, LSB = 0.9	
		15:12	DMDRMPDH	Range = 0.9 to 15.3 ms/count, LSB = 0.9	
78	14	8:0	RESDTY	Range = 0 to 100%, LSB = 0.2%	0x0000
			RESWID	Range = 0 to 50%, LSB = 0.4%	
79	15	7:0	MAXSPD	Maximum Electrical Frequency	0x320C
		15:8	TLOCK	0 to 25.5 seconds	
80	16	7:0	RDLOW	Range = 0 to 4095, LSB = 16 rpm	0x0000
		15:8	RDHIGH	Range = 0 to 4095, LSB = 16 rpm	
81	17	7:0	RDBLK	Range = 0 to 25.5 seconds, LSB = 100 ms	0x0000
		11:8	RDDLY	Range = 0 to 15 seconds, LSB = 1 second	
		15:12	RETRY	Count > 1 = number of lock detect events before disable	
82	18	11:0	PHASLP	Calculated Slope for Linear Phase Advance	0xF0A7
		15:12	SOWLIN	Window Width With Linear Phase Advance	

Continued on next page...

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EEPROM MAP (continued)

Note: refer to application note and user interface for additional detail.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
83	19	0	OCLDIS	0 = Normal, 1 = Disabled	0xA508
		1	OCLOPT	0 = Cycle by cycle, 1 = Reduce demand	
		3:2	PWMF	Motor PWM Selection	
		5:4	BEMFFILT	Bemf comp filter	
		6	TCENB	Temperature Compensation, 0 = Off, 1 = On	
		8:7	WINDM	Windmill Option	
		12:9	SPDCLP	Minimum clamp is speed control mode	
		14:13	PHARNG	0 = >32 krpm, 1 = 16 to 32 krpm, 2 = 8 to 16 krpm, 3 = <8 krpm	
		15	PCDLY	Post Coast delay, 0 = 100 ms, 1 = 500 ms	
84	20	0	CL	Speed Control Mode, 0 = Open Loop, 1 = Closed	0x5111
		1	PHA	Running Mode, 0 = Auto, 1 = Linear Phase Advance	
		2	RDOPT	Rd Function Mode select	
		3	FGRD	Pin Function for FG/RD; 0 = FG, 1 = RD	
		6:4	PP	Pole Pair = PP + 1	
		7	NOCOAST	1 = No Coast, 0 = Coast	
		8	ALIGNMODE	0 = Align, 1 = One Cycle	
		9	QCKSTRT	0 = Disable, 1 = Enable	
		10	RDPWM	0 = No Alarm if PWM off, 1 = Alarm ignores PWM off	
		11	FGSTRT	0 = FG disabled during Startup, 1 = FG Enabled	
		13:12	BEMFHYS	Bemf Hys Level for Startup	
		14	SOWAUTO	Initial Value of Window	
		15	DIR	0 = ACB, 1 = ABC	
85	21	7:0	KP	Closed Loop	0x0210
		15:8	KI	Closed Loop	
86	22	7:0	SLPSWDTY	Duty at which slope changes	0x0000
		11:8	TRAPSWDTY	Duty to switch to trap	
		15:12	PHAOFF	Offset for Linear Phase Advance	
87	23	14:0	SLPSWRPM	Range 0 to 16384, LSB = 1 rpm	0x0000
88	24	13:0	SPDSLP2	Calculated Slope	0x0000
		15:14	Unused		
89	25	0	DUTYINV	0 = Normal, 1 = Invert	0x6102
		1	MAXDTYOPT	0 = Run at Open Loop, 1 = Run at MAXDTYCLP	
		2	ONOFFCNTL	0 = Normal hysteretic on/off, 1 = Off between DC_ON and DC_OFF	
		3	PIOPT	0 = 1×, 1 = 8×	
		4	REVOPT	1 = reverse when duty < DC_OFF and ONOFFCNTL = 1	
		6:5	OCLLEV	OCL Level	
		8:7	ACOCL	AC loss OCL level	
		12:9	DCDISTH	Threshold for DC disable function	
		15:13	TRAPOL	Trapezoidal Overlap Control	

Continued on next page...

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EEPROM MAP (continued)

Note: refer to application note and user interface for additional detail.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
90	26	7:0	TCOAST	Coast time for brake or dir change	0xAF1E
		15:8	OPNLPMAX	Max speed limit for open-loop mode	
91	27	11:0	MINSPD	Minimum Speed (y intercept)	0x07D0
		12	OVPDIS	0 = Normal, 1 = Disable	
		14:13	Unused		
		15	BRKOFF	0 = Coast, 1 = Brake when PWM off state after t_{COAST}	
92	28	13:0	SPDSLP1	Calculated Slope of Speed Curve	0x84E3
		15:14	OCLTOFF	OCL Offtime Select	
93	29	7:0	DCON	Range = 0 to 49.9%, LSB = 0.2%	0x101A
		15:8	DCOFF	Range = 0 to 49.9% LSB = 0.2%	
94	30	5:0	Unused		0x004A
		7:6	BLANK	Blank Time for OCL	
		8	OCPDIS	OCP Disable, 0 = Enabled, 1 = Disabled	
		9	ACLOSS	0 = Disable, 1 = Enable	
		11:10	ACLOSSREL	Duty at which ACLOSS OCL function is released	
		12	ACLOSSOCL	0 = Disable, 1 = Enable	
		13	FCOLOPT	Wait before Data Output	
		14	FCOLCOAST	0 = Normal Drive, 1 = Disable motor during Data output	
		15	FCOLENB	0 = Disable, 1 = Enable	
95	31	15:0	Trim3	Allegro Reserve	n/a
n/a	32-63	15:0	USER	User-defined Memory	0x0000

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Serial Port Control Option

Normally, the IC is controlled by duty cycle input and uses the EEPROM data that is stored to create the speed curve profile. However, it is possible to use direct serial port control to avoid programming EEPROM.

When using direct control, the input duty cycle command is replaced by writing to a 10-bit number to register 165.

Example:

REGADDR[data]: (in decimal)

165[1023] → Duty=100%

165[102] → Duty=102/1023=10%

Upon power-up, the IC defaults to duty cycle input mode. To use serial port mode, the internal registers should be programmed before turning the part on. The sequence to use serial port mode is:

1. Drive FG and PWM pins low**
2. Power up IC
3. Program registers for parameter setting that correspond to each of the EEPROM memory locations.
   A. REGADDR = 64 + EEPROM ADDR.
   B. Program register addresses 65 to 84 corresponding to EEPROM addresses 1 to 20.
   C. It may be helpful to use the GUI text file to help define the hex data for each of the EEPROM addresses.
4. Write to register 165 to start motor.

**Note: If PWM is not driven low before power-up, the motor will try to start immediately as the default high value will demand 100% on signal.

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Serial Port

The A89331 uses standard fast mode I²C serial port format to program the EEPROM or to control the IC speed serially. The PWM pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG may pull the data line low while trying to initialize into serial port mode. Once an I²C command is sent, the PWM input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The A89331 7-bit slave address is 0x55.

I²C Timing Diagrams

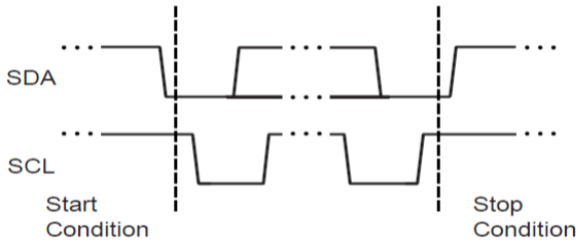

Figure 10: Start and Stop Conditions

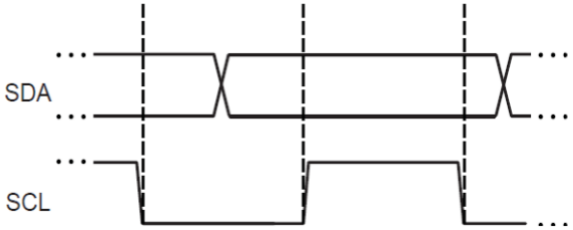

Figure 11: Clock and data bit synchronization

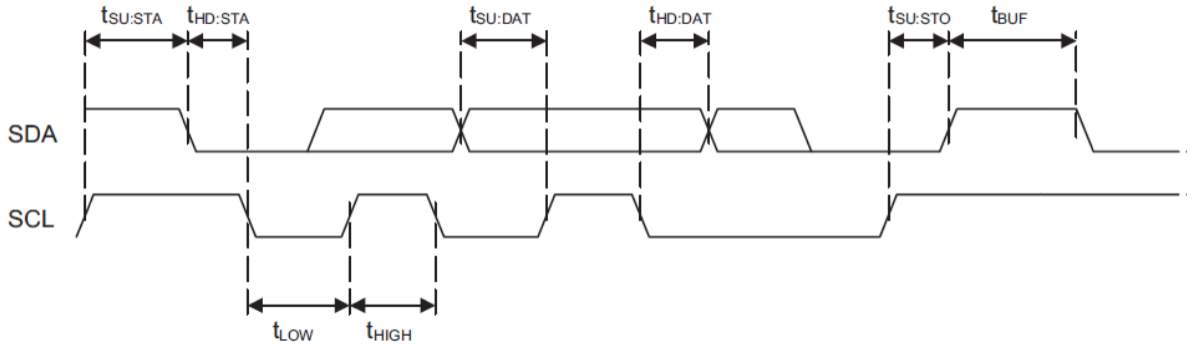

Figure 12: I²C-Compatible Timing Requirements

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Write Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address
4. 2 data bytes, MSB first
5. Stop Condition

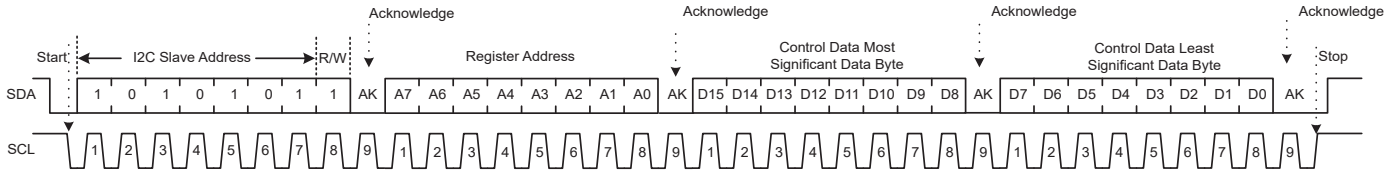

Figure 13: Write Command

Read Command: Two-Step Process

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address to be read
4. Stop Condition
5. Start Condition
6. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 1
7. Read 2 data bytes
8. Stop Condition

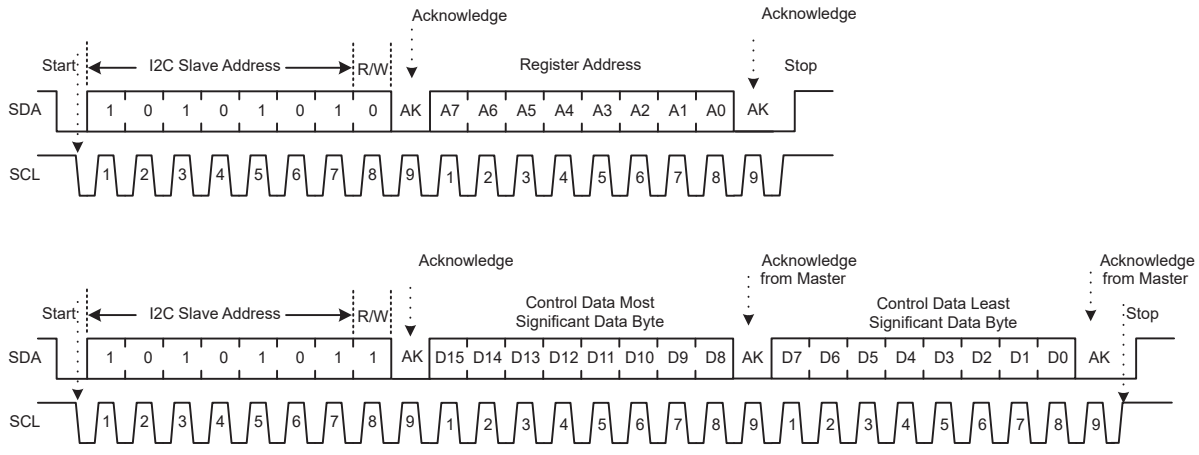

Figure 14: Read Command

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Programming EEPROM

The A89331 contains 63 words of 16-bit length. The EEPROM is controlled with the following I²C registers. Refer to application note for EEPROM definition.

EEPROM Control – Register 161: Used to control programming of EEPROM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM Voltage required for Writing or Erasing
1	ER	Sets Mode to Erase
2	WR	Sets Mode to Write
3	RD	Sets Mode to Read
15:4	n/a	Do not use, always set to zero during programming process

EEPROM Address – Register 162: Used to set the EEPROM address to be altered

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory controlled
15:5	n/a	Do not use always set to zero during programming process

EEPROM DataIn – Register 163: Used to set the EEPROM new data to be programmed

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed

EEPROM DataOUT – Register 164: Used for read operations

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

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There are 3 basic commands, Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 12 ms per word.

Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (hex = 0x0105).

1. Erase the word
   I²C Write REGADDR[Data] ; comment
   A. 162[5] ; set EEPROM address to erase
   B. 163[0] ; set 0000 as Data In
   C. 161[3] ; set control to Erase and Voltage High
   D. Wait 12 ms ; requires 12 ms High Voltage Pulse to Write
2. Write the new data
   A. 162[5] ; set EEPROM address to write
   B. 163[261] ; set Data In = 261
   C. 161[5] ; set control to Write and Set Voltage High
   D. Wait 12 ms ; requires 12 ms High Voltage Pulse to Write

Example #2: Read address 5 to confirm correct data properly programmed.

1. Read the word
   A. 5[i2c read] ; read register 5; this will be contents of EEPROM

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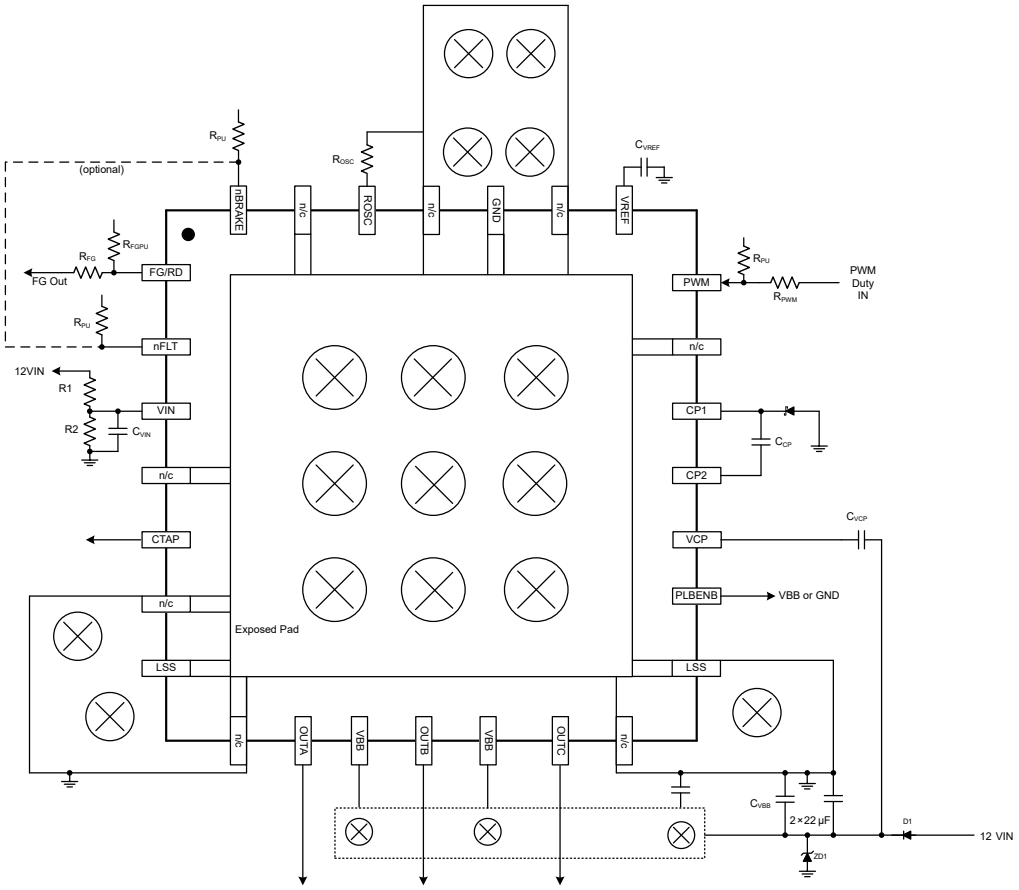
APPLICATION INFORMATION



Name	Suggested	Comment
C_{VREF}	0.22 µF / X5R / 10 V	Ceramic capacitor required
C_{VBB}	22 to 220 µF	Power Supply Stabilization – electrolytic or ceramic
R_{PU}	10 kΩ	Pull-up resistor to VREF
C_{VCP}	0.1 µF	Ceramic capacitor required
C_{CP}	0.1 µF	Ceramic capacitor required
D1	B24013F	Required to isolate motor for reverse polarity protection and power loss brake function
D2	PMEG3002AEL	Schottky diode, V_f < 500 mV @ 100 mA
ZD1	SMBJ14A	TVS to limit max V_{BB} due to transients due to motor generation on power line
R_{FG}, R_{PWM}	500 Ω	Isolate IC pin from noise or overvoltage transients or protect from connector issues
R1	10 kΩ	Required for reverse polarity protection VIN pin
R2	10 kΩ	Pulldown for VIN
C_{VIN}	0.1 µF	Noise filter for hot swap events

Layout Notes

1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VREF} and C_{VBB} as close as possible to IC, connected to GND plane.

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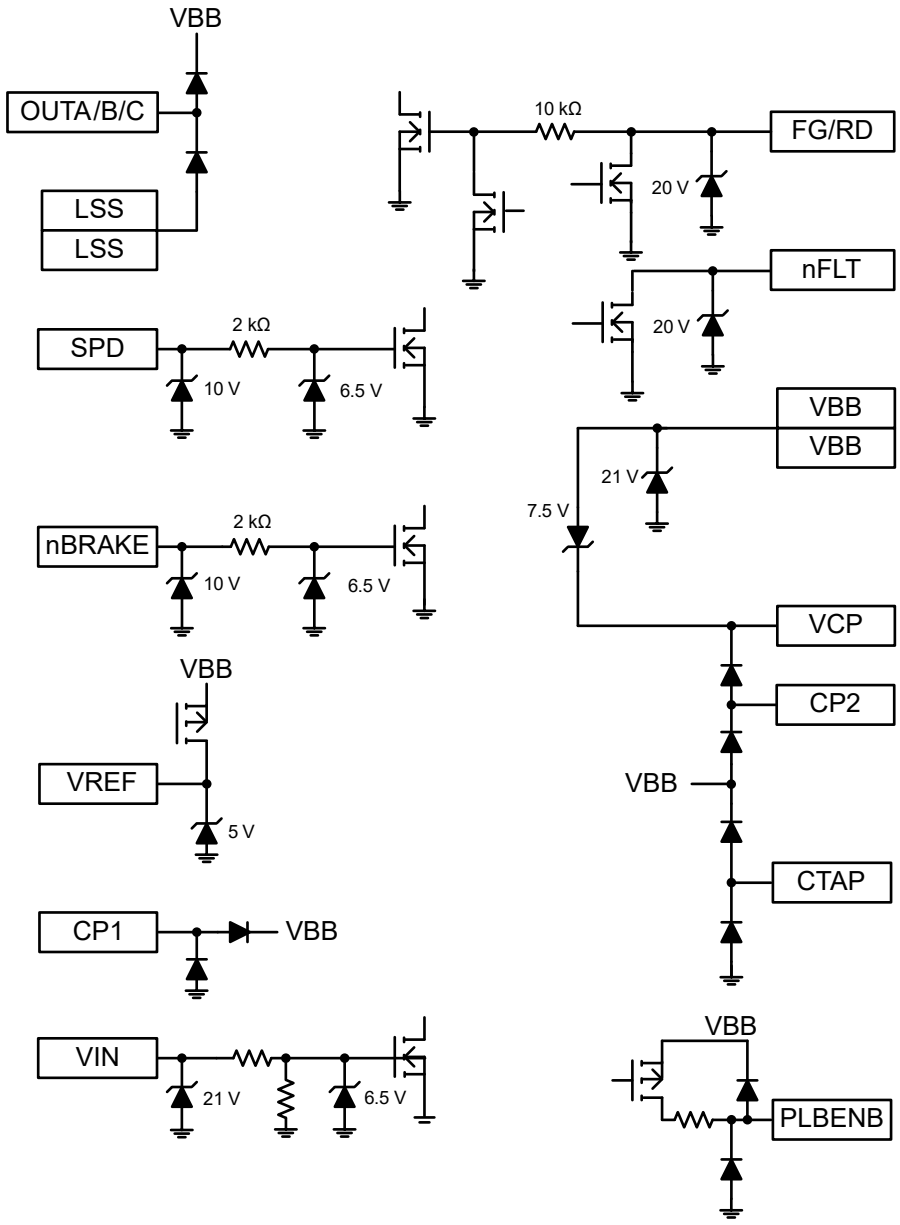
PIN DIAGRAMS



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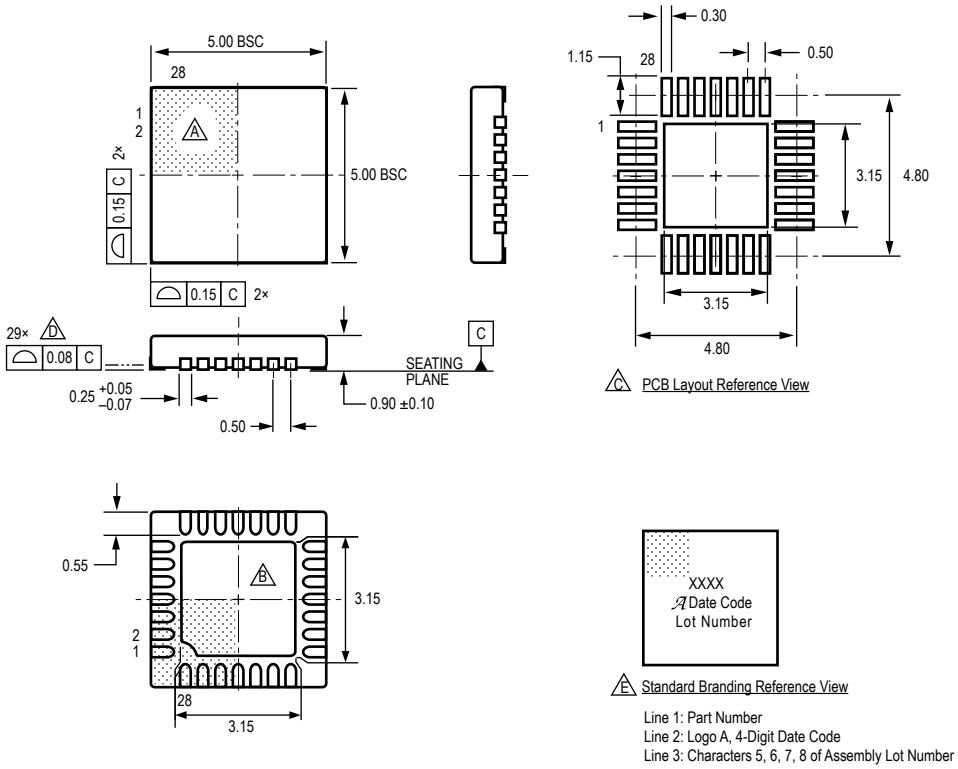
PACKAGE OUTLINE DRAWINGS



For Reference Only; not for tooling use
(reference DWG-0000378, Rev. 3)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 15: ET Package, 28-Pin QFN with Exposed Pad

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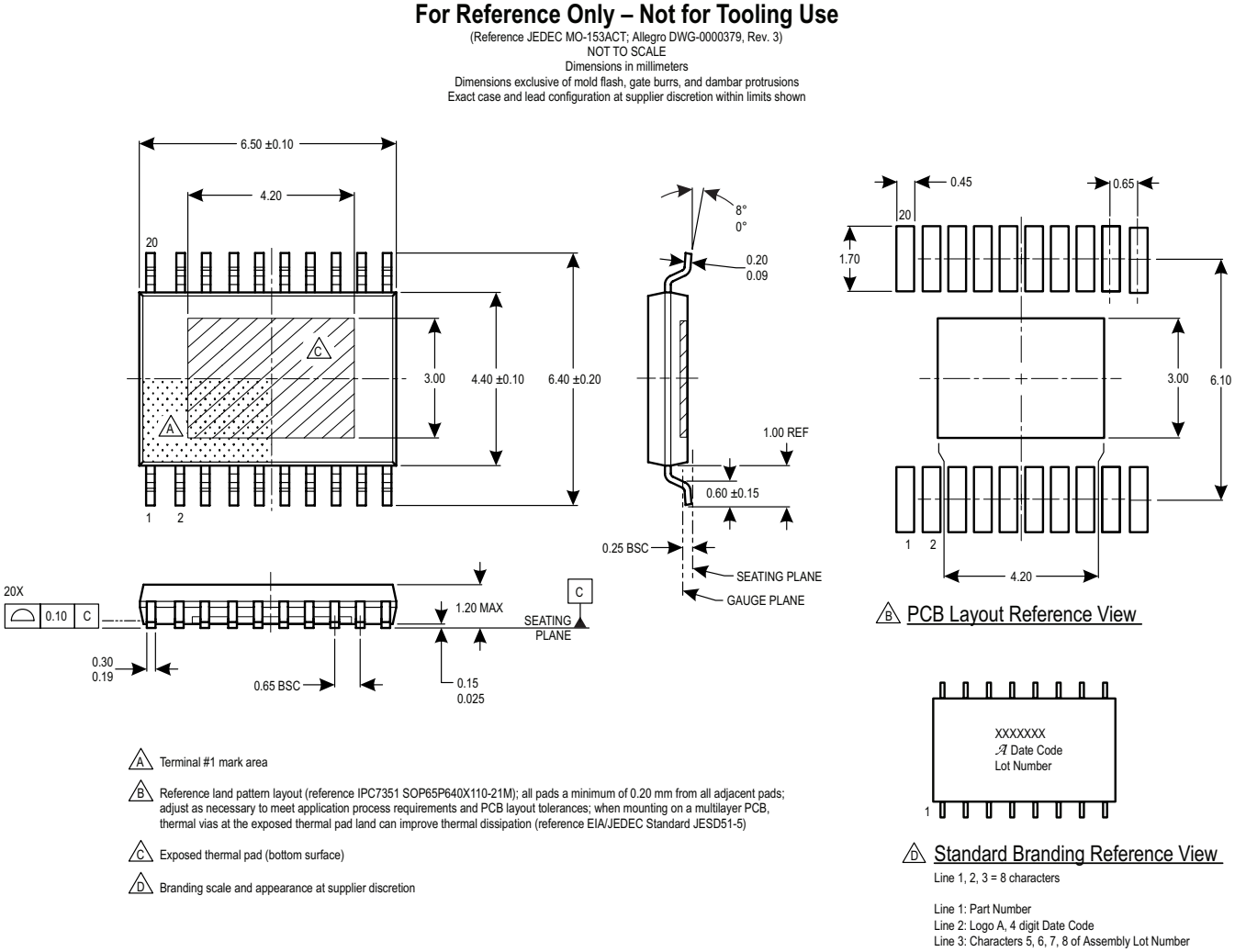

Figure 16: LP Package, 20-Pin TSSOP with Exposed Pad

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Revision History

Number	Date	Description
–	May 20, 2020	Initial release
1	June 8, 2022	Updated package drawings (pages 26-27) and A89331GETSR packing information (page 2)

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