A89332-3

Three-Phase Sensorless Fan Controller

FEATURES AND BENEFITS

- Closed-loop speed control
- Power loss brake
- AC Loss IBB control
- Fault mode brake
- Configurable rotor detect (RD) or frequency generator (FG) output
- Speed curve configuration via EEPROM
- I²C serial port
- Sinusoidal modulation for reduced audible noise and low vibration
- Sensorless (no Hall sensors required)
- Trapezoidal drive option for high speed
- Adjustable gate drive option
- Minimal external components
- PWM duty cycle speed input
- FG speed output
- Lock detection
- Soft start
- Overvoltage protection
- Shorted output protection (OCP)

DESCRIPTION

The A89332-3 three-phase motor controller incorporates a sensorless sinusoidal drive to minimize vibration for high-power, high-speed server fans. Sensorless control eliminates the requirement for Hall sensors for server fan applications.

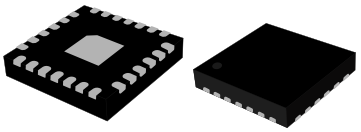
A flexible, closed-loop speed control system is integrated into the IC. An EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

The A89332-3 is available in a 26-contact 4 mm × 4 mm QFN with exposed power pad (suffix EX).

APPLICATIONS

- High-speed 12 V server cooling fans
- Industrial and consumer blowers and fans

PACKAGE



26-Contact QFN with exposed pad (EX package)
Not to scale

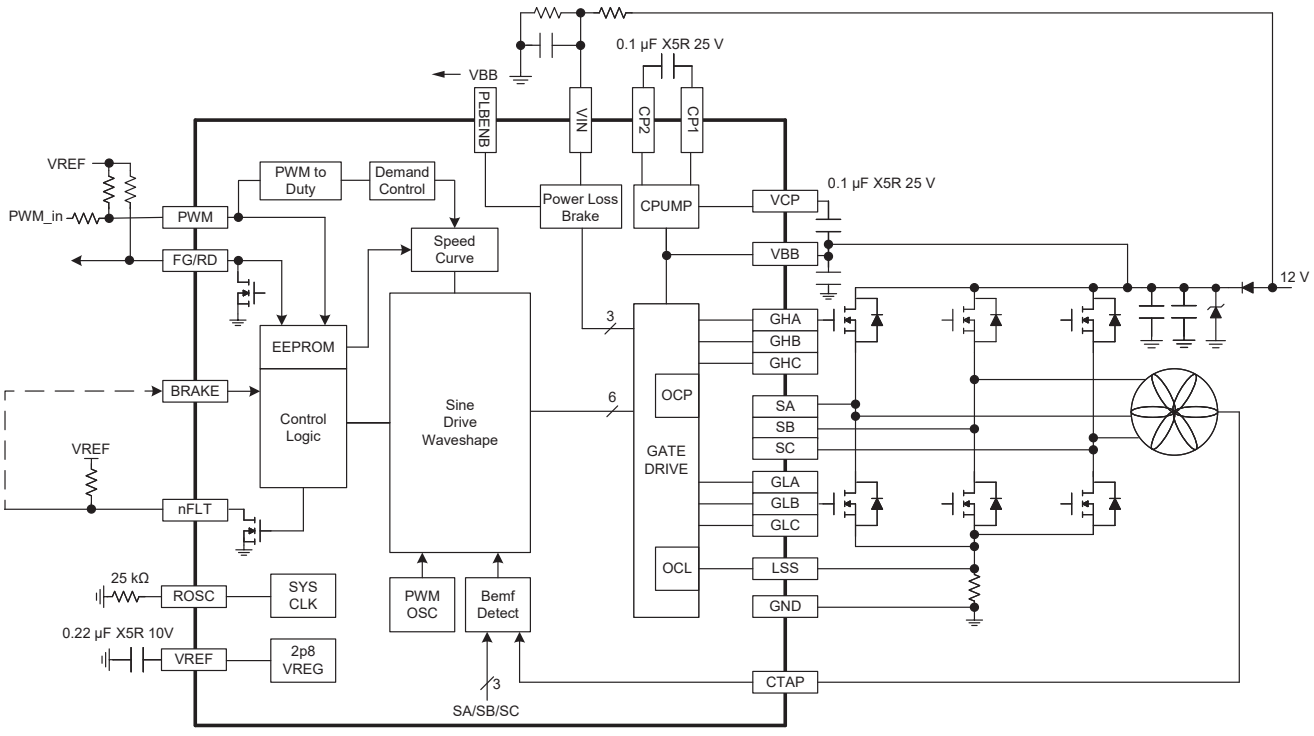


Figure 1: Typical Application

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SPECIFICATIONS

SELECTION GUIDE

Part Number	Package	Packing
A89332BGEXSR-1	26-contact 4 mm × 4 mm QFN with exposed thermal pad	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{BB}		–0.3 to 36	V
Control Input	V_i	VIN, PLBENB	–0.3 to 36	V
Analog Input	V_{ROSC}	ROSC	4	V
Logic Input Voltage Range	V_i	PWM, BRAKE	–0.3 to 6	V
Logic Output	V_O	FG/RD, nFLT (I < 5 mA)	18	V
LSS	V_{LSS}	DC	–500 to 500	mV
		t_w < 500 ns	–4 to 4	V
Output Voltage	V_{OUT}	SA, SB, SC	–2 to V_{BB} + 2	V
CTAP	V_{CTAP}	DC	–0.6 to V_{BB} + 0.6	V
		t_w < 500 ns	–2 to V_{BB} + 2	V
GHx	V_{GH}		V_{Sx} – 0.3 to V_{CP} + 0.3	V
GLx	V_{GL}		V_{LSS} – 0.3 to 8.5	V
VCP	V_{VCP}		V_{BB} – 0.3 to V_{BB} + 8	V
CP1	V_{CP1}		–0.3 to V_{CP} + 0.3	V
CP2	V_{CP2}		V_{BB} – 0.3 to V_{CP} + 0.3	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_S		–55 to 150	°C
Operating Temperature Range	T_A		–40 to 105	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information.

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	26-contact QFN (package EX), on 2-sided PCB with 1 in^2 copper	55	°C/W

*Additional thermal information is available on the Allegro website.

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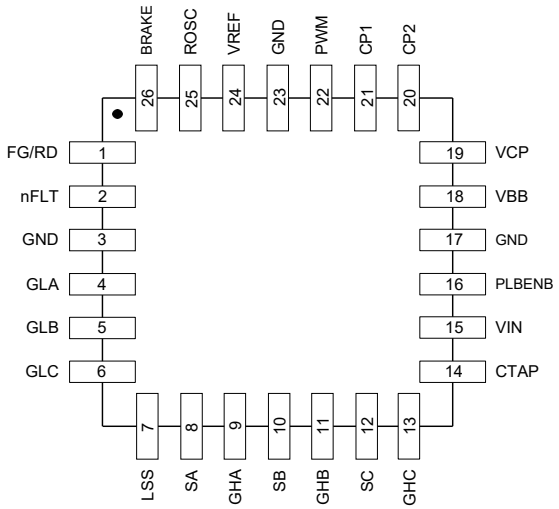
PINOUT DIAGRAM AND TERMINAL LIST TABLE



EX Package

Terminal List Table

Number	Name	Function
1	FG/RD	Logic Output
2	nFLT	Logic Output
3	GND	Ground
4	GLA	Gate Drive Output
5	GLB	Gate Drive Output
6	GLC	Gate Drive Output
7	LSS	Low Side Source
8	SA	Motor Output
9	GHA	Gate Drive Output
10	SB	Motor Output
11	GHB	Gate Drive Output
12	SC	Motor Output
13	GHC	Gate Drive Output

Number	Name	Function
14	CTAP	Motor Common
15	VIN	Analog Input
16	PLBENB	Logic Input
17	GND	Ground
18	VBB	Power Supply
19	VCP	Charge Pump
20	CP2	Charge Pump
21	CP1	Charge Pump
22	PWM	Logic Input
23	GND	Ground
24	VREF	Logic Supply Output
25	ROSC	Analog Input
26	BRAKE	Logic Input

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ELECTRICAL CHARACTERISTICS [1]**:** Valid at T_J = 25°C, V_{BB} = 5 to 18 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	I_{BB}	$V_{IN} > V_{INTH}$, $V_{BB} > V_{BBUVLO}$	–	15.5	18	mA
	I_{BB2}	$V_{BB} = V_{BOOST}$ to 12 V, $V_{IN} < V_{INTH}$	–	0.7	1.3	mA
VREF	V_{REF}	I = 0 to 10 mA	2.75	2.85	2.95	V
VREF Current Limit	V_{REFOCL}	V_{REF} = 0 V	25	–	120	mA
VCP UVLO	V_{CPUVLO}	Falling	3.6	3.95	4.2	V
		Rising	3.95	4.25	4.55	V
GATE DRIVER						
High-Side Gate Drive Output	V_{GH}	V_{BB} = 8 V	6.5	6.8	–	V
Low-Side Gate Drive Output	V_{GL}	V_{BB} = 8 V	7	7.5	–	V
Gate Drive Source Current	I_{SO}	V_{BB} = 8 V, relative to target	–35	–	35	%
Gate Drive Sink Current	I_{SI}	V_{BB} = 8 V, relative to target	–35	–	35	%
SPEED CONTROL						
PWM Duty Input	f_{PWM}		0.1	–	100	kHz
Duty Cycle On Threshold	DC_{ON}	Relative to target	–0.5	–	0.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to target	–0.5	–	0.5	%
Speed Setpoint	f_{SPD}	T_J = 25°C, R_{OSC} = 25 kΩ	–1.5	–	1.5	%
		T_J = –40°C to 125°C, R_{OSC} = 25 kΩ	–2	–	2	%
System Oscillator	f_{OSC}	T_J = 25°C, R_{OSC} = 25 kΩ	–1	–	1	%
		T_J = –40°C to 125°C, R_{OSC} = 25 kΩ	–1.5	–	1.5	%
PROTECTION CIRCUITS						
Lock Protection	t_{OFF}	Relative to target	–4	–	4	%
Overcurrent Limit	I_{OCL}	V_{OCL}= 100 to 250 mV	–5	–	5	%
AC Loss Overcurrent Limit [2]	$I_{OCL\_AC\_Loss}$	Relative to target	–15	–	15	%
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
VREF Undervoltage Lockout	$V_{REFUVLO}$	V_{REF} rising	–	2.63	2.75	V
VREF UVLO Hysteresis	V_{REFHYS}		100	150	200	mV
VBB Overvoltage Threshold	V_{BBOVTH}	Relative to target	–5	–	5	%
VBB Overvoltage Hysteresis	V_{BBOHYS}		–	1.5	–	V
VBB Undervoltage Lockout	V_{BBUVLO}	V_{BB} rising	6.5	6.85	7	V
VBB UVLO Hysteresis	$V_{BBUVLOHYS}$		–	880	–	mV
VIN Logic Threshold	V_{INTH}	V_{IN} falling	–	2.54	–	V
VIN Logic Hysteresis	V_{INHYS}		–	400	–	mV
VIN Pulldown Resistor	V_{INPD}		–	300	–	kΩ
VBB Regulated Boost Voltage	V_{BOOST}	$V_{IN} < V_{INTH}$	4.6	5	5.5	V
VBB Boost Low Threshold	V_{BBTH}		–	1	–	V
Boost Switching Frequency	f_{BOOST}		27	41	56	kHz

[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.
[2] Over temperature range of 0°C to 105°C.

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ELECTRICAL CHARACTERISTICS (cont.) [1]**:** Valid at T_J = 25°C, V_{BB} = 5 to 18 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
LOGIC/INPUT OUTPUT/I²C						
Logic Input Low Level	V_{IL}		0	–	0.8	V
Logic Input High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Logic Input Current	I_{in}	PWM, BRAKE	–10	< 1	10	µA
		PLBENB, V_{IN} = 0 V	–	100	–	µA
Output Saturation Voltage (FG/RD, nFLT)	V_{SAT}	I = 5 mA	–	–	0.3	V
Output Leakage (FG/RD, nFLT)	I_O	V = 16 V, Switch OFF	–	–	5	µA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		8	–	400	kHz
Bus Free Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	ms

[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A89332-3 targets high-speed fan applications to meet the objectives of minimal vibration, high efficiency, and ability to customize the IC to the speed control specification.

In typical systems, a microcontroller unit (MCU) is required to meet each application specification. The A89332-3 integrates the basic closed-loop speed control function, thus allowing elimination of the cost, printed circuit board (PCB) space, and programming requirements of a custom MCU.

For each specific application, the EEPROM settings can be created with the Allegro evaluation board (EVB) and software. To order the custom IC, contact Allegro sales (minimum volume requirements apply).

The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 10-bit number. This “demand” is translated to a speed signal based on settings that are configured via EEPROM.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, overvoltage monitor, and thermal shutdown.

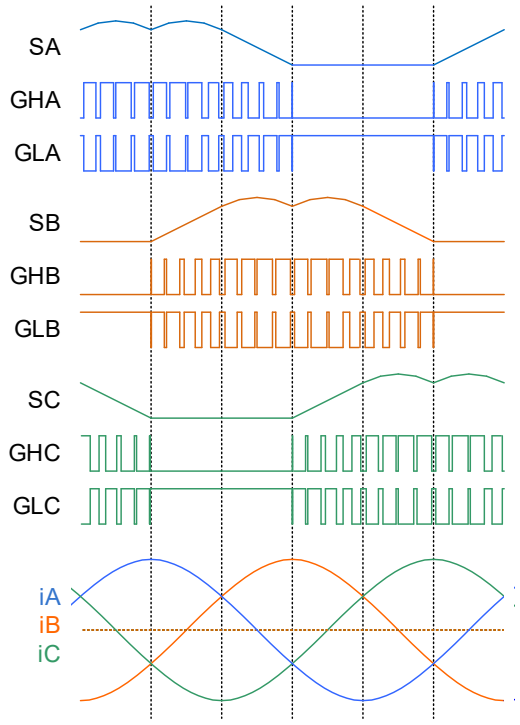

Figure 2: Sinusoidal Drive Sequence for DIR = HI

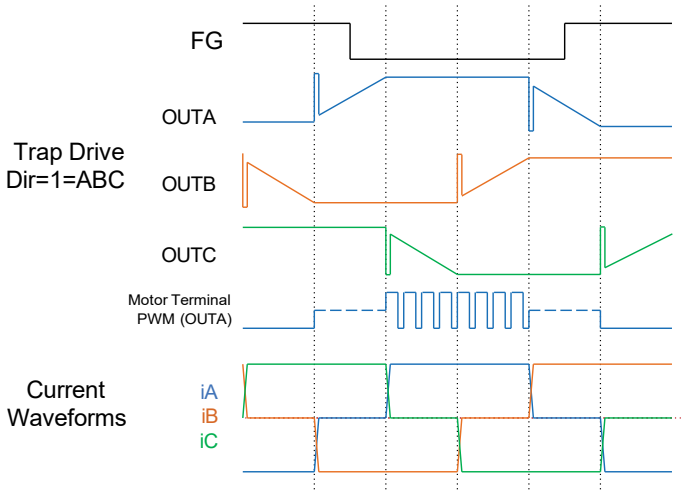

Figure 3: Trapezoidal Drive Sequence for DIR = HI

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FG/RD

Open drain output. Function is determined by selection of the FGRD EEPROM bit, as shown below. The FG/RD pin also serves as the data line (SDA) for I²C communication.

FGRD EEPROM Bit	FG/RD Function
0	FG
1	RD Alarm

PWM

Speed demand input. Duty cycle is measured and translated to target speed request. The PWM pin also serves as the clock line (SCL) for I²C communication.

CTAP

This analog input is an optional connection for motor common (Wye motors). If not used, as in the case of the Delta wound motor, the pin must be left open.

ROSC

System clock reference. Connect 0.1% 25 kΩ resistor between the ROSC pin and the GND pin.

BRAKE

Active low signal; turns on all low sides for braking function. This pin can be used to prevent coast operation during fault conditions. The brake function overrides the speed control input. Brake input is ignored during a thermal shutdown (TSD) event or if ($V_{BB} > V_{BBOVLO}$) or ($V_{BB} < V_{BBUVLO}$). Avoid stress on the MOSFET when braking while the motor is running. During braking, the current will be limited by V_{BEMF}/R_{MOTOR}, where V_{BEMF} is the voltage of the back electromagnetic force and R_{MOTOR} is the resistance of the motor.

PLBENB

Active high control input to enable power loss brake function. Pin should be connected directly to VBB or GND on the PCB. If the PLBENB function is disabled, the motor will coast when power is disconnected.

VIN

Connect to input power supply at connector to the anode of the required power supply blocking diode. This pin will pull down when the power supply is disconnected and will disable driver when the voltage drops to V_{INTH}. A series resistor is needed for reverse polarity protection.

Overvoltage Protection

The A89332-3 will disable the motor outputs when the power supply voltage exceeds V_{BBOVTH}.

OVPSEL	OVPTH (V)
00	20
01	26
10	32
11	disabled

Current Limit

Maximum load current can be set by choice of internal threshold voltage and external sense resistor connected between the LSS terminal and GND. The overcurrent limit function can be disabled by setting the OCLDIS EEPROM bit to 1.

$$I_{LIM} = V_{OCL}/R_{SENSE}$$

OCLTH Code	V_{OCL} (mV)
00	250
01	200
10	150
11	100

OCLOPT	Overcurrent Limit Function
0	Source drivers transition to disabled for fixed t_{OFF} when threshold is reached.
1	Applied duty is reduced when overcurrent threshold is reached.

OCP

Overcurrent protection (OCP) is intended to protect the IC from application conditions of shorted load, motor short to ground, and motor short to battery. The OCP protection monitors the drain to source voltage (VDS) across any source or sink driver when the output is turned on. If the OCP threshold is exceeded for a short blank time, all drivers are shut off. This fault mode can be reset by a PWM ON/OFF cycle or a power cycle.

OCPTH Code	V_{OCLP} (V)
00	0.5
01	0.75
10	1
11	1.5

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nFLT

The following signals will bring output nFLT low:

- V_{BB} undervoltage
- Thermal shutdown
- Charge pump UVLO
- VBB overvoltage
- Output VDS fault (OCP)
- Loss of synchronization

The fault output can be connected to the BRAKEn pin to allow the motor brake mode for the faults shown below.

Fault	Brake i/p	Fault Action	Latched	Readback Reg[Bit]
V_{BB} Under-voltage	X	Disable outputs	N	147[8]
TSD	X	Disable outputs	N	147[6]
V_{BB} Over-voltage	X	Disable outputs	N	147[9]
Charge Pump	H	Disable outputs	N	147[7]
	L	Brake	N	
VDS Fault	H	Disable outputs; latch reset with PWM off/on sequence or power cycle	Y	147[5:0]
	L	Brake	Y	147[5:0]
Loss of Sync	H	Set lock detect timeout—motor coast	N	148[6:0]
	L	Set lock detect timeout—motor brake	N	148[6:0]

Gate Drive

The A89332-3 uses a current source architecture to control the slew rate of the selected power MOSFET. The MOSFET charging and discharging currents are controlled by choice of EEPROM variable GATEDR Output Slew rate can be estimated by the Q_{GD} specification of the MOSFET and the chosen gate drive current, as follows:

$$dt = Q_{GD}/(I_{SRC} \text{ or } I_{SNK})$$

GATEDR Code	I_{SRC}	I_{SNK}
00	15	30
01	30	60
10	50	100

Note: Series gate resistors are not needed for this current source architecture.

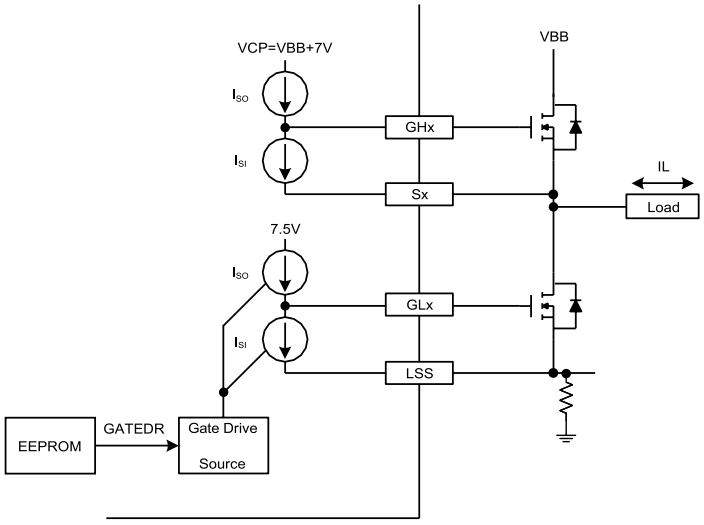

Figure 4: Gate Drive

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Power Loss Brake

If input power is lost to A89332-3, a brake function can be applied to slow the speed of the motor. With a spinning motor, a back electromotive force (BEMF) voltage is generated on motor outputs. This voltage will be rectified by the body diodes on output DMOS devices and the VBB power supply capacitor. If adequate voltage can be stored on the VBB capacitor, then the low side DMOS devices can be turned on to provide braking force to the motor. When the speed of the motor slows, the BEMF voltage is reduced. At some point, there will not be enough voltage on the VBB pin to power the low side drive, so the braking force will not be applied.

The A89332-3 power loss brake circuitry boosts the voltage on the VBB line when the motor is spinning by pulsing the motor windings off. If the motor is rotating, there will be current in the motor winding during the applied brake. This current can be used to charge the VBB line by pulsing off the brake mode for a short time, similar to hysteretic boost converter operation.

There are several modes of operation depending on state of the VBB and VIN pins, as shown below.

Table 1: Power Loss Brake Modes

VIN	PLBENB	V_{BB}	Mode of Operation	Notes
LOW	VBB	< V_{BBTH}	Coast—No Braking	
LOW	VBB	> V_{BBTH} and < V_{BOOST}	Brake PWM	VBB ramps up to VBOOST if the motor is spinning fast enough.
LOW	VBB	V_{BOOST}	Brake—Hysteretic Boost	VBB is regulated by VBOOST.
LOW	VBB	> V_{BOOST}	Brake	VBB decays depending on IBB2 and VBB capacitance.
HIGH	X	< V_{BBUVLO}	Coast—No Braking	Power up or power down.
HIGH	X	> V_{BBUVLO}	Run Mode	VREF powers up logic; motor starts if PWM signal is valid.
LOW	GND	< V_{BBUVLO}	Coast	To disable power loss brake function, connect PLBENB to GND.

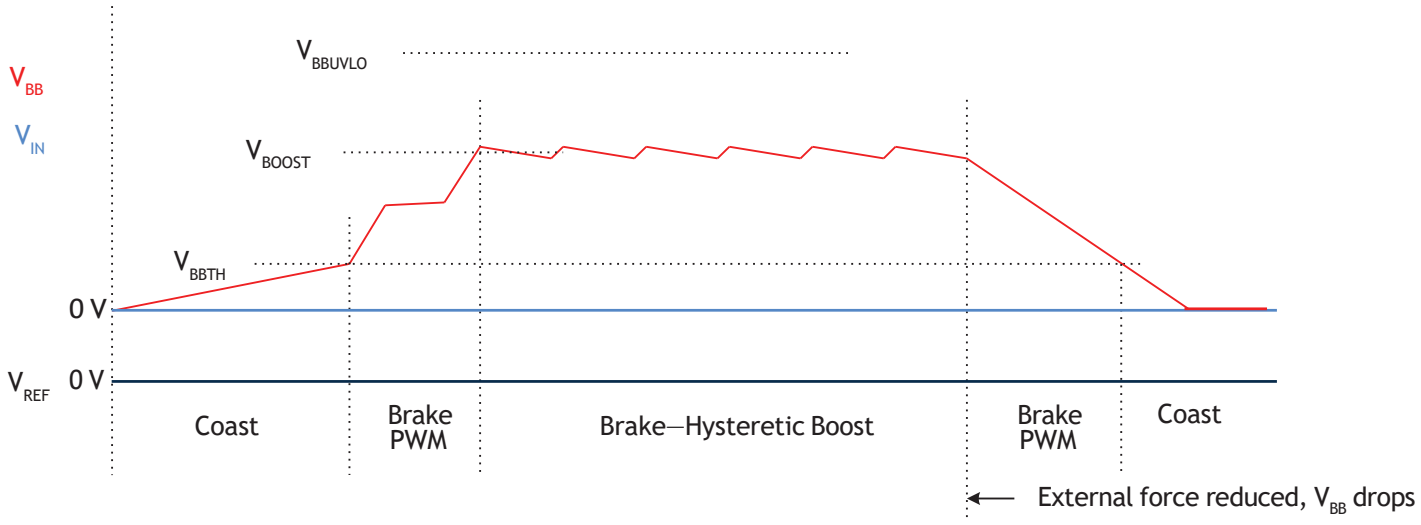

Figure 5: Motor Spinning By External Force—No Power Applied To Fan Module

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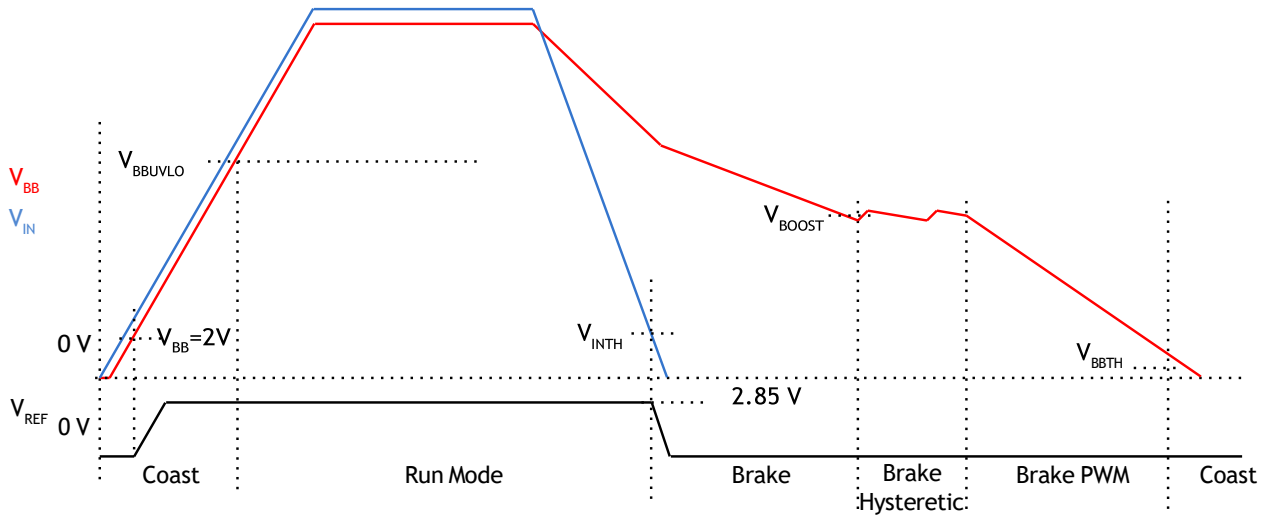


Figure 6: Normal Power Sequence

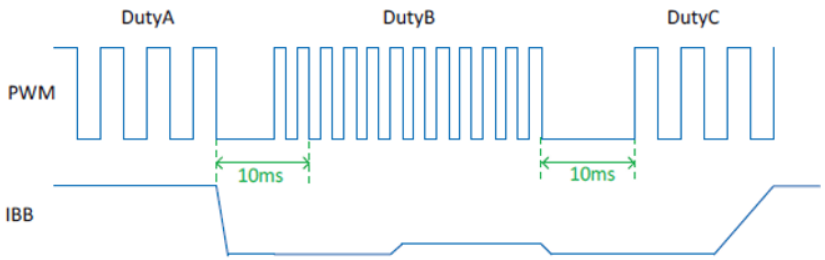
AC Loss Function and AC Loss OCL

With EEPROM option, AC Loss function can be used when system switch to battery power due to the loss of AC main supply and motor is required to operate at much reduced IBB level and at the same time maintains a minimum required speed. The A89332-3 enters AC Loss Mode if PWM input is stuck low for more than 500 µs and it will coast for a programmable coast time followed by windmill restart. In addition, OCL function can be used to limit the IBB current. If enabled, four programmable threshold voltages are available selected through EEPROM for the AC Loss function.

PLS OCL Code	V_{OCL} (mV)
0	75
1	60
2	45
3	30

There are two options for OCL control:

1. OCL is enabled when PWM input is low for more than 6 ms but less than 8 ms, and OCL is released when PWM input is low for more than 10 ms.
2. OCL is enabled when the 500 µs stuck low condition is detected and OCL is released if PWM input duty (DutyB/DutyC) is greater than a selected threshold before 15 seconds timeout or after 15 seconds if DutyB/DutyC is less than the threshold. With option 2, if DutyC is not used and DutyB is less than the threshold, then OCL is released after 15 seconds due to timeout. Refer to application note and user interface for additional detail.



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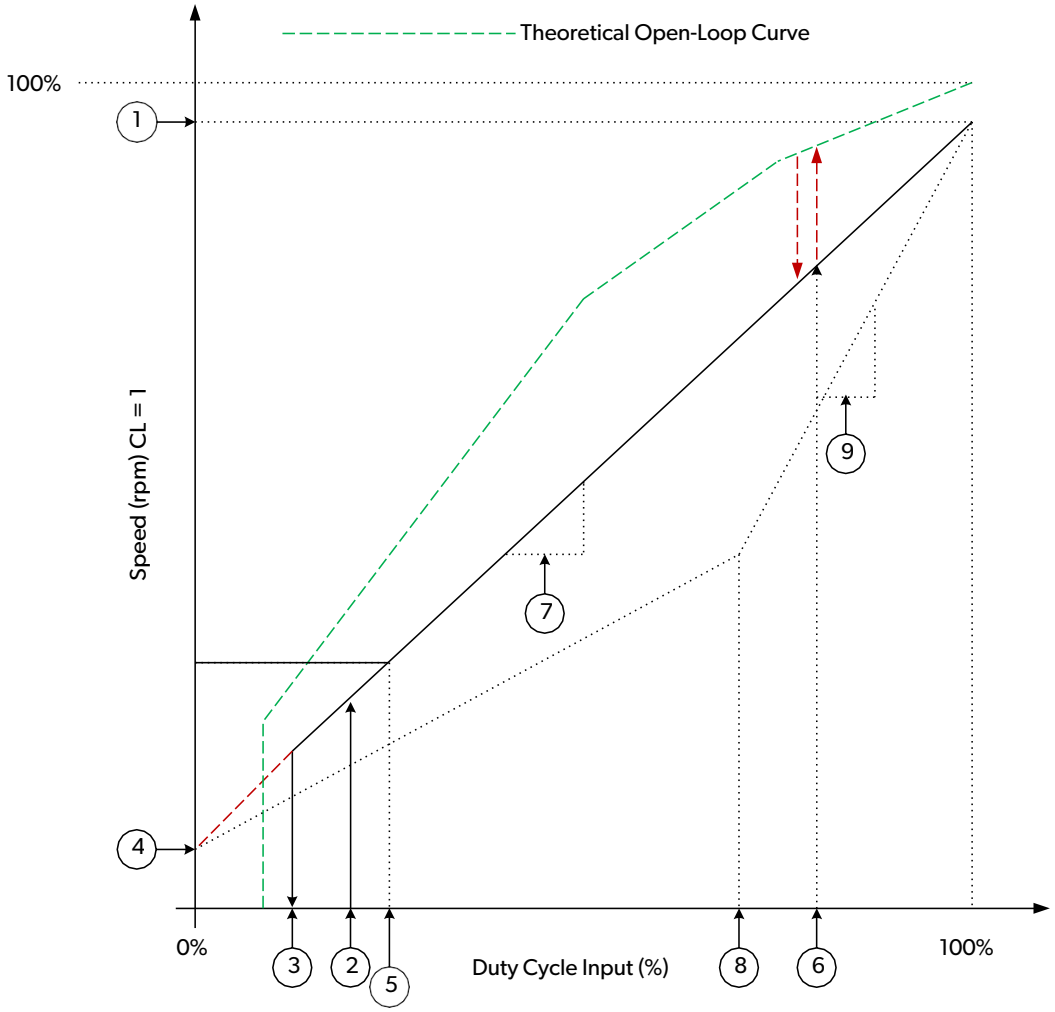
Speed Curve Parameters



1. Maximum speed (calculated from slope of line and offset)
2. Duty on (DCON/511)
3. Duty off (DCOFF/511)
4. MINSPD
5. Min duty clamp
6. Max duty threshold and hysteresis
7. Slope (based on SPDSLP variable)
8. Slope switch duty
9. Slope 2 option

Figure 7: Speed Curve Parameters

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Speed Curve Parameters (continued)

The functions presented in this topic are defined in Figure 7.

Minimum Speed Setpoint

The minimum speed is defined by the value stored in EEPROM variable MINPWM. The resolution is 1 rpm.

MINPWM (RPM) = 0 … 4095

Maximum Speed Setpoint

The A89332-3 calculates the maximum speed based on line equation y = mx + B. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable PWMSLP.

PWMSLP = 64 × (Maximum Speed [rpm] – MINPWM) / 511

Example: Max Speed = 25000, Min Speed = 3000.

PWMSLP = 64 × 22000 / 511 = 2755

where PWMSLP = 0 … 8192.

Motor Speed (rpm) = Slope × DutyIN + MINPWM

where Slope = PWMSLP × 511 / 64, and DutyIN is expressed in %.

Duty In Enable Threshold

EEPROM variable DCON defines the input duty signal that enables the drive. DCON is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

Duty On (%) = 100 × DCON / 511

If DCON is set to 0, the motor will power on with 0% duty cycle input.

Duty In Disable Threshold

EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

Duty Off(%) = DCOFF / 511

DCOFF should always be set to a value lower than DCON.

Duty Cycle Invert

To create a mirror image of the speed curve, set the Duty Cycle Invert bit to 1.

Minimum Duty Clamp

Minimum speed can be clamped to a value to allow the motor to run at the defined low-level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

Min Duty Clamp (%) = 100 × MINDTY / 511

Therefore, the minimum speed will be defined by:

MinSpeedClamp (rpm) = Slope × MinDutyClamp + MINPWM

Setting MINDTY to 0 disables the function.

MINDTY = 0 … 255.

Maximum Duty Clamp

EEPROM variable DTYMAX defines a duty level at which the motor will change operation from the closed-loop curve. The change of operation depends on the MAXDTYOPT setting:

- If MAXDTYOPT = 0, open-loop operation will result.
- If MAXDTYOPT = 1, closed-loop operation will remain. However, the speed will be clamped at the value calculated by the DTYMAX level.

Four bits are used for this setting at a resolution of 1.6% to span the range from 76.5% to 100%.

Maximum Duty (%) = 100 × (511 – MAXDTY × 8) / 511

MAXDTY = 0 … 15; If MAXDTY = 0, the function is disabled.

Hysteresis is needed to prevent the motor from going back and forth between open-loop and closed-loop mode.

MAXDTYHYS = 0 … 15

HYS (%) = (MAXDTYHYS + 1) × 0.4

Speed Feedback Clamp

An EEPROM variable to adjust the deceleration time when switching from forced open back to close-loop speed control. The smaller the clamp value, the longer the deceleration time.

SpeedFeedBack Clamp (rpm) = code × 8,

where code = 0 … 255. If the code is less than 16, the speed feedback clamp is set to the default value of 128.

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Forced Open-Loop Duty Selection

EEPROM-programmable applied duty selection when motor speed is under forced open-loop control.

forcedOpenLpDutySel	Forced Open-Loop Applied Duty
0	External PWM duty (default)
1	90%
2	91%
3	93%
4	95%
5	97%
6	99%
7	100%

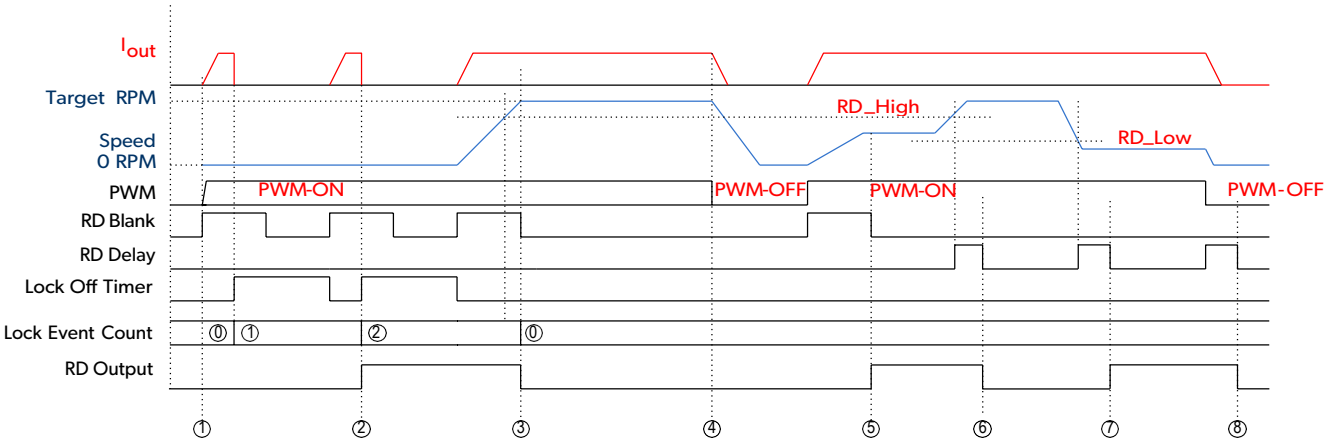
RD Function

The rotor detect (RD) output can be used to indicate the motor is not running as expected. A high level on RD indicates a fault. Possible causes of an RD fault are:

1. Motor lock events, where events are enabled during the lock or events are locked when they should be enabled. There are two methods for handling motor lock events. These methods are controlled by setting of the EEPROM bit LOCKEVT.
2. Motor running at the target speed, then falling below the defined speed threshold. This can result in the RD signaling after the RD Delay Timer times out.

Parameter	Range	Resolution	Comment
LOCKEVT	0/1		0 = RD triggered at lock event count of 2 1 = Use RDBLANK for lock events
RD_High (rpm)	0 to 4080 rpm	16 rpm	If set to 0, RD function disabled
RD_Low (rpm)	0 to 4080 rpm	16 rpm	Must be programmed lower than RD_High
RDDLY	0 to 15 seconds	1 second	
RDBLANK	0.1 to 25.4 seconds	100 ms	
T_LOCK_OFF	0.1 to 25.4 seconds	100 ms	

RD Timing Diagrams



1. Power-on is with the rotor in the locked condition.
2. RD is high after the second lock event.
3. RD resets to low after RDBLANK if Speed > RD_High; Lock event count resets to zero.
4. PWM off—RD remains low after PWM off due to the normal operational state of the motor prior to PWM off.
5. RD is high after RDBLANK if Speed < RD_High.
6. RD is low if Speed > RD_High after RDDLY.
7. RD is high if Speed < RD_Low after RDDLY.
8. PWM off—RD switches to low after RDDLY low.

Figure 8: RD Timing Diagram (LOCKEVT = 0)

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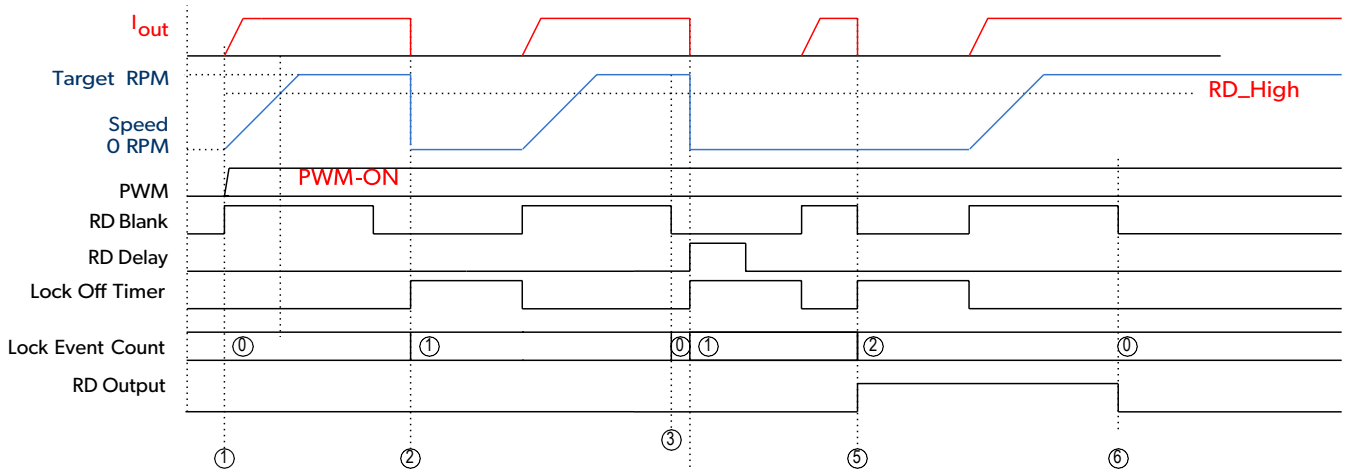
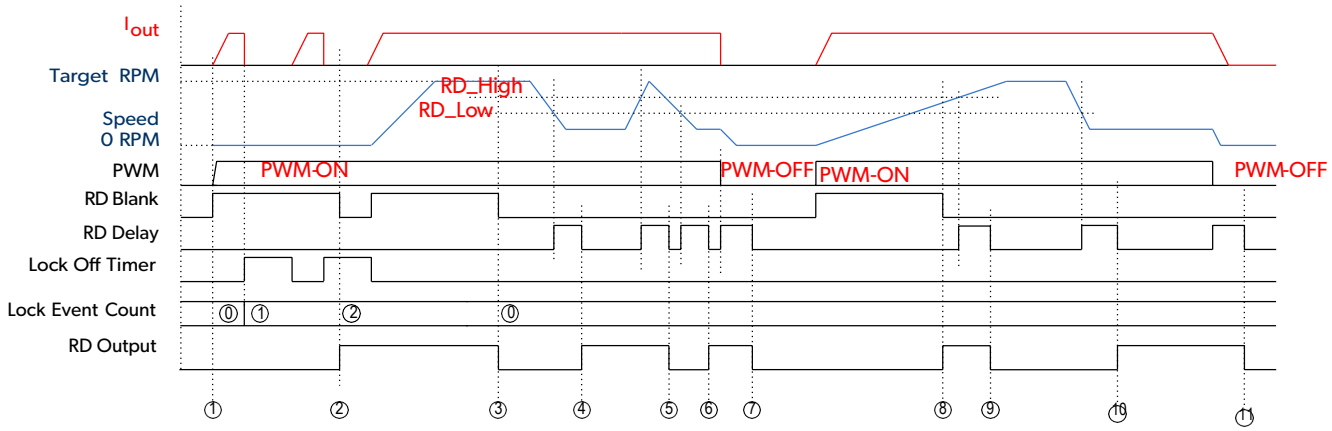


1. Power-on is with PWM normal at startup.
2. Rotor is locked while running; lock event counter is one.
3. Lock event count is reset to zero if Speed > RD_High after RDBLANK.
4. Rotor is locked while running; lock event counter is one.
5. RD is high after the second lock event.
6. RD is reset to low after RD BLANK if Speed > RD_high; lock event count is reset to zero.

Figure 9: RD Timing Diagram (LOCKEVT = 0) of Lock Condition While Running



1. Power-on is with the rotor in the locked condition.
2. RD is high after RDBLANK if Speed < RD_High.
3. RD resets to low after RDBLANK if Speed > RD_High.
4. RD changes to high if Speed < RD_Low after RDDLY.
5. RD changes to low if Speed > RD_High after RDDLY.
6. RD changes to high if Speed < RD_Low after RDDLY.
7. RD changes to low when PWM switches to off after RDDLY.
8. RD changes to high after RDBLANK if Speed < RD_High (even if > RD_Low)
9. RD changes to low if Speed > R_High after RDDLY.
10. RD changes to high if Speed < RD_Low after RDDLY.
11. RD changes to low when PWM switches to off after RDDLY.

Note: RDBlank should be programmed longer than the time is taken to accelerate to the level of RD_High as:

Startup time + time to accelerate to RD_High

Figure 10: RD Timing Diagram (LOCKEVT = 1)

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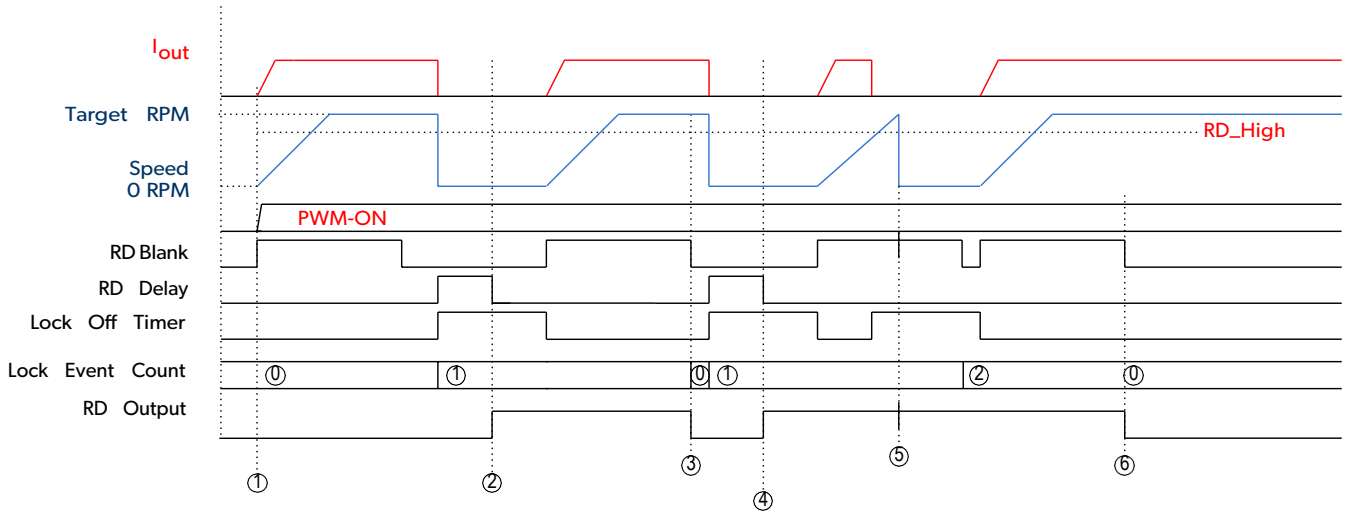

1. Power-on is with PWM normal at startup.
2. Rotor is locked while running—RD changes to high after RDDLY if Speed < RD_Low.
3. RD changes to low If Speed > RD_High after RDBLANK.
4. Rotor is locked while running—RD changes to high after RDDLY if Speed < RD_Low.
5. RD remains high, even if speed is OK; this is because RD-BLANK has not timed out.
6. RD is reset to low after RD BLANK if Speed > RD_High.

Figure 11: RD Timing Diagram (LOCKEVT = 1) lock condition while running

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EEPROM MAP

Note: For additional detail, refer to the application note and user interface.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
64	0	15:0	Dev1	Allegro reserved	–
65	1	15:0	Dev1	Allegro reserved	–
66	2	15:0	Dev1	Allegro reserved	–
67	3	15:0	Dev1	Allegro reserved	–
68	4	15:0	Dev1	Allegro reserved	–
69	5	0	DTYIN	0 = Low frequency < 3.2 kHz; 1 = High frequency > 2.5 kHz	17
		2:1	REVDMD	0 = 1×; 1 = 1.5×; 2 = 2×; 3 = 2.5×	
		3	FGMSK	0 = Disabled; 1 = Enabled	
		4	FCOLCHK	0 = Enabled; 1 = Disabled	
		5	Reserved	–	
		6	FILTRNG	BEMF comparator filter time range selection (default is 0): 0 = Select BEMF filter time range of 4, 8, 12, or 16 µs 1 = Select BEMF filter time range of 1, 2, 3, or 4 µs	
		9:7	FODTYSET	Set applied duty during forced open loop (default is 0): 0 = external applied PWM duty; 1 = 90%; 2 = 91%; 3 = 93%; 4 = 95%; 5 = 97%; 6 = 99%; 7 = 100%	
		15:10	SPDCLAMP	Speed Feedback Clamp for deceleration time adjustment	
70	6	15:0	Trim1	Allegro reserved	–
71	7	15:0	Trim2	Allegro reserved	–
72	8	3:0	MAXDTYCLP	Range = 100% to 76.5%; LSB = 1.6%	8000
		7:4	MAXDTYHYS	Range = 0 to 5.9%; LSB = 0.4%	
		14:8	MINDTYCLP	Range = 0 to 49.9%; LSB = 0.78%	
		15	CL25	0 = Closed loop when > target speed; 1 = Closed loop at 25% duty	
73	9	8:0	STRTDMD	LSB = VBBRNG/511	F81A
		15:9	DMDPOST	Range = 0 to 100%, LSB = 0.8%	
74	10	7:0	ALIGNT	Range = 0 to 20.4 seconds; LSB = 100 ms	FD06
		15:8	ASLOPE	Range = 160 ms to 40 seconds	
75	11	7:0	STRTF	Range = 0 to 15.94 Hz; LSB = 0.0625 mHz	9812
		15:8	ACCEL	Range = 0 to 99.6 Hz/second; LSB = 0.78	
76	12	7:0	ACCELT	Range = 0 to 10.2 seconds; LSB = 40 ms	001B
		15:8	MAXOFFDTY	Range = 100% to 76.5%; LSB = 0.4%	
77	13	3:0	DMDRMPAL	Range = 0.9 to 15.3 ms/count; LSB = 0.9	6669
		7:4	DMDRMPAH	Range = 0.9 to 15.3 ms/count; LSB = 0.9	
		11:8	DMDRMPDL	Range = 0.9 to 15.3 ms/count; LSB = 0.9	
		15:12	DMDRMPDH	Range = 0.9 to 15.3 ms/count; LSB = 0.9	
78	14	8:0	RESDTY	Range = 0 to 100%; LSB = 0.2%	0
		15:9	RESWID	Range = 0 to 50%; LSB = 0.4%	
79	15	7:0	MAXSPD	Maximum electrical frequency	320F
		15:8	TLOCK	0 to 25.5 seconds	

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EEPROM MAP (continued)

Note: For additional detail, refer to the application note and user interface.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
80	16	7:0	RDLOW	Range = 0 to 4095; LSB = 16 rpm	0
		15:8	RDHIGH	Range = 0 to 4095; LSB = 16 rpm	
81	17	7:0	RDBLK	Range = 0 to 25.5 seconds; LSB = 100 ms	0
		11:8	RDDLY	Range = 0 to 15 seconds; LSB = 1 seconds	
		15:12	RETRY	Count > 1 = Number of lock detect events before disable	
82	18	11:0	PHASLP	Calculated slope for linear phase advance	F0B7
		15:12	SOWLIN	Window width with linear phase advance	
83	19	0	OCLDIS	0 = Normal; 1 = Disabled	A509
		1	OCLOPT	0 = Cycle by cycle; 1 = Reduce demand	
		3:2	PWMF	Motor PWM selection	
		5:4	BEMFFILT	BEMF comp filter	
		6	TCENB	Temperature compensation: 0 = Off; 1 = On	
		8:7	WINDM	Windmill option	
		12:9	SPDCLP	Minimum clamp is speed control mode	
		14:13	PHARNG	0 = >32 000 rpm; 1 = 16 000 to 32 000 rpm; 2 = 8 000 to 16 000 rpm; 3 = < 8 000 rpm	
		15	PCDLY	Post coast delay: 0 = 100 ms; 1 = 500 ms	
84	20	0	CL	Speed control mode: 0 = Open loop; 1 = Closed loop	5B11
		1	PHA	Running mode: 0 = Auto; 1 = Linear phase advance	
		2	RDOPT	RD function mode select	
		3	FGRD	Pin function for FG/RD: 0 = FG; 1 = RD	
		6:4	PP	Pole pair = PP + 1	
		7	NOCOAST	1 = No coast; 0 = Coast	
		8	ALIGNMODE	0 = Align; 1 = One cycle	
		9	QCKSTRT	0 = Disable; 1 = Enable	
		10	RDPWM	0 = No alarm if PWM off; 1 = Alarm ignores PWM off	
		11	FGSTRT	0 = FG disabled during startup; 1 = FG enabled	
		13:12	BEMFHYS	BEMF HYS level for startup	
		14	SOWAUTO	Initial value of window	
		15	DIR	0 = ACB; 1 = ABC	
85	21	7:0	KP	Closed loop	210
		15:8	KI	Closed loop	
86	22	7:0	SLPSWDTY	Duty at which the slope changes	0
		11:8	TRAPSWDTY	Duty to switch to trap	
		15:12	PHAOFF	Offset for linear phase advance	
87	23	14:0	SLPSWRPM	Range = 0 to 16 384; LSB = 1 rpm	0
88	24	13:0	SPDSLP2	Calculated slope	8000
		15:14	GATEDRSLEWCTRL	Gate drive source and sink current level selection	

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EEPROM MAP (continued)

Note: For additional detail, refer to the application note and user interface.

I²C REG	EE ADDR	Bits	Name	Description	Default Setting
89	25	0	DUTYINV	0 = Normal; 1 = Invert	6102
		1	MAXDTYOPT	0 = Run at open loop; 1 = Run at MAXDTYCLP	
		2	ONOFFCNTL	0 = Normal hysteretic on/off; 1 = Off between DC_ON and DC_OFF	
		3	PIOPT	0 = 1×; 1 = 8×	
		4	REVOPT	1 = Reverse when duty < DC_OFF and ONOFFCNTL is set to 1	
		6:5	OCLLEV	OCL level	
		8:7	ACOCL	AC Loss OCL level	
		12:9	DCDISTH	Threshold for DC disable function	
		15:13	TRAPOL	Trapezoidal overlap control	
90	26	7:0	TCOAST	Coast time for brake or direction change	AF15
		15:8	OPNLPMAX	Maximum speed limit for open-loop mode	
91	27	11:0	MINSPD	Minimum Speed (y intercept)	320
		13:12	OVPSEL	Overvoltage protection threshold selection	
		14	VBBREF	VBB reference voltage selection	
		15	BRKOFF	0 = Coast, 1 = Brake when PWM off state after t_{COAST}	
92	28	13:0	SPDSLP1	Calculated slope of speed curve	84B0
		15:14	OCLTOFF	OCL offtime select	
93	29	7:0	DCON	Range = 0 to 49.9%; LSB = 0.2%	101A
		15:8	DCOFF	Range = 0 to 49.9%; LSB = 0.2%	
94	30	3:0	DEADT	Range = 240 to 680 ns	000A
		5:4	VDS	Range = 0.5 to 1.5 V	
		7:6	BLANK	Blank Time for OCL	
		8	OCPDIS	OCP Disable: 0 = Enabled, 1 = Disabled	
		9	ACLOSS	0 = Disable, 1 = Enable	
		11:10	ACLOSSREL	Duty at which AC Loss OCL function is released	
		12	ACLOSSOCL	0 = Disable, 1 = Enable	
		13	FCOLOPT	0 = 0.5 seconds wait with preamble, 1 = 2 seconds wait without preamble	
		14	FCOLCOAST	0 = Normal Drive, 1 = Disable motor during Data output	
		15	FCOLENB	0 = Disable, 1 = Enable	
95	31	15:0	Trim3	Allegro reserved	–
–	32 – 63	15:0	USER	User-defined memory	0x0000
	32	15:8	BYTE 0		
		7:0	BYTE 1		
	33 – 62	15:8	BYTE 2,4,6…		
		7:0	BYTE 3,5,7…		
	63	15:8	BYTE 62		
		7:0	CHKSUM	For readback	

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Serial Port Control Option

Normally the IC is controlled by duty cycle input and uses the EEPROM data stored to create the speed curve profile (as show in Figure 7). However, it is possible to use direct serial port control to avoid programming the EEPROM. When using direct control, the input duty cycle command is replaced by writing to a 9-bit number to register 165. For example:

- REGADDR[data]: (in decimal)
- 165[511] → Duty = 100%
- 165[102] → Duty = 102/511 = 20%

Upon power up, the IC defaults to duty cycle input mode. To use serial port mode, program the internal registers before power-on. The sequence to use serial port mode is:

1. Drive the FG and PWM pins low
   Note: If the PWM is not driven low before power-on, the motor will try to start immediately because the default high value will demand a signal that is 100% on.
2. Power-on the IC
3. Program the registers for parameter settings that correspond to each of the EEPROM memory locations:
   A. REGADDR = 64 + EEPROM ADDR.
   B. Program register addresses 65 to 84 corresponding to EEPROM addresses 1 to 20.
   C. It may be helpful to use the GUI text file to help define the hex data for each of the EEPROM addresses.
4. Write to register 165 to start the motor.

**Note: If PWM is not driven low before power up, motor will try to start immediately as the default high value will demand 100% on signal.

Serial Port

The A89332-3 uses standard fast mode I²C serial port format to program the EEPROM or to control the IC speed serially. The PWM pin functions as the clock (SCL) input, and the FG pin functions as the data line (SDA). To begin data transfer, there is no special required sequence. If the motor is running, the FG may pull the data line low while trying to initialize serial port mode. Once an I²C command is sent, the PWM input is ignored, and the motor powers off, much like the response to a PWM duty command of 0%.

The A89332-3 7-bit peripheral device address is 0x55.

I²C Timing Diagrams

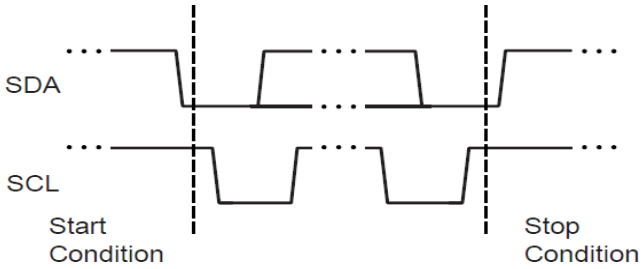

Figure 12: Start and Stop Conditions

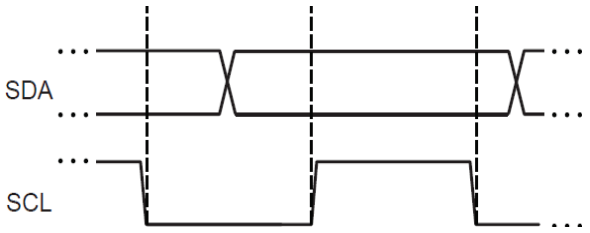

Figure 13: Clock and Data Bit Synchronization

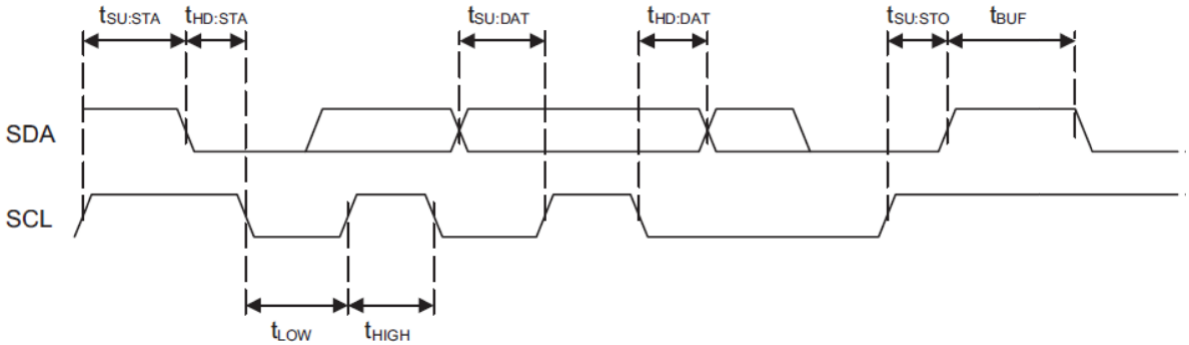

Figure 14: I²C-Compatible Timing Requirements

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WRITE COMMAND

(Refer to Figure 15.)

1. Start condition
2. 7-bit I2C peripheral device address (Device ID) 1010101, R/W bit = 0
3. Internal register address
4. 2 data bytes, MSB first
5. Stop condition

READ COMMAND

(Refer to Figure 16.)

1. Start condition
2. 7-bit I2C peripheral device address (Device ID) 1010101, R/W bit = 0
3. Internal register address to be read
4. Stop condition
5. Start condition
6. 7-bit I2C peripheral device address (Device ID) 1010101, R/W bit = 1
7. Read 2 data bytes
8. Stop condition

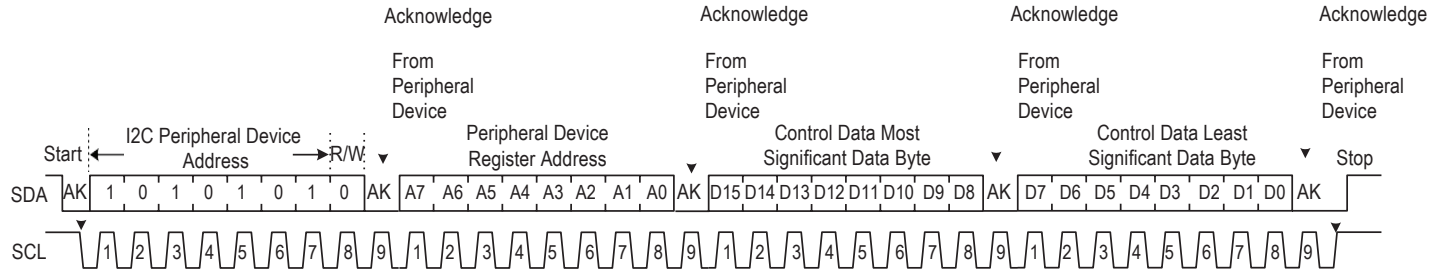

Figure 15: Write Command

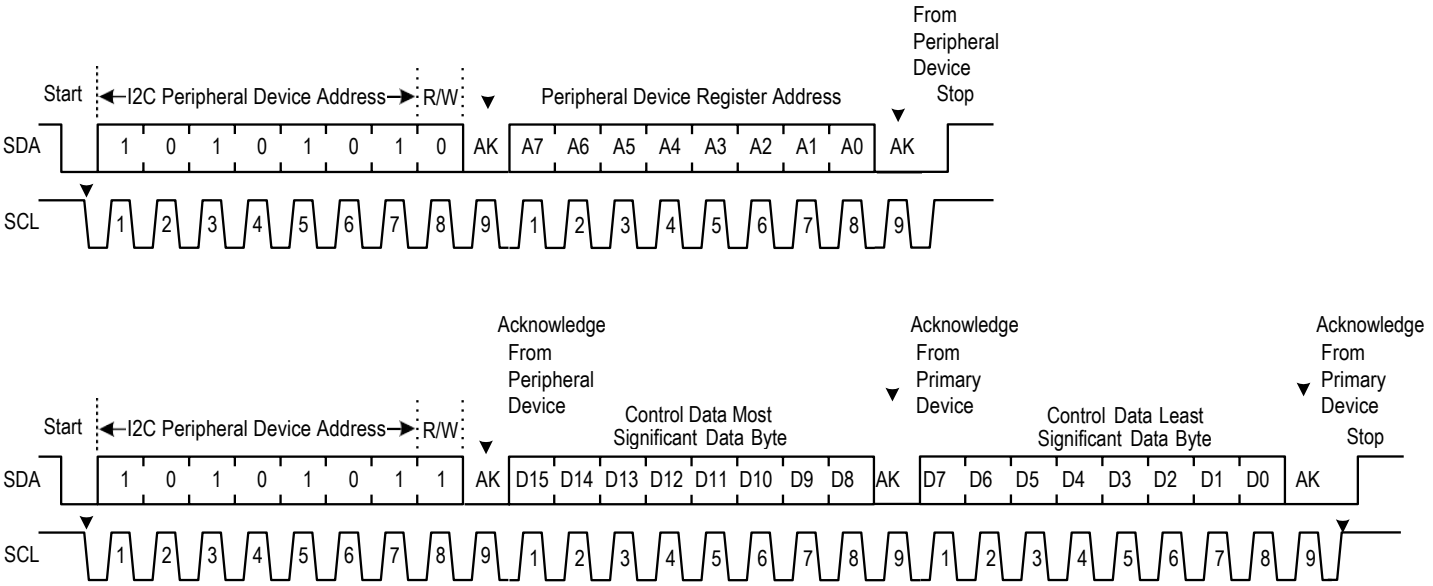

Figure 16: Read Command

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Programming EEPROM

The A89332-3 contains 24 words of 16-bit length. The EEPROM is controlled with the I2C registers shown below. Refer to the application note for EEPROM definition. There are 3 basic commands, Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 15 ms per word. Each word must be written individually.

Example 1: Write EEPROM address 5 to 261 (hex=0x0105)

1. Erase the word
   I2c Write REGADDR[Data]; comment
   A. 162[5]; set EEPROM address to erase
   B. 163[0]; set 0000 as Data In
   C. 161[3]; set control to Erase and Voltage High
   D. Wait 15 ms; requires 15 ms high-voltage pulse to write
2. Write the new data
   A. 162[5]; set EEPROM address to write
   B. 163[261]; set Data In = 261
   C. 161[5]; set control to Write and set Voltage High
   D. Wait 15 ms; requires 15 ms high-voltage pulse to write

Example 2: Read address 5 to confirm correct data are properly programmed.

1. Read the word
   A. 5[i2c read]; read register 5; this will be the contents of the EEPROM

EEPROM Control—Register 161: Used to control programming of EEPROM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Sets EEPROM voltage required for writing or erasing
1	ER	Sets mode to erase
2	WR	Sets mode to write
3	RD	Sets mode to read
15:4	–	Do not use; always set to zero during programming process

EEPROM Address—Register 162: Used to set the EEPROM address to be altered

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory controlled
15:5	–	Do not use; always set to zero during programming process

EEPROM DataIn—Register 163: Used to set the EEPROM new data to be programmed

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed.

EEPROM DataOUT—Register 164: Used for read operations

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

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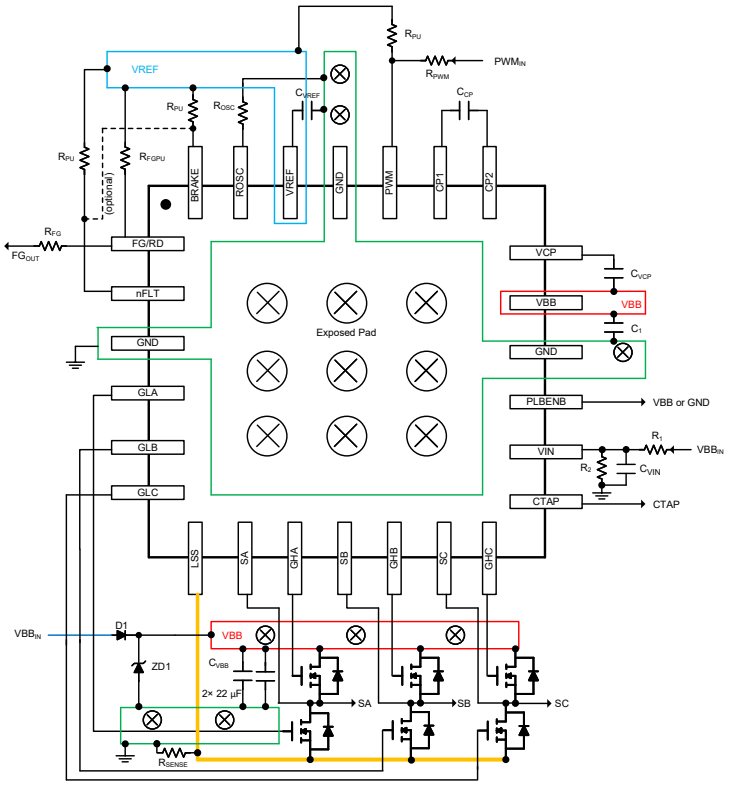
APPLICATION INFORMATION



Name	Suggested	Comment
C_{VREF}	0.22 µF / X5R / 10 V	Ceramic capacitor required
C_{VBB}	20 µF through 220 µF	Power supply stabilization—Electrolytic or ceramic OK
R_{PU}, R_{FGPU}	10 kΩ	Pull up resistors to VREF
C_{VCP}	0.1 µF	Ceramic capacitor required
C_{CP}	0.1 µF	Ceramic capacitor required
C1	0.1 µF	Ceramic capacitor required
D1	MBRS340T3G	Required to isolate motor for reverse polarity protection
ZD1	SMBJ28A	TVS to limit max VBB due to transients due to motor generation on power line Suggested to clamp below 36 V
R_{FG}, R_{PWM}	500 Ω	Isolate IC pins from noise or over voltage transients or protect from connector issues
R1	10 kΩ	Required for reverse polarity protection VIN pin
R2	10 kΩ	Pull down for VIN
C_{VIN}	0.1 µF	Noise filter for hot swap events

Layout Notes

1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VREF} and C1 as close as possible to IC, connected to GND plane.
4. Place C_{CP} and C_{VCP} as close as possible to IC.
5. Place C_{VBB} close to the external FETS VBB power rail.

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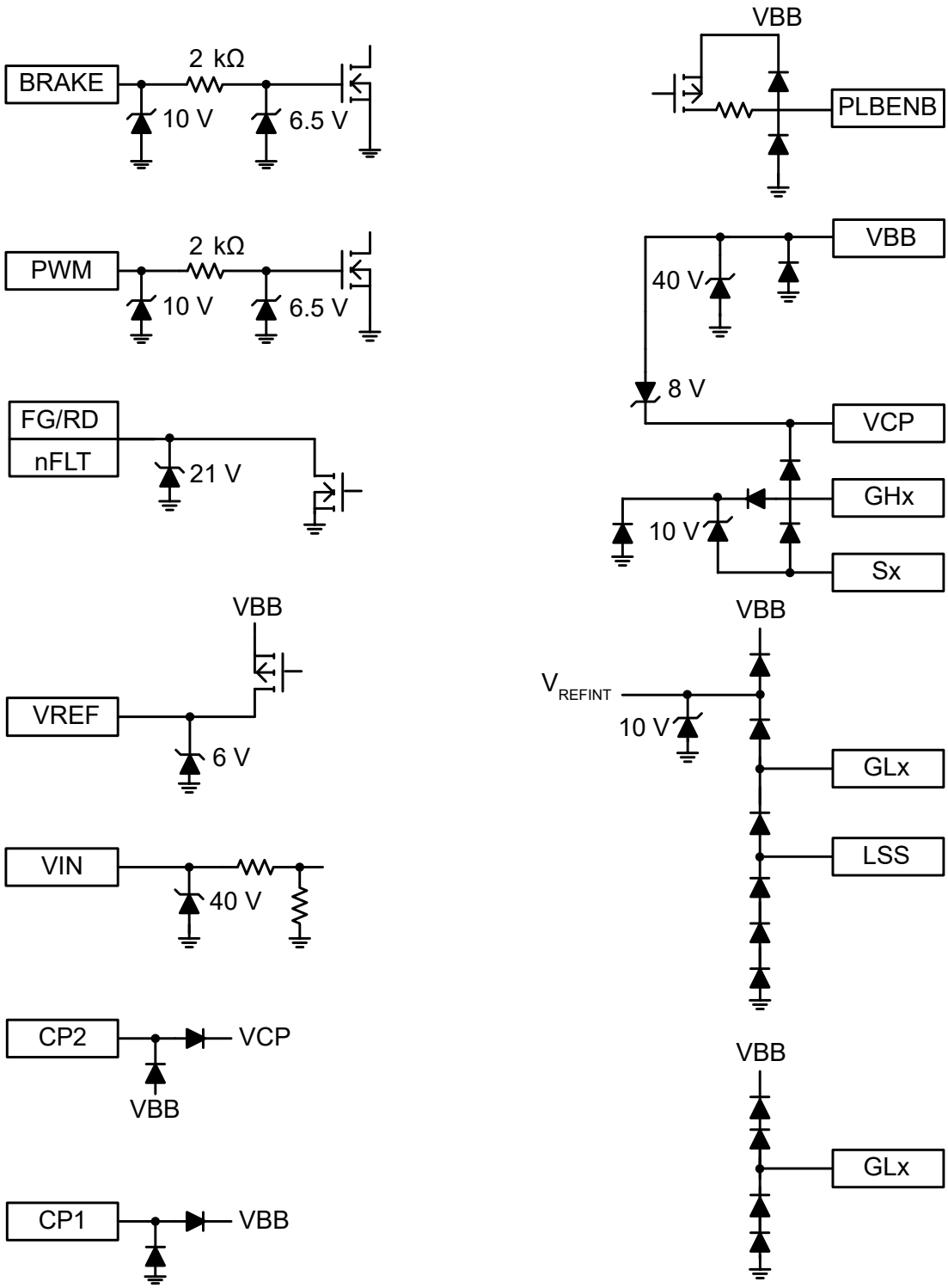
PIN DIAGRAM



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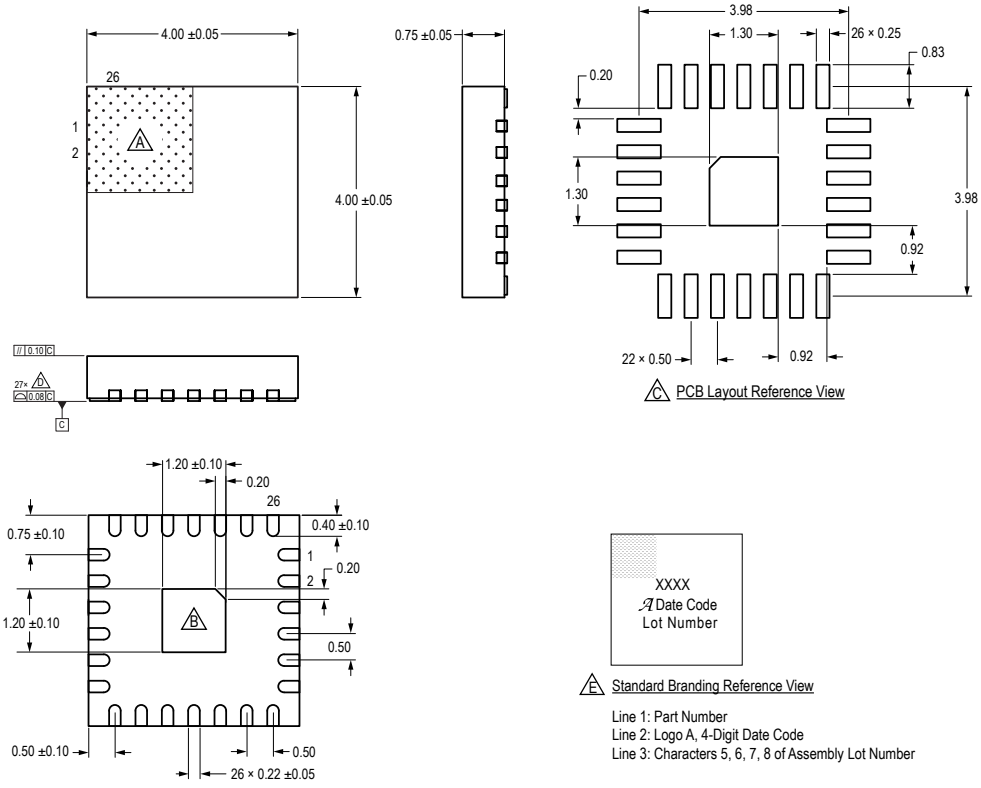
PACKAGE OUTLINE DRAWING



For Reference Only; not for tooling use
(Reference Allegro DWG-0000382, Rev. 2)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout;
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 17: EX Package, 26-Pin QFN with Exposed Pad

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Revision History

Number	Date	Description
–	February 9, 2024	Initial release

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