
A New Microstepping Motor-Driver IC With Integrated Step and Direction Translator Interface

Abstract

A new series of microstepping motor driver integrated circuits with an integrated step and direction translator interface has been developed specifically to drive bipolar stepper motors. These new ICs incorporate several unique design features, including automatic mixed-mode current decay control, PWM current control, synchronous rectification, low $r_{DS(on)}$ power DMOS outputs, full-, half-, quarter-, eighth-, and sixteenth-step operation, HOME output, sleep mode, and an easy-to-implement step and direction interface.

Introduction

Most microstepping motor drivers require control lines for DACs to set the reference for the PWM current regulator and PHASE inputs for current polarity control. In more sophisticated drivers there are also inputs required for the PWM current-control mode to operate in slow, fast, or mixed decay. These control lines can quickly add up to eight to twelve inputs depending on the DAC resolution and have to be supplied by the system microprocessor. The requirement of this many control inputs, and complex sequencing tables in the microprocessor will add to the cost and complexity of the system. The A3977 and A3979 (figure 1), solve this problem with its simple two-line STEP and DIRECTION interface and an efficient DMOS output, all in one IC. For each transition in the STEP input the driver sequences one microstep. This is ideal for applications where a complex microprocessor controller is unavailable or overburdened.

A stepper motor system will have reduced audible noise if the microstepping driver can switch between slow-decay and mixed-decay mode PWM operation. The A3977 and A3979 include circuitry that automatically sets the current

decay mode either slow or mixed decay, which eliminates the need for the user to provide additional control lines.

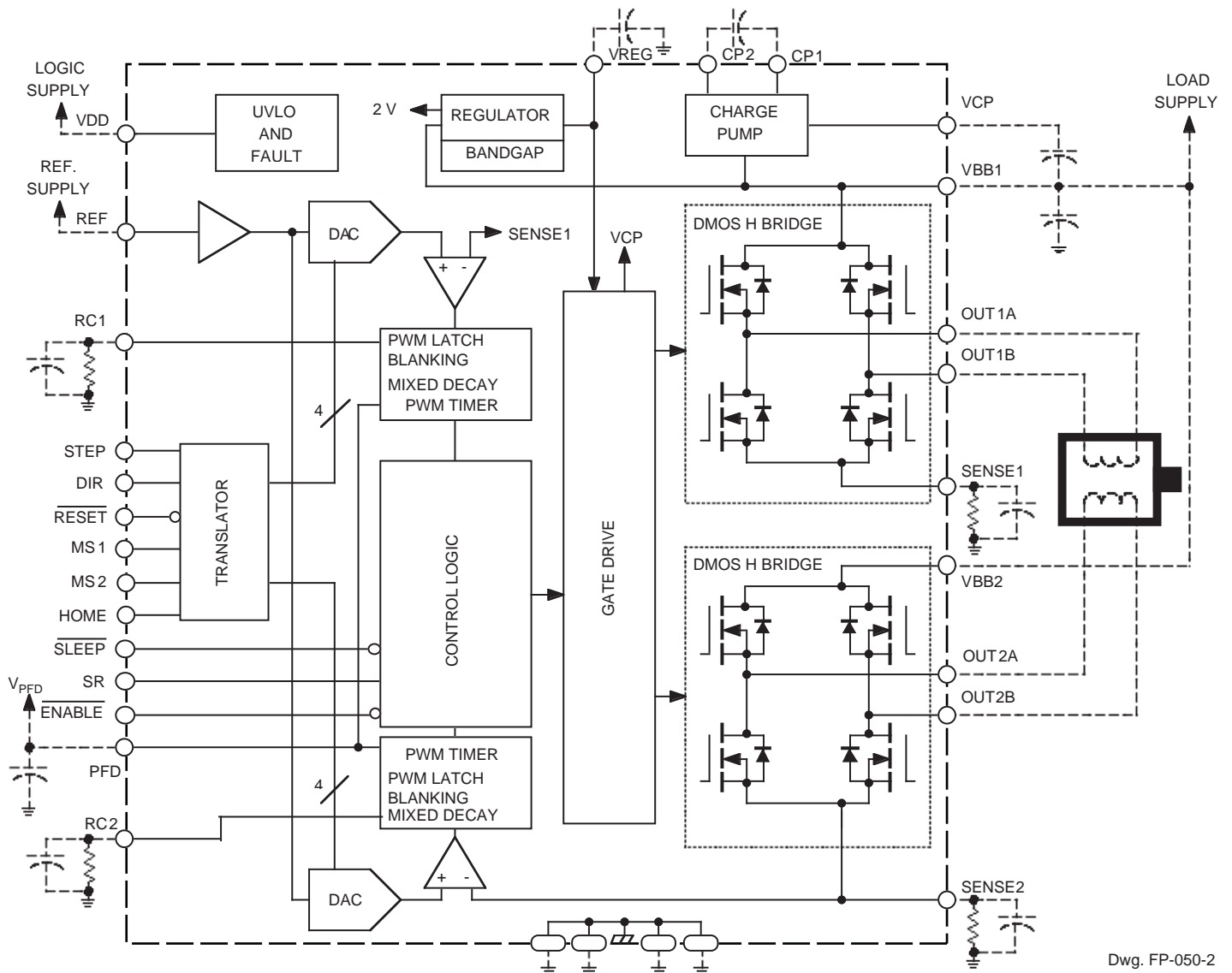
In order to satisfy high-end applications that require low power dissipation, the A3977/79 uses low $r_{DS(on)}$ n-channel power DMOS outputs rated at ± 2.5 A and 35 V. Another benefit of the DMOS outputs is the ability to implement synchronous rectification. The A3977/79 synchronous-rectification control circuitry will turn on the appropriate output DMOS device during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This results in significantly lower power dissipation and eliminates the need for external Schottky diodes in most applications.

The A3977 and A3979 are truly next-generation microstepping motor-driver ICs combining low-power dissipation and high-current outputs, efficient current control, and a simple-to-use interface. These design features and their resulting benefits are discussed in further detail below.

Functional Description

Microstepping Translator The A3977/79 translator converts the STEP and DIRECTION inputs into the control signals required to sequence the current in each of the two H-bridge outputs for full-, half-, quarter-, eighth- (3977 only), and sixteenth-step (3979 only) microstepping operation of a bipolar stepper motor.

At power up or reset the translator sets the DACs and phase current polarity to the initial HOME state conditions and sets the current regulator for both phases to mixed-decay mode (see table 2 and figures 2 through 5 for home-state conditions). When a step command signal (logic Low-to-High transition of the STEP input) occurs the translator automatically sequences the DACs to the next level and current polarity. Table 2 shows the current sequence table for



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Figure 1. A3977 Functional Block Diagram

motor operation (DIRECTION input logic Low). For the reverse operation the DIRECTION input is set to logic High and the translator reverses the sequence through table 2. The DAC outputs are used by the PWM current regulator to set the trip point of the current output of each phase. The (micro)step resolution is set by inputs MS1 and MS2 as shown in table 1.

Table 1

MS1	MS2	Microstepping Resolution
L	L	Full Step (2 phase)
H	L	Half Step
L	H	Quarter Step
H	H	Sixteenth Step (3979)
H	H	Eighth Step (3977)

Internal PWM Current Control Each H-bridge is controlled by a fixed-off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and the current-sense resistor (R_S) as shown in figure 6. When the voltage across R_S equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off either the source drivers (slow-decay mode) or both the source and sink drivers (fast-decay or mixed-decay modes) and the current recirculates as shown in figure 6. During this recirculation the current decreases until the fixed-off time expires. The appropriate output drivers are enabled again, the motor-winding current again increases, and the PWM cycle is repeated.

The maximum value of current limiting is set by the selection of R_S and the voltage at the V_{REF} input with a transconductance function approximated by:

$$I_{TRIPmax} = V_{REF} / (8R_S)$$

The DAC output reduces the V_{REF} output to the current-sense comparator in precise steps (see table 2 for % $I_{TRIPmax}$ at each step).

$$I_{TRIP} = (\% I_{TRIPmax} / 100) \times I_{TRIPmax}$$

The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one shot off-time, t_{off} , is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminals to ground. The off time is approximated by:

$$t_{off} = R_T C_T$$

In addition to the fixed-off time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false over-current detections due to reverse-recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. This blanking feature eliminates the low-pass filter between R_S and the

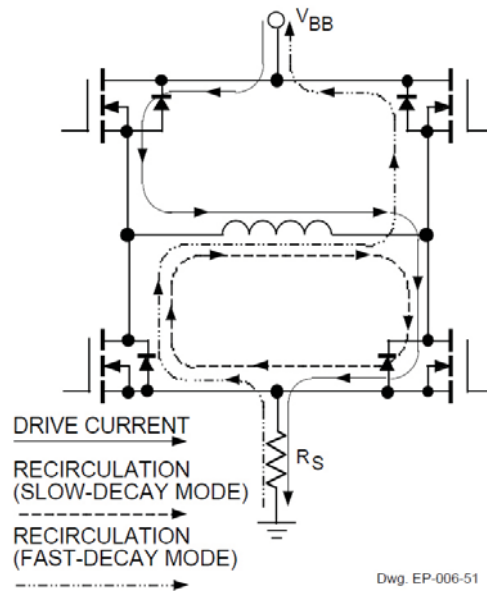


Figure 6. Current Paths

current-sense comparator that is required on most PWM-current regulators. The blank time, t_{BLANK} , can be approximated by:

$$t_{BLANK} = 1900 C_T$$

Mixed-Decay Operation Automatic mixed decay is a key feature of the A3977/79. Automatic mixed-decay operation optimizes the current chopping mode in order to achieve the best sinusoidal current waveform for microstepping.

Slow decay (figure 7) has the advantage of minimum current ripple. However, when microstepping at higher step rates, slow-decay chopping may fail to properly regulate current on the falling slope of the sine wave when current is decreasing. This is a result of motor BEMF overriding the voltage applied to the motor, forcing the current to increase during the decay period. Figure 8 is a scope plot of motor current that illustrates the limitations of slow-decay chopping. This distortion in the current will cause increased audible noise in the motor.

Table 2. Step Sequencing

Home microstep position at Step Angle 45°; DIR = H; 360° = 4 full steps

Full Step #	1/2 Step #	1/4 Step #	(A3977 only) 1/8 Step #	(A3979 only) 1/16 Step #	Phase 1 Current [% I _{tripmax}] (%)	Phase 2 Current [% I _{tripmax}] (%)	Step Angle (°)	Full Step #	1/2 Step #	1/4 Step #	(A3977 only) 1/8 Step #	(A3979 only) 1/16 Step #	Phase 1 Current [% I _{tripmax}] (%)	Phase 2 Current [% I _{tripmax}] (%)	Step Angle (°)
	1	1	1	1	100.00	0.00	0.0		5	9	17	33	-100.00	0.00	180.0
				2	99.52	9.80	5.6					34	-99.52	-9.80	185.6
			2	3	98.08	19.51	11.3				18	35	-98.08	-19.51	191.3
				4	95.69	29.03	16.9					36	-95.69	-29.03	196.9
		2	3	5	92.39	38.27	22.5			10	19	37	-92.39	-38.27	202.5
				6	88.19	47.14	28.1					38	-88.19	-47.14	208.1
			4	7	83.15	55.56	33.8				20	39	-83.15	-55.56	213.8
				8	77.30	63.44	39.4					40	-77.30	-63.44	219.4
1	2	3	5	9	70.71	70.71	45.0	3	6	11	21	41	-70.71	-70.71	225.0
				10	63.44	77.30	50.6					42	-63.44	-77.30	230.6
			6	11	55.56	83.15	56.3				22	43	-55.56	-83.15	236.3
				12	47.14	88.19	61.9					44	-47.14	-88.19	241.9
		4	7	13	38.27	92.39	67.5			12	23	45	-38.27	-92.39	247.5
				14	29.03	95.69	73.1					46	-29.03	-95.69	253.1
			8	15	19.51	98.08	78.8				24	47	-19.51	-98.08	258.8
				16	9.80	99.52	84.4					48	-9.80	-99.52	264.4
	3	5	9	17	0.00	100.00	90.0		7	13	25	49	0.00	-100.00	270.0
				18	-9.80	99.52	95.6					50	9.80	-99.52	275.6
			10	19	-19.51	98.08	101.3				26	51	19.51	-98.08	281.3
				20	-29.03	95.69	106.9					52	29.03	-95.69	286.9
		6	11	21	-38.27	92.39	112.5			14	27	53	38.27	-92.39	292.5
				22	-47.14	88.19	118.1					54	47.14	-88.19	298.1
			12	23	-55.56	83.15	123.8				28	55	55.56	-83.15	303.8
				24	-63.44	77.30	129.4					56	63.44	-77.30	309.4
2	4	7	13	25	-70.71	70.71	135.0	4	8	15	29	57	70.71	-70.71	315.0
				26	-77.30	63.44	140.6					58	77.30	-63.44	320.6
			14	27	-83.15	55.56	146.3				30	59	83.15	-55.56	326.3
				28	-88.19	47.14	151.9					60	88.19	-47.14	331.9
		8	15	29	-92.39	38.27	157.5			16	31	61	92.39	-38.27	337.5
				30	-95.69	29.03	163.1					62	95.69	-29.03	343.1
			16	31	-98.08	19.51	168.8				32	63	98.08	-19.51	348.8
				32	-99.52	9.80	174.4					64	99.52	-9.80	354.4

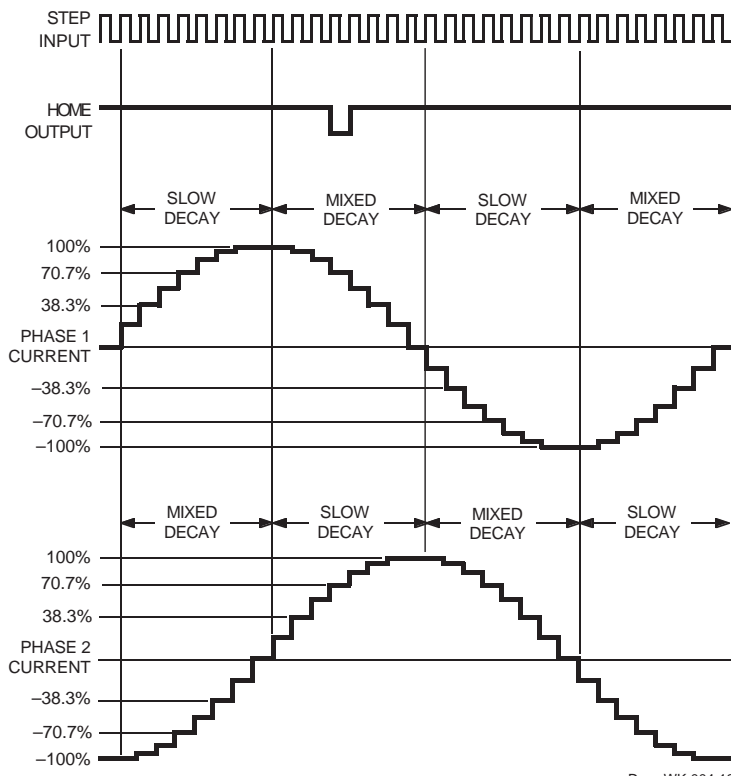


Figure 2. A3977 Eighth-Step (Microstepping) Operation

$$MS_1 = MS_2 = H, DIR = H$$

NOTE – Refer to table 2 for complete phase current level at each step.

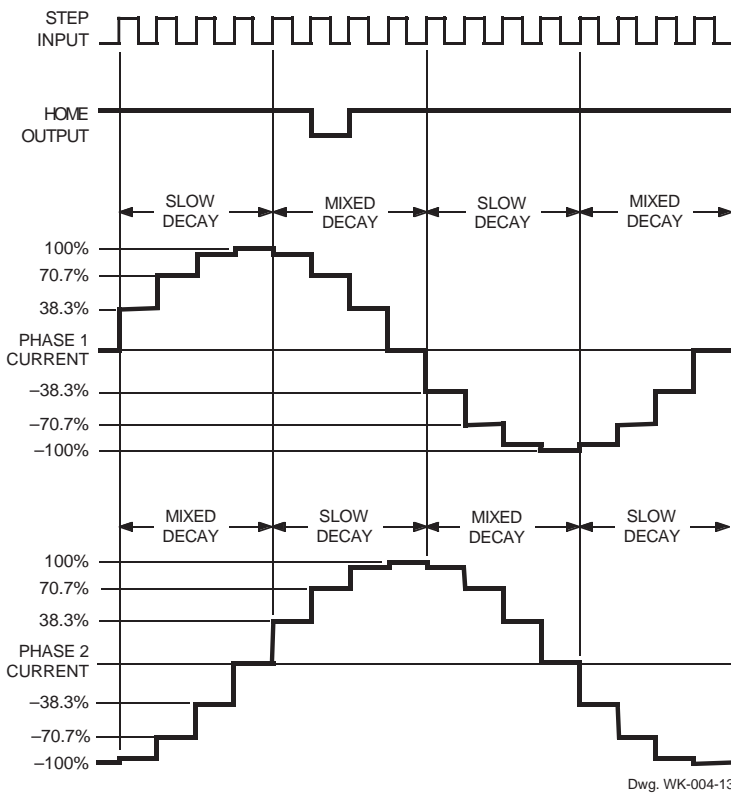


Figure 3. A3977 Quarter-Step Operation

$$MS_1 = L, MS_2 = H, DIR = H$$

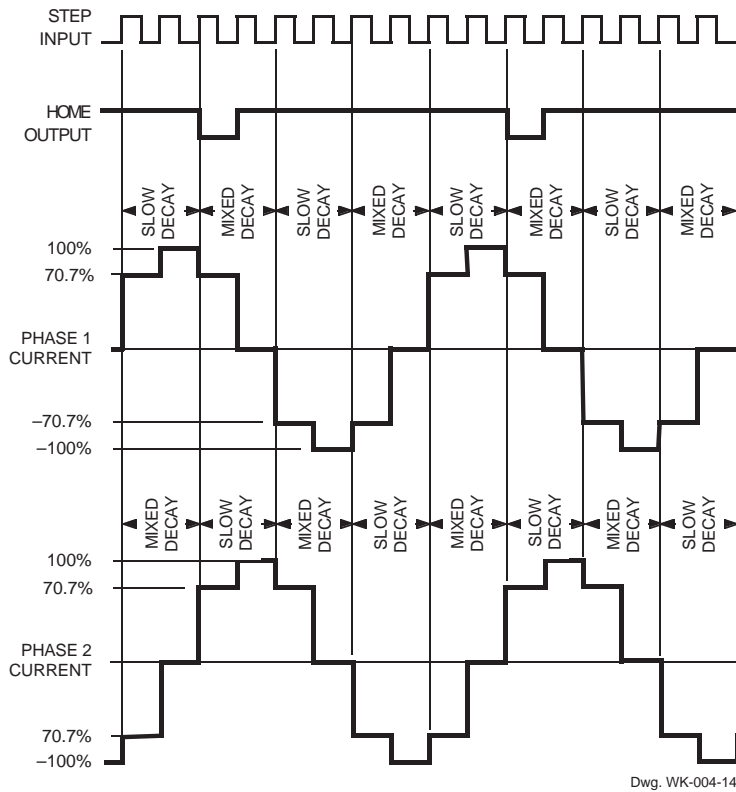


Figure 4. A3977 Half-Step Operation
 $MS_1 = H, MS_2 = L, DIR = H$

NOTE – Refer to table 2 for complete phase current level at each step.

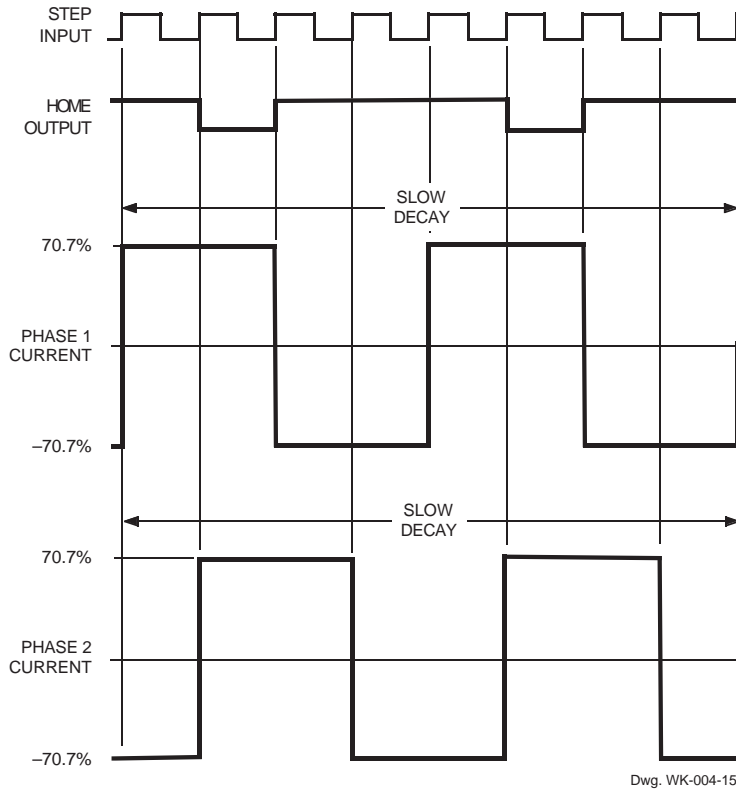
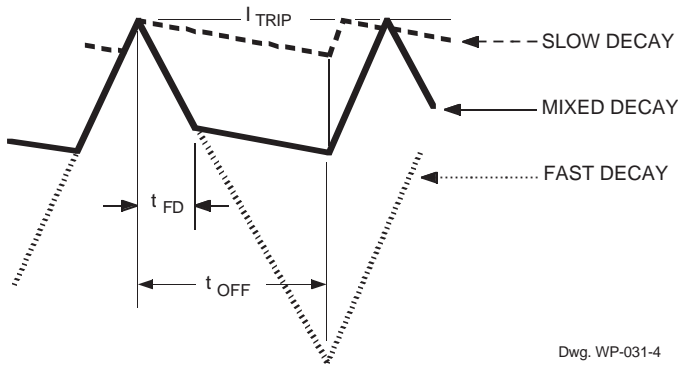


Figure 5. A3977 Full-Step Operation
 $MS_1 = MS_2 = L, DIR = H$



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Figure 7. Current-Decay Waveforms

Fast decay (figure 7) solves the current-regulation problem of slow decay. With almost the full supply across the motor winding it has the ability to quickly get the current out of the winding. The disadvantage of fast decay is the increased current ripple, which in turn causes increased motor heating.

Mixed decay (figure 7) splits the fixed-off time of the PWM cycle into fast and then slow decay. When the current reaches I_{TRIP} , the device will go into fast-decay mode until the voltage on the RC terminal decays to the voltage on the PFD terminal (V_{PFD}). The time that the device operates in fast decay is approximated by:

$$t_{FD} = R_T C_T \ln(0.6V_{DD}/V_{PFD})$$

After this fast-decay portion (t_{FD}), the device will switch to slow-decay mode for the remainder of the fixed-off time period. The result is low current ripple, but with increased bandwidth to track the ideal sine wave for microstepping.

Although mixed decay improves microstepping performance it will still have higher current ripple than slow decay. The best solution is to use a slow decay on the increasing slope of the sine wave and mixed decay on the falling slope of the sine wave output, which the A3977/97 does automatically. When a step-command signal occurs on the STEP input the translator automatically sequences the DACs to the next level. If the new DAC output level is lower than the previous level then the decay mode for that H-bridge will be set by the voltage level on the

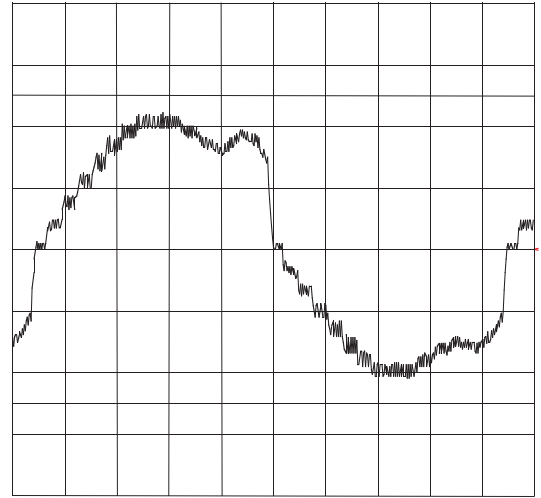


Figure 8. Slow-Decay Motor Current

PFD input (fast, slow, or mixed decay). If the new DAC level is equal or higher to the previous level then the decay mode for that H-bridge will be slow decay (see figures 2 thru 5). Figure 9 is a scope plot of the A3977 motor current with slow decay on the rising slope and mixed decay on the falling slope. For comparison, included is a motor current scope plot (figure 10) of the A3977 set to 100% fast decay on the falling slope of the sine wave and slow decay on the rising slope.

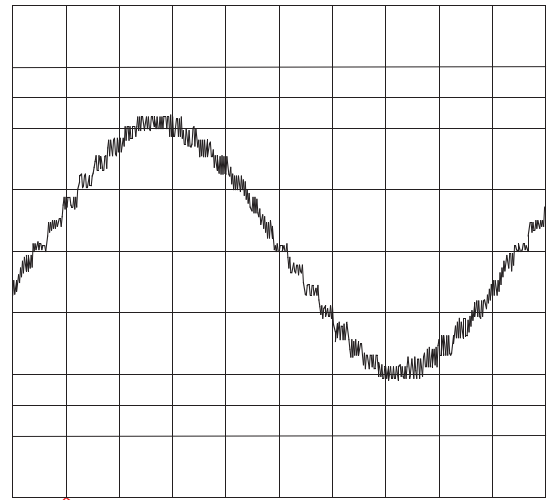


Figure 9. Mixed-Decay Motor Current

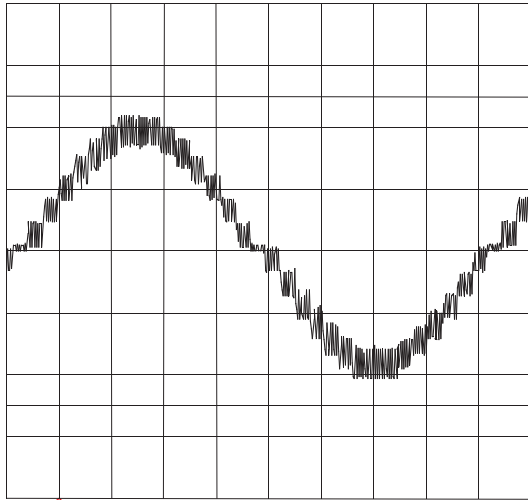


Figure 10. Fast-Decay Motor Current

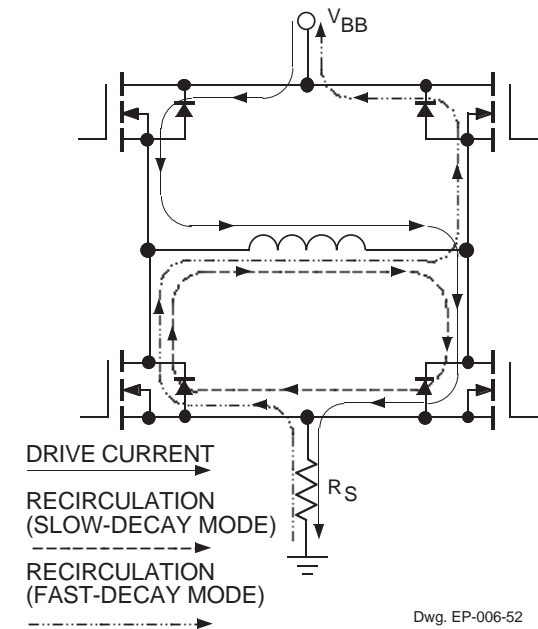


Figure 11. Current Paths with Synchronous Rectification Enabled

Synchronous Rectification When a PWM off cycle is triggered, by a bridge disable command or internal fixed-off time cycle, load current will recirculate according to the decay mode selected by the control logic (figure 6). The A3977/79 synchronous rectification (SR) feature will turn on the appropriate DMOS devices during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver (figure 11). In fast-decay synchronous rectification mode the voltage across R_S is monitored to prevent reverse conduction. Just before the recirculation current reaches zero all of the DMOS devices are turned off and current flows through the body diodes.

In a typical stepper-motor application the motor driver IC is in current-decay (recirculation) mode for a higher percentage of the PWM cycle compared to the on time. This means that most of the power dissipation is a result of the forward-voltage drop of the internal body diode of the power DMOS. This is illustrated by the first order power calculation of output power dissipation in slow-decay recirculation mode with and without synchronous rectification enabled for the A3979.

Assume:

$$I = I_{LOAD} = 1.5 \text{ A, and}$$

$$r_{DS(on)} = \text{on resistance of the sink DMOS transistors} = 0.22 \text{ ohm, and}$$

$$V_F = \text{forward voltage drop of the sink DMOS body diodes} = 1.4 \text{ V.}$$

With synchronous rectification enabled:

$$P_D = I^2 (r_{DS(on)} + r_{DS(on)}) = 1.52 (0.22 + 0.22) = 0.99 \text{ W.}$$

With synchronous rectification disabled:

$$P_D = (IV_F) + (I^2 r_{DS(on)}) = (1.5 \times 1.4) + (1.52 \times 0.22) = 2.595 \text{ W.}$$

The power dissipation reduction by using the A3977's synchronous rectification feature can eliminate the need for external Schottky diodes in most stepper-motor applications thereby saving the cost and board space for these components.

Logic Control The A3977/79 SLEEP input is used to minimize power consumption when not in use. This disables much of the internal circuitry including the output DMOS, regulator, and charge pump. Total logic plus motor supply current in sleep mode is $40 \mu\text{A}$. Logic Low will put the device into sleep mode; logic High will allow normal operation and starts up the device in the home position. The A3977/79 sleep-mode feature is critical to new designs requiring low off-state current draw. The ENABLE and RESET inputs turn on or off all of the DMOS outputs. Translator inputs are independent of the ENABLE input state so the outputs can be disabled and then stepped to a defined microstep state and then reenabled in this position. The RESET input resets the translator to the home state.

The HOME output is a logic output indicator of the initial state of the translator. At power up, the translator is reset to the home state. (See figures 2 through 5 for home state conditions). The HOME output-current level is common to all four microstepping levels in the A3977/79. It can be used as a control input to indicate that the microstepping resolution can be changed at this step without causing a current and therefore torque disturbance to the motor.

Protection Circuitry An under-voltage lockout circuit protects the A3977/79 from potential shoot-through currents when the motor supply voltage is applied before the logic supply voltage. All outputs are disabled until the logic supply voltage is above 2.7 V; the control logic is then able to correctly control the state of the outputs. Thermal protection circuitry turns off all the power outputs if the junction temperature exceeds 165°C. As with most integrated thermal shutdown circuits, this is intended only to protect the A3977/79 from failure due to excessive junction temperature and will not necessarily protect the IC from output short circuits. Normal operation is resumed when the junction temperature has decreased by about 15°C.

Packaging The A3977/79 is offered in two power packages, a 44-lead plastic power PLCC package (A3977SED) and a 28-lead TSSOP package with exposed thermal pad (A3977SLP and A3979SLP). The 44-lead PLCC has four copper batwing tabs for maximum heat transfer and a thermal resistance of 32°C/W. The 28-lead TSSOP measures only 9.7 mm × 4.4 mm × 0.9 mm and has a thermal resistance of 38°C/W. The TSSOP package is less than 1/4 the size of the PLCC package yet it can achieve close to the same thermal resistance. This is an important advantage in applications that have extreme space constraints.

CONCLUSION

Allegro's new microstepping motor driver ICs, A3977 and A3979, with integrated step and direction translator interface offers several features resulting in application benefits. The A3977/79 features automatic mixed-mode current-decay control, PWM current control, synchronous rectification, low $r_{\text{DS(on)}}$ power DMOS outputs, full-, half-, quarter-, eighth-, and sixteenth-step operation, home output, sleep mode, and an easy-to-implement step and direction interface. With the A3977 and A3979, Allegro has produced high performance and cost-effective solutions for the next generation of stepper motor drivers.

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