

SCM1100M Series High Voltage 3 Phase Motor Drivers

Introduction

The SCM1100M is a high voltage three-phase motor driver IC for 85 to 253 VAC input, middle output power motor driver systems. IGBTs, diodes, and controller ICs are all housed in the proprietary SCM package (figure 1), and the protection circuits enhance system-level reliability. Features and benefits include the following:

- Each half-bridge circuit consists of a pre-driver circuit that is completely independent from the others
- Protection against simultaneous high- and low-side turn-on (STP)
- Bootstrap diodes with series resistors for suppressing inrush current are incorporated
- CMOS compatible input (3.3 to 5 V)
- Designed to minimize simultaneous current through both high- and low-side IGBTs by optimizing gate drive resistors
- UVLO protection with auto restart
- Overcurrent protection with off-time period adjustable by an external capacitor
- Fault (FO indicator) signal output at protection activation: UVLO (low side only), OCP, and STP
- Proprietary power DIP package
- UL Recognized Component (File No.: E118037)



The product lineup for the SCM1100M series provides the following options for motor driving applications:

Part Number	IGBT Rating	Remarks
SCM1101M	600 V/10 A	Low saturation voltage
SCM1103M	600 V/5 A	Low saturation voltage
SCM1104M	600 V/8 A	Low saturation voltage
SCM1104MF	600 V/8 A	Low saturation voltage
SCM1105MF	600 V/15 A	Low saturation voltage
SCM1106M	600 V/10 A	High speed
SCM1106MF	600 V/10 A	High speed
SCM1110MF	600 V/15 A	High speed

Energy-Conserving Technology

The SCM1100M series is one of the expanding IPM product lines being offered by the Sanken Electric Company. *IPM*

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

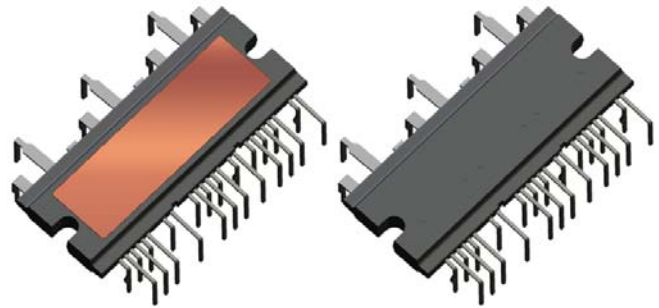


Figure 1. SCM1100M Series packages are fully molded DIPs. For 10 to 15 A (suffix F) variants, a copper heat dissipation pad is attached to the upper surface of the case.(left); for 5 to 10 A devices, the standard case is available (right).

stands for inverter power module, a technology that has now become prominent in the marketplace, and for Sanken, it highlights a broad variety of high voltage, three-phase motor driver ICs targeted at the residential white goods (home appliance) and commercial three-phase motor market segments, such as: air conditioners, refrigerators, and washing machines.

Sanken IPM devices are particularly well-suited to applications in variable speed control systems and power inverter systems. Sanken has developed a great deal of expertise in these markets, which have become mature in certain areas due to governmental regulations, and are emerging in many other marketplaces. Demand for these applications is expected to increase rapidly in the near future, due to commercial economic pressures and governmental regulations mandating the use of energy-conserving technologies.

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Rapid Redesign Support

IPM type ICs are gradually becoming prevalent for controlling motors in residential and commercial laundry washing machines. In this application, the ICs replace several discrete components, thus saving application space and design effort. In many instances, IPM devices yield the lowest overall cost solution, especially in the current regulatory environment, which is forcing manufacturers to redesign their power management systems. Traditional discrete-device topologies are proving difficult to adapt to these applications, and manufacturers can take advantage of rapid design solutions using the highly integrated topologies offered by IPM types of devices. Sanken Electric IPMs optimally fulfill such market needs with products that integrate our latest technologies inside a single package. Simplified Design for Application Circuits

The SCM1100M series supports the 3-shunt method, in which a shunt resistor is used in each phase. This enables small currents to be detected, and highly accurate inverter control to be achieved, thus contributing to low motor noise. In addition, each of the three phases contains an overcurrent protection circuit, and a function that prevents simultaneous turn-on of both the high-side and low-side IGBTs.

Overall, use of the SCM1100M series with the 3-shunt method allows a 15% reduction in the area of the application print circuit board used for the main circuit of the inverter, and a reduction in the quantity of components of about 50%. With these and many other designer-friendly features, the SCM1100M series allows a highly reliable inverter main circuit to be designed using only a small number of external components.

Robust Device Design

Several built-in features allow the SCM1100M series to support a more dependable overall application.

A built-in high-voltage bootstrap diode is built-in, simplifying trace layout on the application PCB by reducing component count, and eliminating the corresponding adequate creepage distance.

An in-rush current-absorbing resistor provides built-in protection (STP) circuit against high-side/low-side simultaneous on (shoot-through). In addition, employing a pre-driver for each half-bridge, prevents high/low simultaneous ON due to erroneous command signal input or external noise.

The embedded pre-driver for each half-bridge ensures short input dead-time. This optimizes the switching speed of high/low sides,

allowing stable control to be achieved. It also avoids consecutive short-circuits when OCP protection mode is released.

The OCP mode also features soft turn-off at power-down during an overcurrent event. This minimizes negative voltage impinging on the LS terminal, by restraining di/dt . This protects the IC from failure due to reverse voltage there and on the external current sense circuit.

All three drive phases can be simultaneously brought to a complete stop (all three gates turned off) during protection modes. This can be implemented by connecting the 3 failure signal output terminals externally. The FO terminal is also used as an enable input. Failure signal output continues during protection modes: CMOS logic circuit operation continues, as well as UVLO during OCP and STP modes.

Pin Functional Descriptions

This section describes the features of the SCM1100M devices in order by pin function. Refer to figure 2 for a block diagram of the devices.

U, V, and W. These pins are the outputs of the individual IC phases, and serve as the connection terminals to the 3 phase motor that is being driven.

VB1, VB2, and VB3. Circuit main supply inputs that drive high-side IGBTs. Serve as terminals for the bootstrap capacitors, CBOOT, for each phase. The bootstrap circuits are floated during operation, thus each half-bridge circuit needs one bootstrap circuit, and it is recommended to place CBOOT as close to the IC as possible (see figure 2).

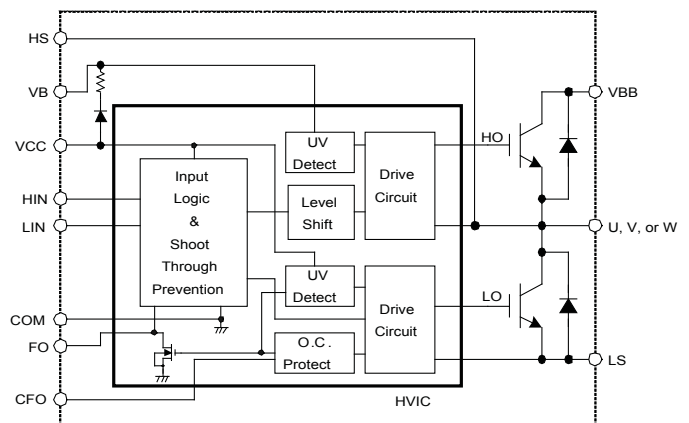


Figure 2. SCM1100M Series Phase Block Diagram. These devices support three phases, referred to as U, V, and W. One of three phases is shown in the diagram.

At the beginning of operation, during the startup period, this capacitor needs to be fully charged by turning on the low-side IGBT. The capacitance of the individual capacitors can be calculated by the following formulas, and whichever resulting capacitance value is larger should be chosen:

$$C_{\text{BOOT}} (\mu\text{F}) > 800 \times t_{\text{Loff}} (\text{s}) ,$$

or

$$C_{\text{BOOT}} = 0.1 \mu\text{F} ,$$

where T_{Loff} is the maximum off-period of the low-side IGBT, in seconds, corresponding to the non-charging period of CBOOT.

The gate driver circuit consumes current even if the high-side IGBT is not on, and the voltage across CBOOT goes down. Therefore, make sure that that sufficient voltage is maintained across CBOOT during low frequency operation, such as the startup period. In addition, capacitance tolerance needs to be taken into account in selecting the CBOOT value, and it is strongly recommended to optimize the value of CBOOT through actual board tests to make sure UVLO circuits for VB1, VB2 and VB3 are not activated.

HS1, HS2, and HS3. These pins are internally connected to the U, V, and W pins. The negative node of corresponding CBOOT is connected to the pin.

VCC1, VCC2, and VCC3. These pins are logic supply inputs. To prevent malfunctioning of operation from ripple voltage on supply voltage input, it is recommended to place a ceramic capacitor ($> 0.01 \mu\text{F}$) as close to the pin as possible.

COM1, COM2, and COM3. These are logic GND pins of the incorporated pre-driver chips. In order to drive and control the internal IGBTs properly, these should be connected as close to the LSx pins as possible.

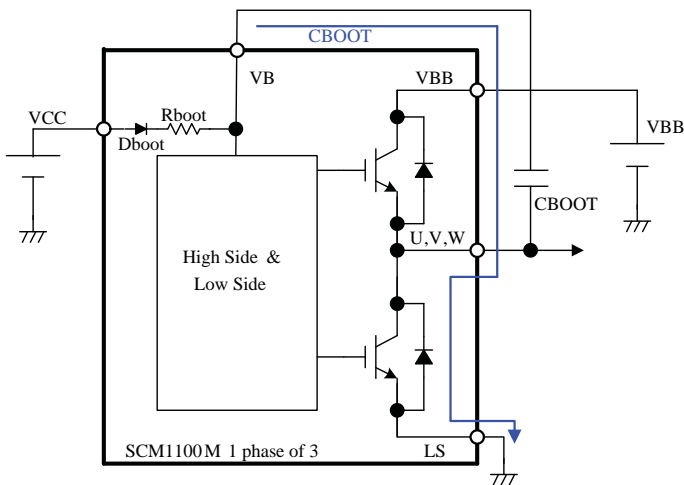


Figure 3. Bootstrap Circuit. Each of the three phases has an independent bootstrap circuit. The CBOOT circuit for one phase is shown above.

HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3. These are gate driver control pins, and are 5 V CMOS compatible, with Schmitt trigger circuits. These are active high, and have internal pull-down 100 kW resistors. In case of high noise interference or unstable input logic status, it is recommended to use external filter circuits or additional pull-down resistors. The equivalent circuits are shown in figure 5.

VBB1, VBB2, and VBB3. These are the main supply inputs. Place bypass capacitors and also film capacitors for snubber circuits of approximately $0.1 \mu\text{F}$ at each pin, in order to suppress surge voltage. In addition, it is recommended to shorten the PCB traces for those pins to a minimum.

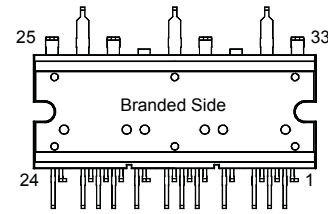


Figure 4. SCM1100M Series Pin-out Diagram. The pin assignments are listed in the table below.

Terminal List Table

Name	Number	Function
1	FO1	U phase fault output for overcurrent and UVLO detected
2	CFO1	Capacitor for U phase overcurrent protection hold time
3	LIN1	Signal input for low-side U phase (active high)
4	COM1	Supply ground for U phase IC
5	HIN1	Signal input for high-side U phase (active high)
6	VCC1	Supply voltage for U phase IC
7	VB1	High-side floating supply voltage for U phase
8	HS1	High-side floating supply ground for U phase
9	FO2	V phase fault output for overcurrent and UVLO detected
10	CFO2	Capacitor for V phase overcurrent protection hold time
11	LIN2	Signal input for low-side V phase (active high)
12	COM2	Supply ground for V phase IC
13	HIN2	Signal input for high-side V phase (active high)
14	VCC2	Supply voltage for V phase IC
15	VB2	High-side floating supply voltage for V phase
16	HS2	High-side floating supply ground for V phase
17	FO3	W phase fault output for overcurrent and UVLO detected
18	CFO3	Capacitor for W phase overcurrent protection hold time
19	LIN3	Signal input for low-side W phase (active high)
20	COM3	Supply ground for W phase IC
21	HIN3	Signal input for high-side W phase (active high)
22	VCC3	Supply voltage for W phase IC
23	VB3	High-side floating supply voltage for W phase
24	HS3	High-side floating supply ground for W phase
25	VBB	Positive DC bus supply voltage
26	W	Output for W phase
27	LS3	Negative DC bus supply ground for W phase
28	VBB	Cut-pin (positive DC bus supply voltage)
29	V	Output for V phase
30	LS2	Negative DC bus supply ground for V phase
31	VBB	Cut-pin (positive DC bus supply voltage)
32	U	Output for U phase
33	LS1	Negative DC bus supply ground for U phase

LS1, LS2, and LS3. These are inverter GND terminals and a shunt resistor for monitoring current should be placed between those pins and the COM pins. Trace length between the corresponding current sensing resistor and LSx pin should be as short as possible, otherwise, malfunctioning may occur.

CFO1, CFO2, and CFO3. In the event of the overcurrent protection enabling, both high- and low-side drivers are turned off. The overcurrent protection off-time period is adjusted by the external capacitors at those pins. See the Protection Circuits section for more details.

FO. This pin is pulled down in the event of the protection circuits enabling; UVLO, OCP, or STP (Simultaneous high- and low-side turning on) being activated; or both high- and low-side IGBTs being turned off.

Figure 6 shows the internal circuit of the FO pin, which must be pulled-up by an external pull-up resistor because of the open drain structure. The sink current is limited to 5 mA. In addition, the FO pin potential is monitored by the internal circuit and when its potential is pulled down externally, it shuts off the circuit. Therefore, by tying the three FO pins together, it can shut off all phases if even one of the phase protection circuits is activated. It is recommended to place a capacitor C_N ($<0.01 \mu\text{F}$) near those pins to prevent malfunctioning from noise interference.

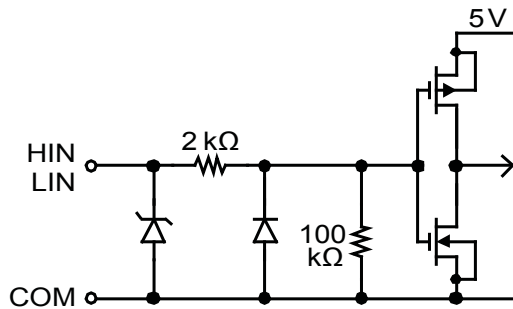


Figure 5. Logic Inputs. The HIN and LIN internal equivalent circuits are illustrated.

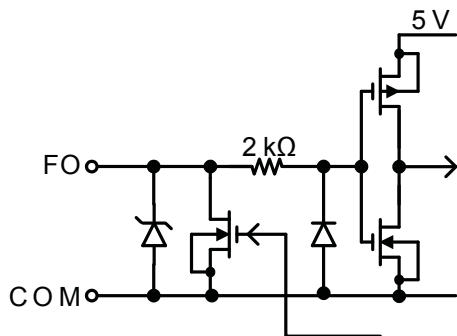


Figure 6. Fault Circuit Inputs. The internal circuits of the FO pins are illustrated.

Protection Circuits

This section describes the various protection circuits provided in the SCM1100M series.

Undervoltage Lockout (UVLO). The UVLO circuit is integrated to protect the IGBT from being driven by low gate driving voltage due to insufficient main supply voltage of the gate driver circuit. The UVLO circuit timing chart is shown in figure 7.

When the boot voltage (between VB and VS) becomes less than U_{VHL} , the high-side IGBT turns off. However, the FO pin is not pulled down. After that, when the boot voltage returns to the normal operating voltage range, it automatically restarts at the first rising edge of the control input signal.

When VCC voltage becomes less than U_{VLL} threshold, both high- and low-side IGBTs are turned off, and the FO pin is pulled down. After it recovers to the normal operating voltage, FO is raised by the pull-up resistor, and the IGBT is turned on at the next rising edge of each corresponding input.

Simultaneous High- and Low-Side On Protection (STP).

This circuit protects the high- and low-side IGBTs against the event of both the low- and high-side inputs being high, or a malfunction turning on both IGBTs because of noise interference. In that case, the FO pin is pulled down.

Overcurrent Protection (OCP). The overcurrent protection circuit monitors the voltage across the external current sensing resistor, and when it reaches the threshold voltage of 0.5 V (V_{TRIP}) and remains there longer than 2 μs , OCP shuts off both high- and low-side IGBTs. The OCP timing is shown in figure 8.

It is possible to adjust the off-time duration by an external capacitor at the CFO pin (see figure 9 for the circuit at the CFO pin, and figure 10 for timing effects). In that case, the current sensing resistor is dedicated to its respective output, and if only

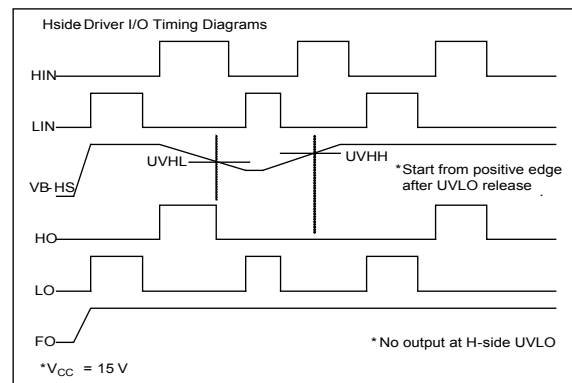


Figure 7. Undervoltage Protection (UVLO) timing diagram.

one of them is activated, only the corresponding phase circuit is turned off. During the off-time period, the FO pin remains low, and the phase circuit remains off, regardless of any input signals to the HIN and LIN pins. The OCP circuit is integrated in each phase circuit, and protects each phase circuit individually. However; as explained before, by tying the FO pins together, it is possible to shut off all phase circuits when one of the phases' OCP circuit is activated. See the Application Circuit section for more details. After being shutoff by OCP, and the CFO duration is passed, FO is pulled-up by the external resistor, and the IGBTs are enabled for activation, but it only occurs at the rising edge of the HIN and LIN inputs.

The value for the shunt (current sensing) resistor, R_S , can be calculated as follows:

$$R_S (\Omega) = 0.5 \text{ V} / I_{TRIP}(\text{typ.}) \text{ A} - 0.0035$$

where 0.0035 is the SCM1100 internal wiring resistance. For example, if $I_{TRIP}(\text{typ.}) = 10 \text{ A}$, then

$$0.5 \text{ V} / 10 \text{ A} - 0.0035 = 0.0465 \Omega$$

Note: The formula above does not include any parasitic resistance of the PCB traces.

The OCP off-time setting capacitors can be configured as either one common capacitor for all three CFOx pins, or as a separate capacitor for each CFOx pin. The value for each configuration can be calculated as follows,

for one common capacitor:

$$t_{off}(\text{min}) = t_{min} \text{ ms} = 0.31 \times C_{FO} \text{ nF}$$

for three individual capacitors:

$$t_{off}(\text{min}) = t_{min} \text{ ms} = 0.93 \times C_{FO} \text{ nF}$$

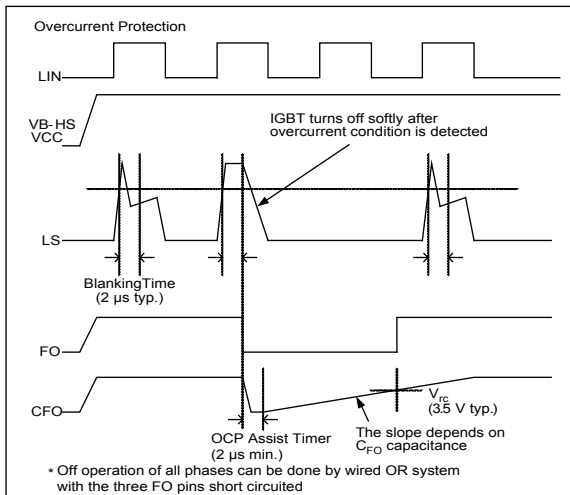


Figure 8. Overcurrent Protection (OCP) timing diagram.

It is recommended to use a less than 10 nF capacitor, otherwise, the formulas above are not applicable.

Precautions

Power-up Sequence. Make sure proper VCC voltage is secured before applying logic high to HIN and LIN. When powering down, apply logic low to all HIN and LIN pins, and then turn off VCC.

Short Circuit. Output short circuit (load short, short to GND) protection is not integrated, therefore; make sure such conditions are not applied to the IC.

PCB Trace Length. Circuit traces around the IC should be as short as possible. If the lengths are long, it may cause not only malfunctioning, but also IC breakdown because of surge voltage resulting from parasitic inductance of the traces.

Surge Voltage. Surge voltage superimposed on the inputs should be suppressed by capacitors. Otherwise, it could cause malfunctioning or IC breakdown in worst case scenarios.

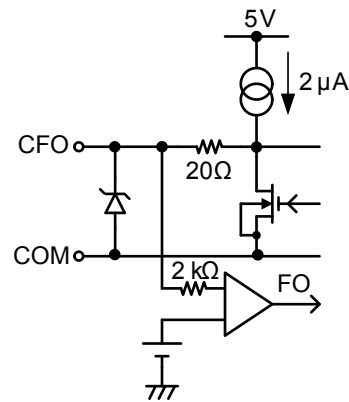


Figure 9. Overcurrent Protection (OCP) timing diagram.

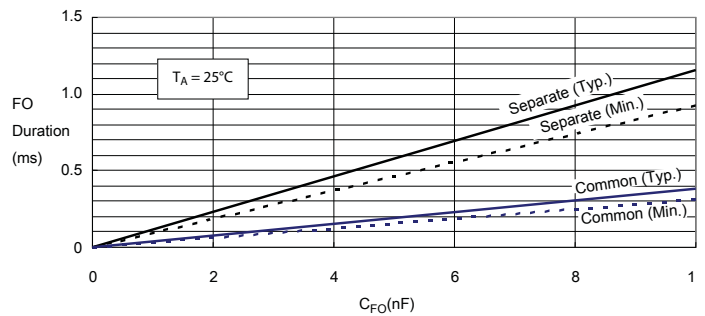
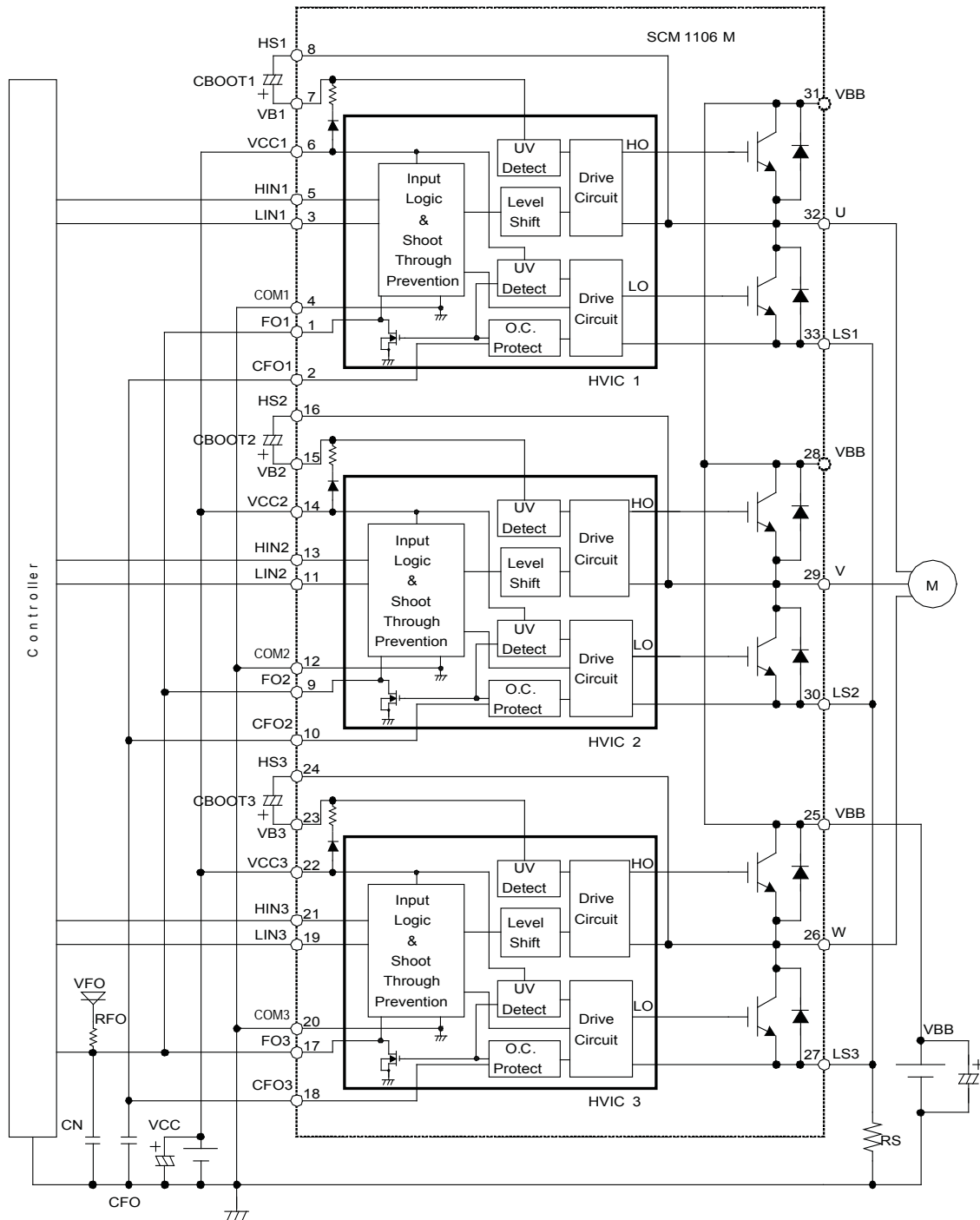


Figure 10. CFO Off-Time Duration versus C_{FO} Capacitance. Shown for common and separate capacitor configurations.

Input Dead-Time. Ensure a dead time between high- and low-side turn on and turn off to avoid simultaneous current flow through the high- and low-side IGBTs. It is recommended that the dead time be longer than 2 μ s. The IC itself does not have an integrated dead time circuit.

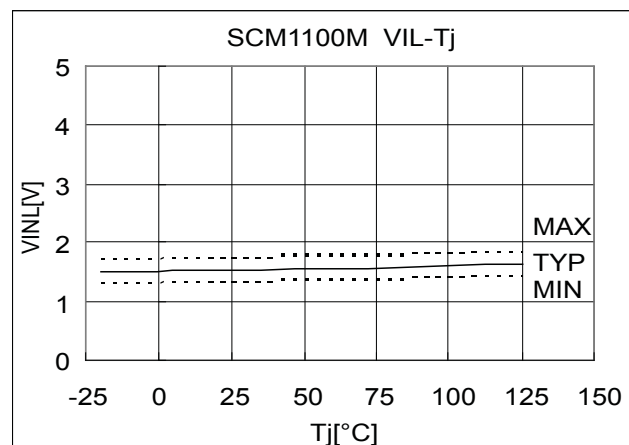
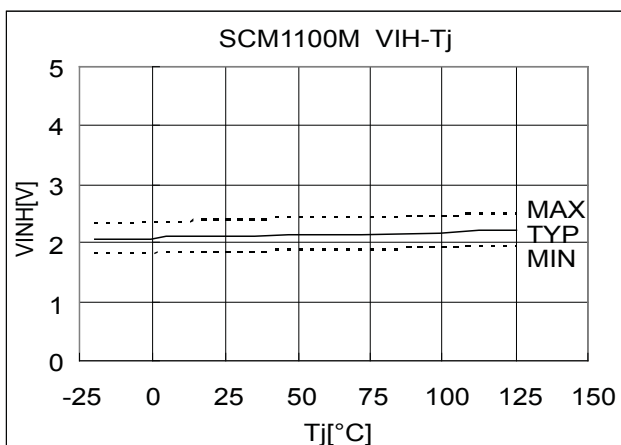
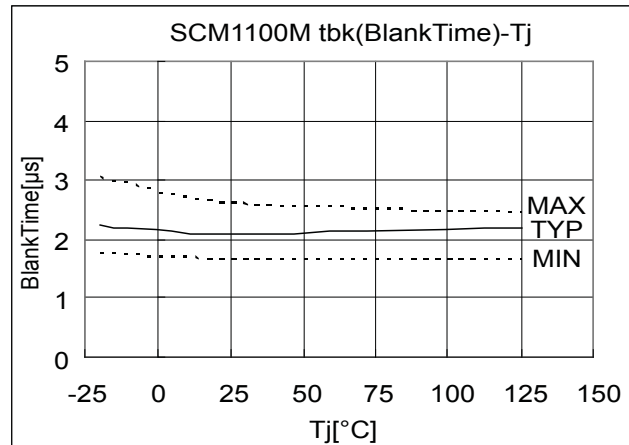
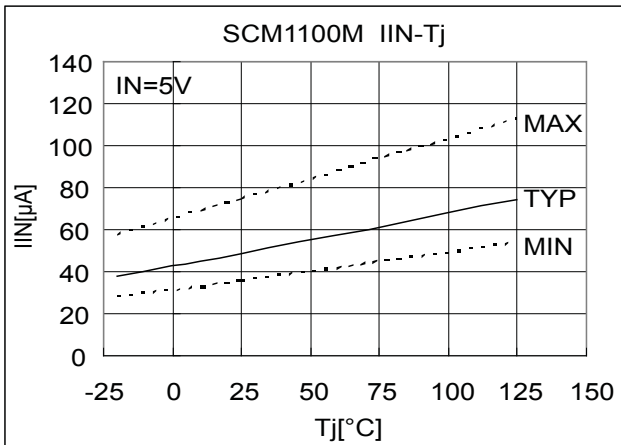
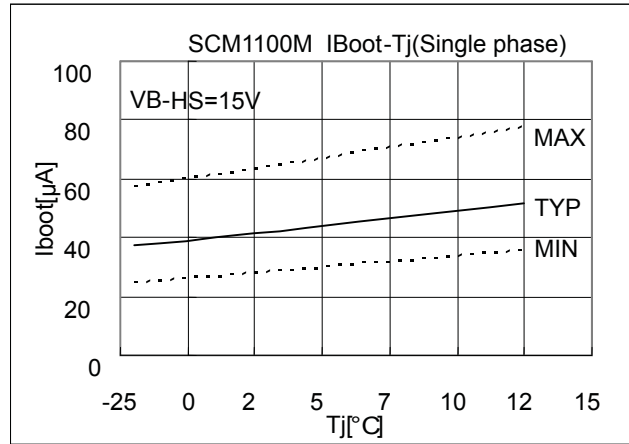
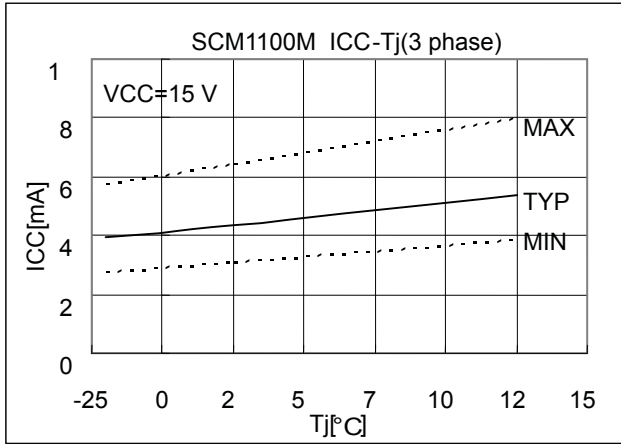
Application Circuit

The following diagram applies for a common current sensing shunt resistor for the three phases.



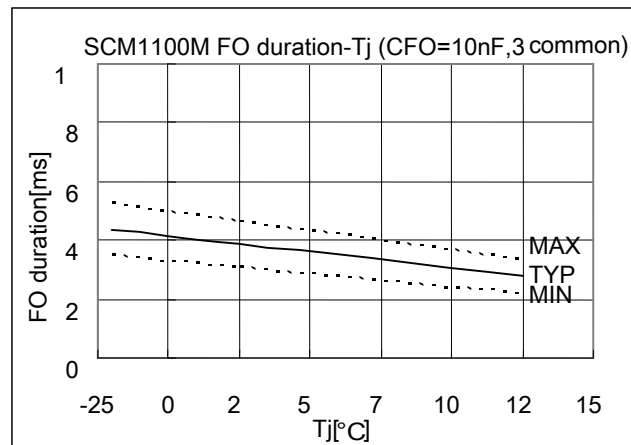
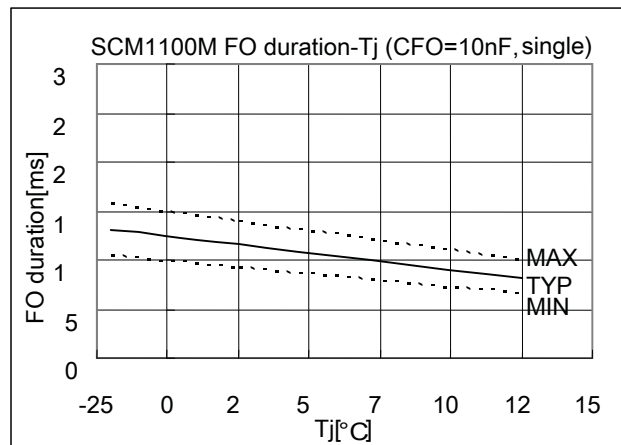
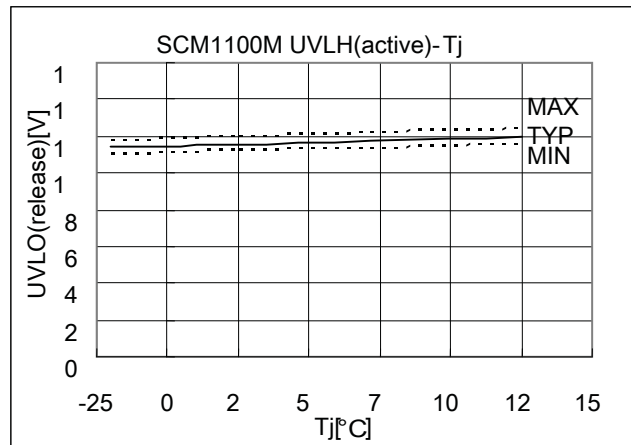
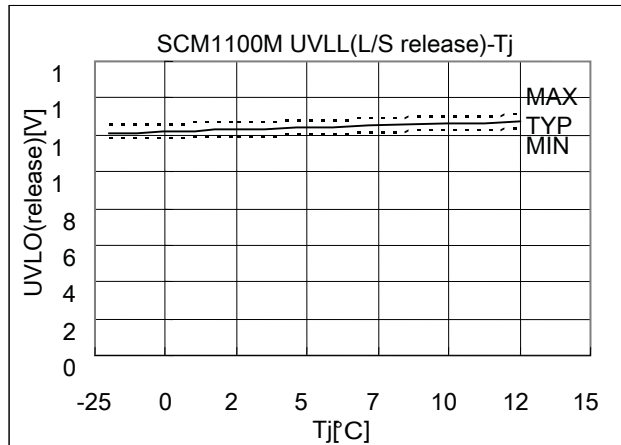
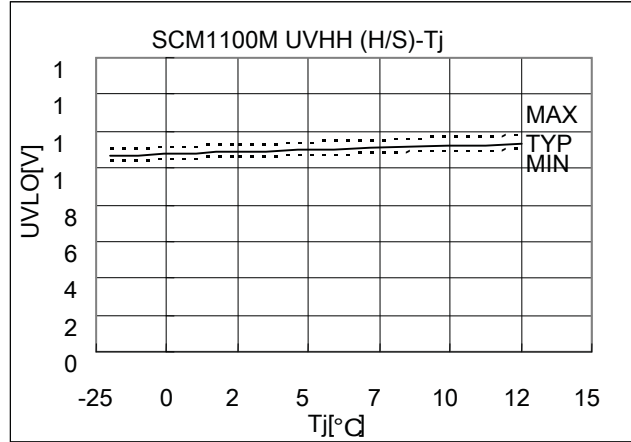
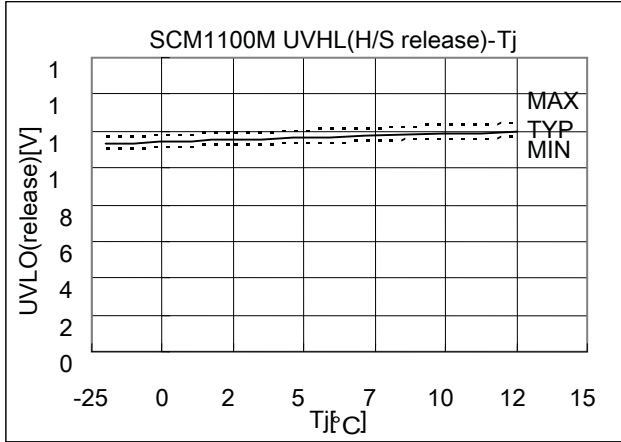
Characteristic Performance Data

The following data is applicable to all of the SCM1100M series.



Characteristic Performance Data (continued)

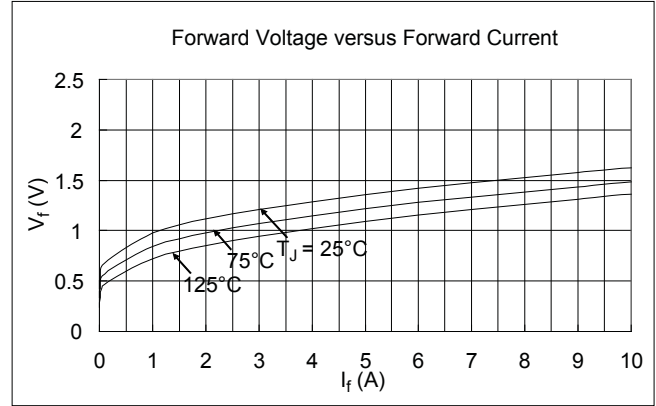
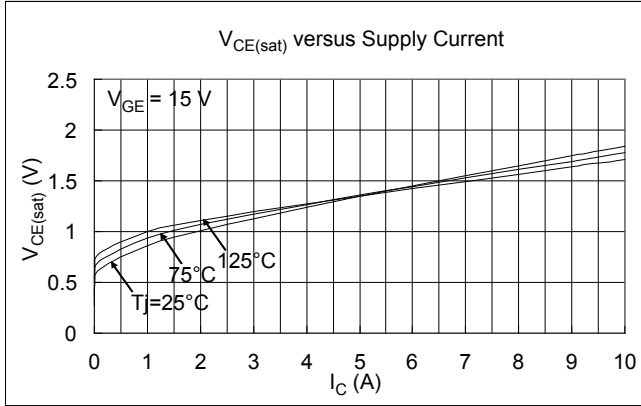
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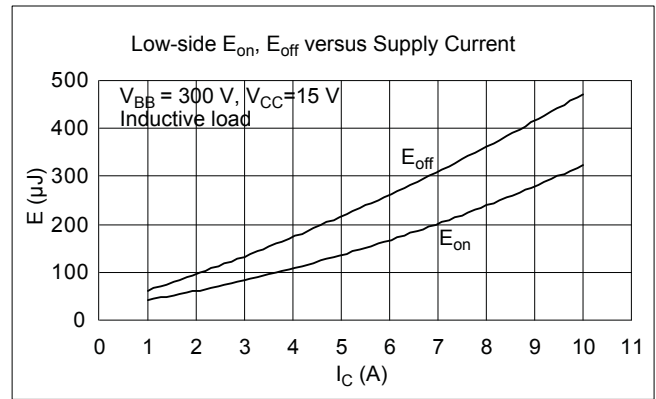
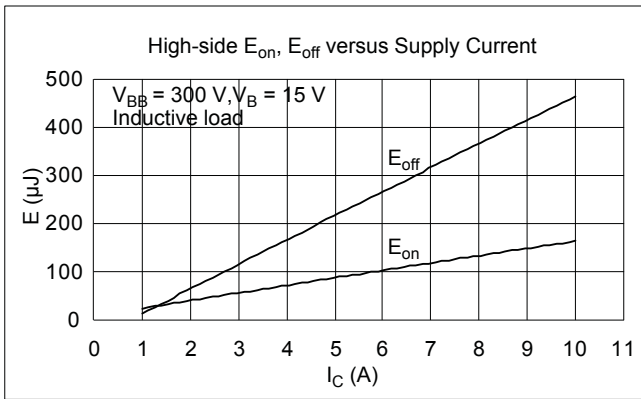
Output Characteristic Performance Data

The following data is applicable to the SCM1101M or SCM1101MF, 10 A device.

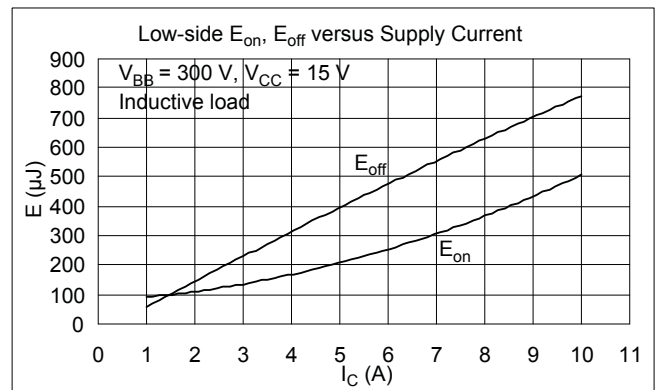
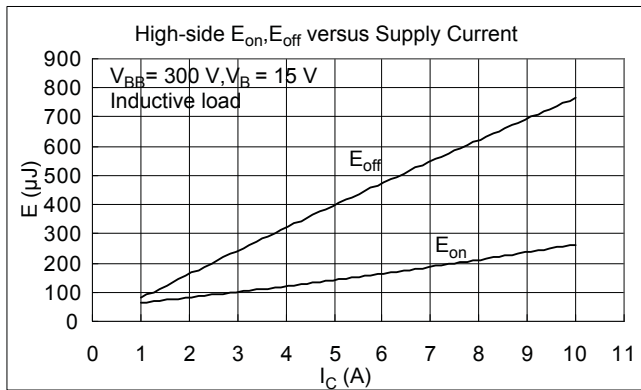
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at T_J = 25°C)



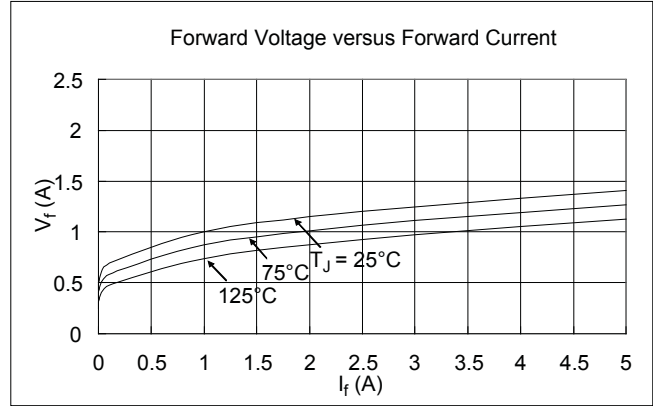
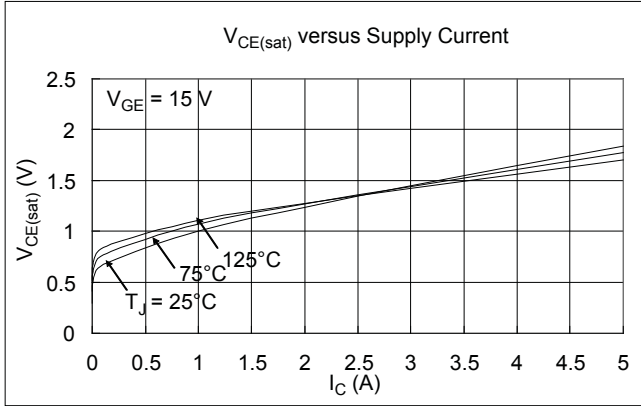
Switching Power Loss (Half-Bridge Operation at T_J = 125°C)



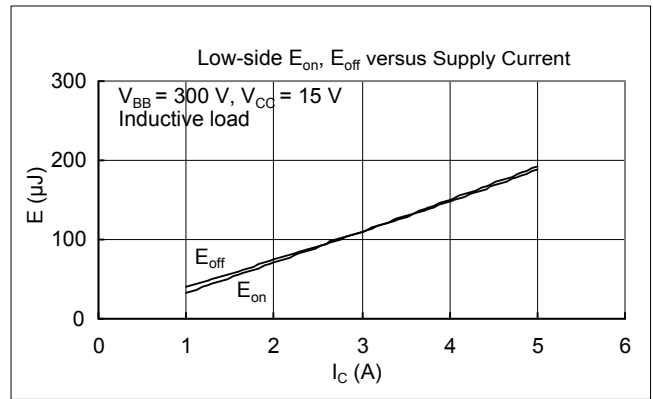
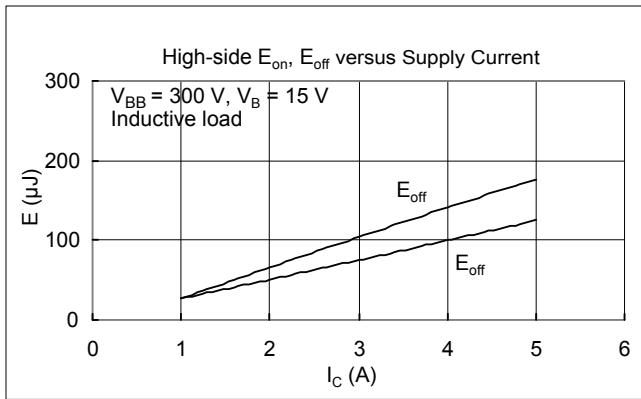
Output Characteristic Performance Data (Continued)

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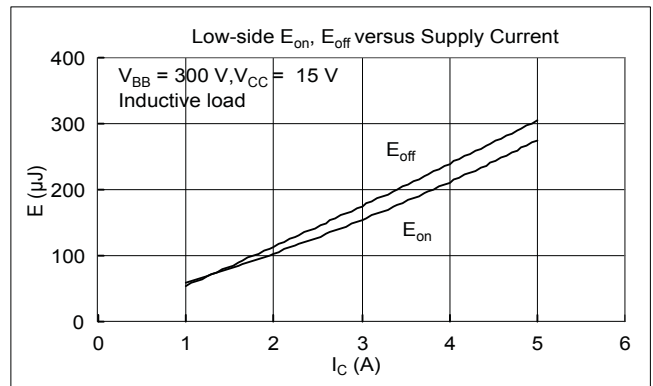
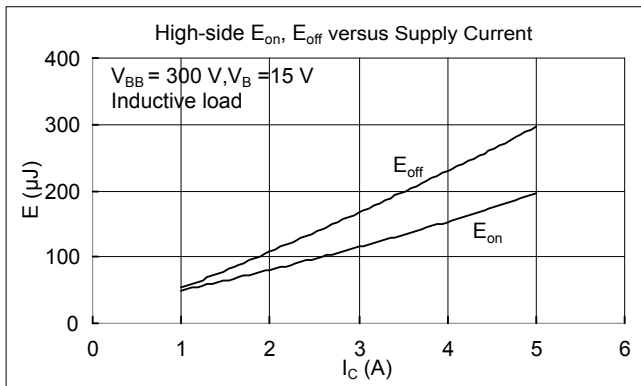
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at $T_J = 25^\circ\text{C}$)



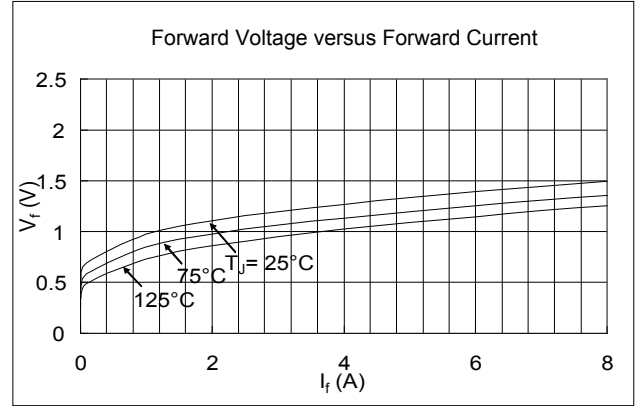
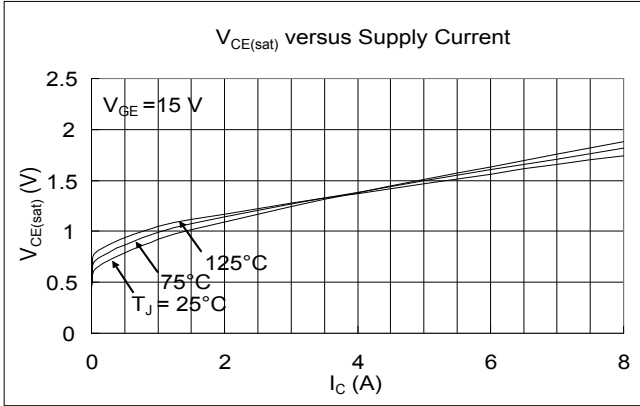
Switching Power Loss (Half-Bridge Operation at $T_J = 125^\circ\text{C}$)



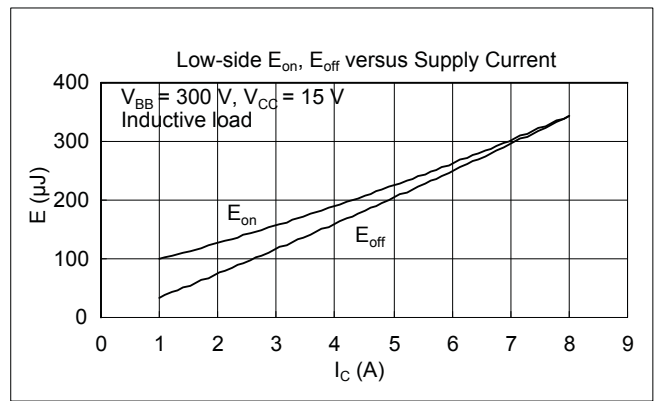
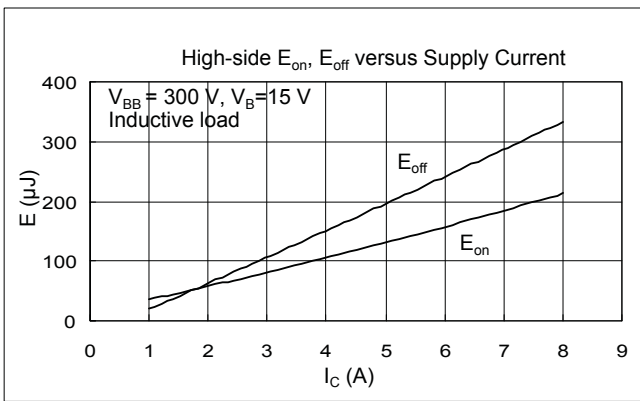
Output Characteristic Performance Data (Continued)

The following data is applicable to the SCM1104M or SCM1104MF, 8 A device.

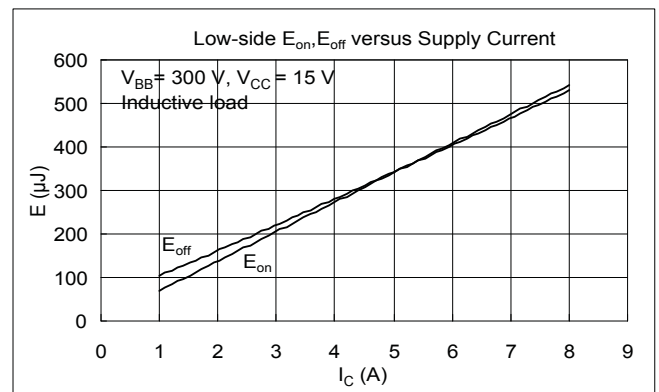
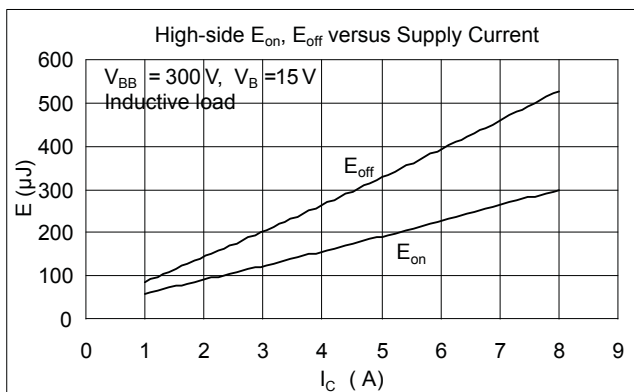
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at $T_J = 25^\circ\text{C}$)



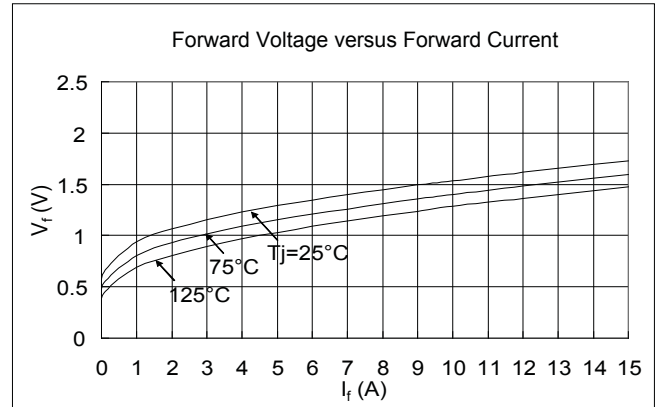
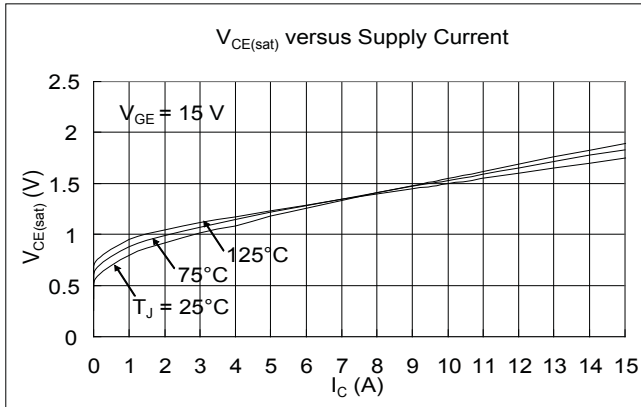
Switching Power Loss (Half-Bridge Operation at $T_J = 125^\circ\text{C}$)



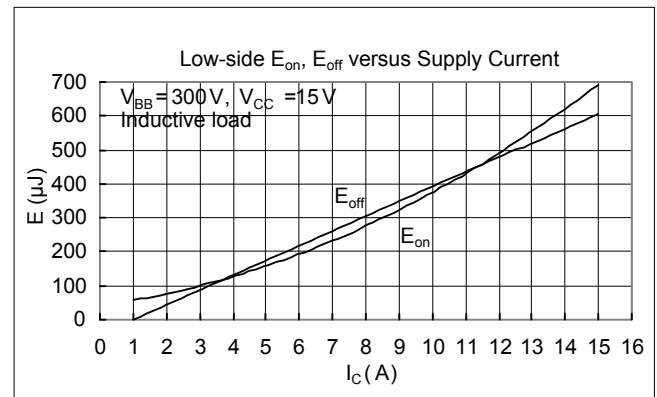
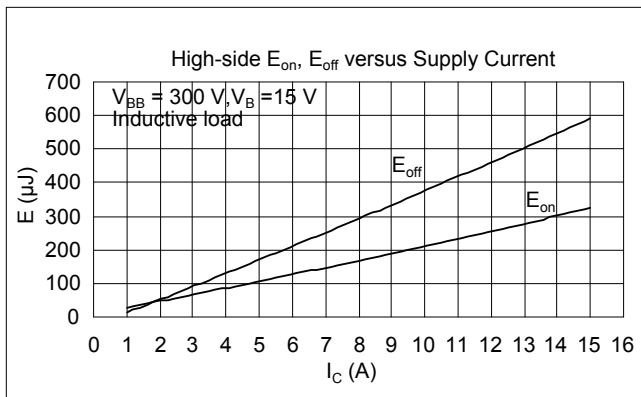
Output Characteristic Performance Data (Continued)

The following data is applicable to the SCM1105MF, 15 A device.

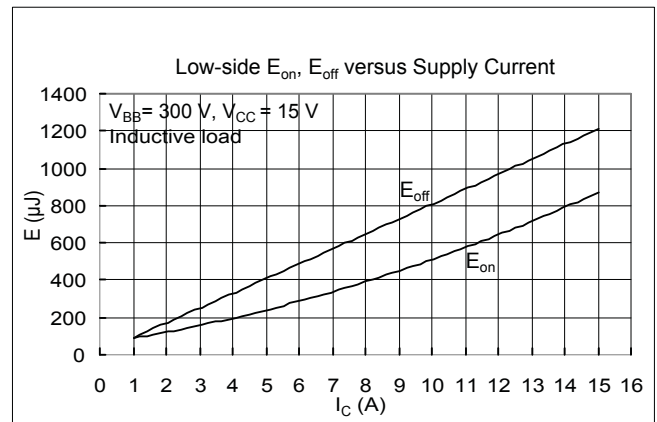
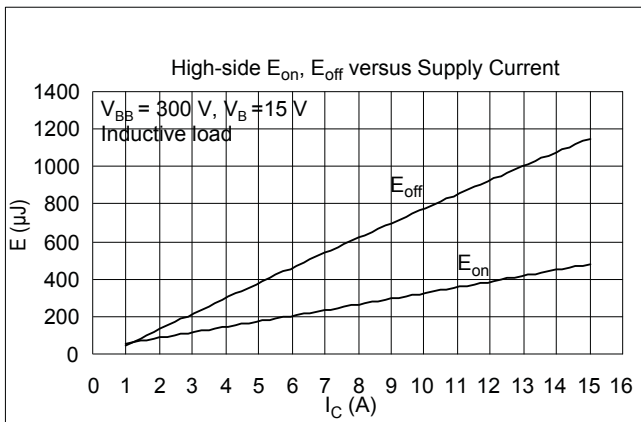
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at $T_J = 25^\circ\text{C}$)



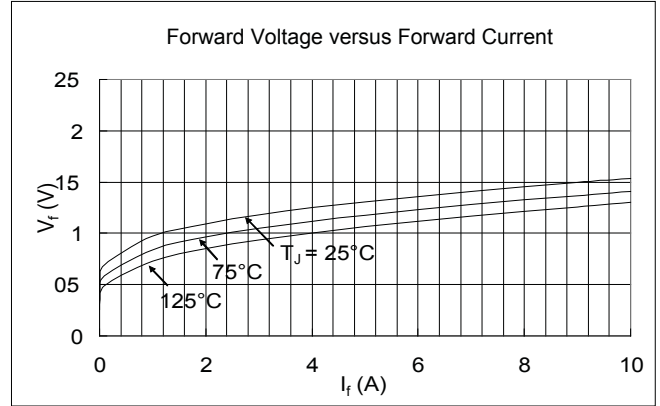
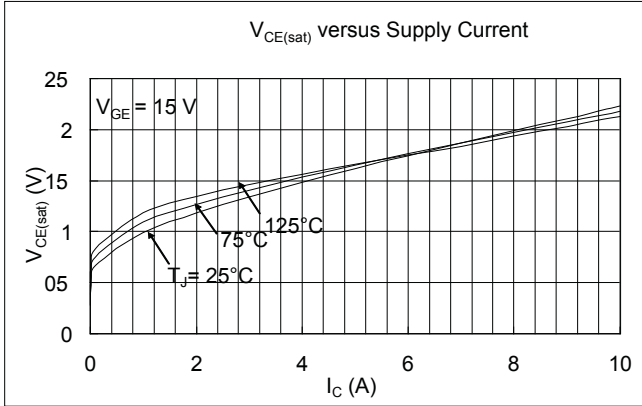
Switching Power Loss (Half-Bridge Operation at $T_J = 125^\circ\text{C}$)



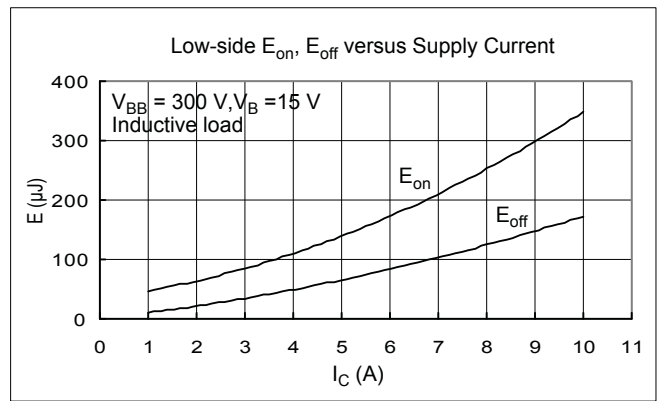
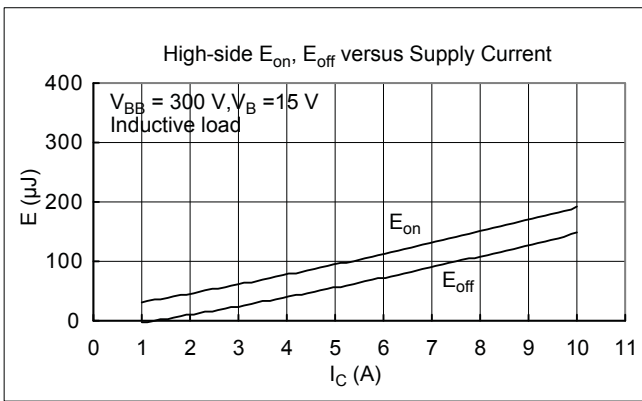
Output Characteristic Performance Data (Continued)

The following data is applicable to the SCM1106M and SCM1106MF, 10 A device.

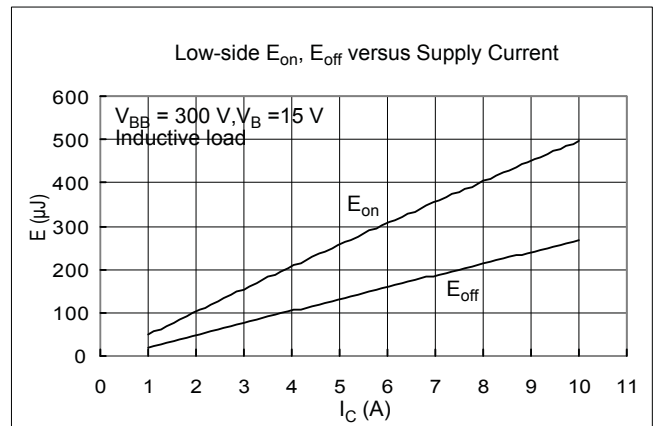
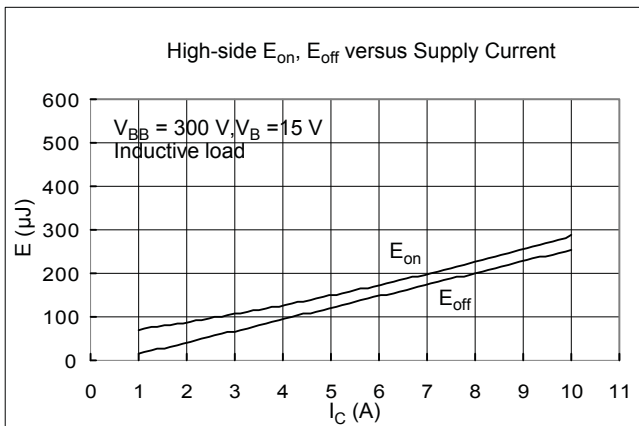
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at $T_J = 25^\circ\text{C}$)



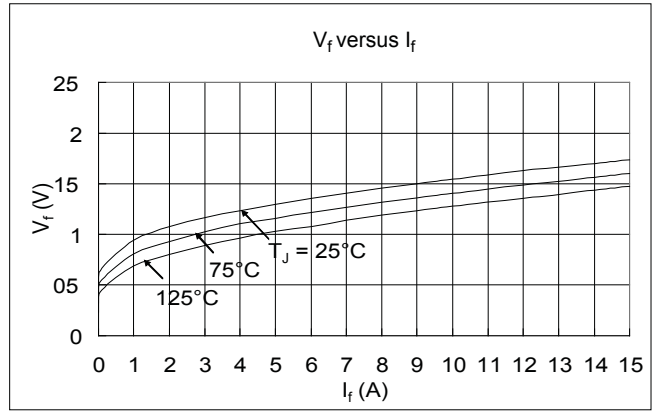
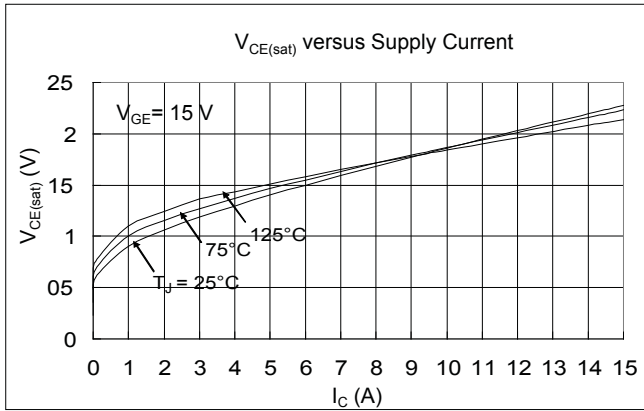
Switching Power Loss (Half-Bridge Operation at $T_J = 125^\circ\text{C}$)



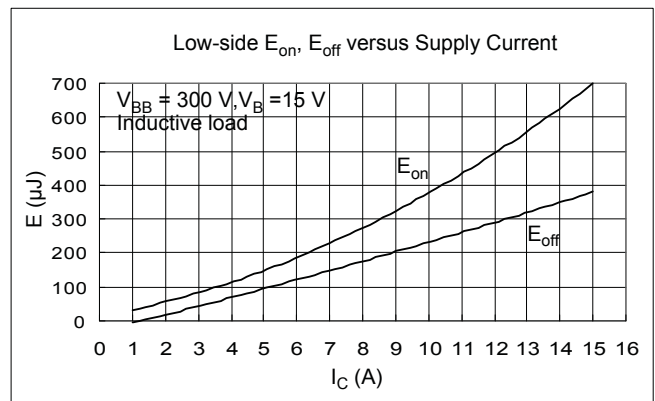
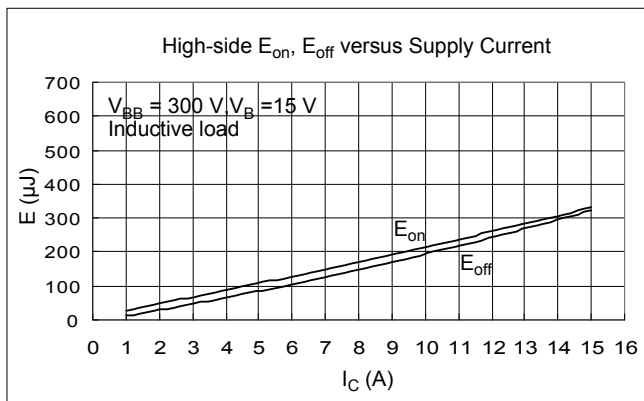
Output Characteristic Performance Data (Continued)

The following data is applicable to the SCM1110MF, 15 A device.

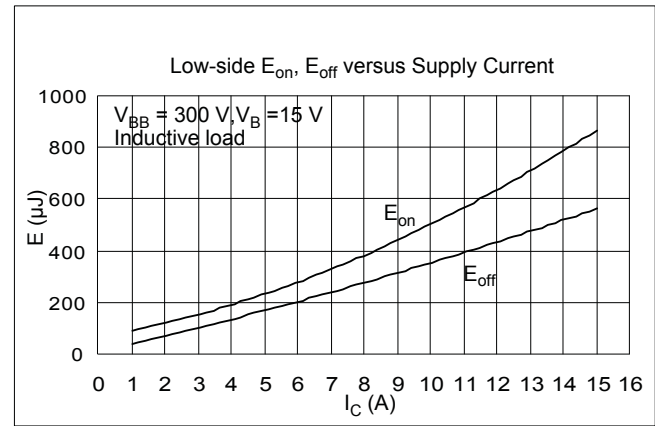
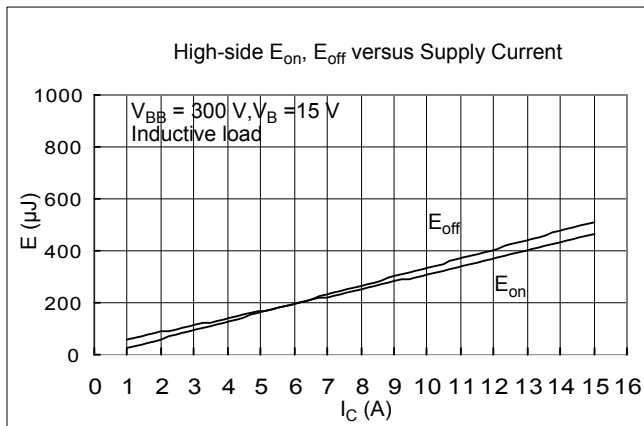
IGBT and FRD DC Characteristics



Switching Power Loss (Half-Bridge Operation at $T_J = 25^\circ\text{C}$)



Switching Power Loss (Half-Bridge Operation at $T_J = 125^\circ\text{C}$)



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