

High Voltage SLA6820M and SMA6820MP Series Driver ICs for 3-Phase DC Motor Applications

Introduction

The SLA6820M and SMA6820MP Series power packages incorporate all of the necessary power control components to configure the main circuit of an inverter power module (IPM). These products are especially suitable for driving the inverters of low-capacity motors, such as those used in 100 to 200 V fans for air conditioners.

Features and benefits include the following:

- Built-in pre-driver ICs and three bootstrap diodes as a high-side drive power supply
- CMOS-compatible input (5 V)
- High-side gate driver using bootstrap circuit or floating power supply
- One pin for 7.5 V regulator output
- Built-in protection circuit for controlling power supply voltage drop (UVLO)
- Built-in overtemperature detection circuit (TD)
- Fault signal output during operation of protection circuit
- Output current up to 2.5 A continuous
- Small SIP (SLA and SMA, 24 pins)

Functional Description

The functional block diagram is shown in figure 2. High voltage power and 15 VDC are input between VBB and LS1/LS2, between VCC1 and COM1, and between VCC2 and COM2. The on/off signals of the power MOSFETs are operated by six signals: HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3. These input signals are positive logic (the MOSFET turns on at $V_{xINx} = \text{high}$). The boot capacitors are connected between VB1 and U, VB2 and V, and VB3 and W1, as the high voltage power source.

Product Lineup

Type	MOSFET Rating	Input Voltage (VAC)	Heatsink Pad
SLA6826M	250 V / 2 A	120	Yes
SLA6827M	500 V / 1.5 A	230	Yes
SLA6828M	500 V / 2.5 A	230	Yes
SMA6821MP	250 V / 2 A	120	No
SMA6822MP	500 V / 1.5 A	230	No
SMA6823MP	500 V / 2.5 A	230	No

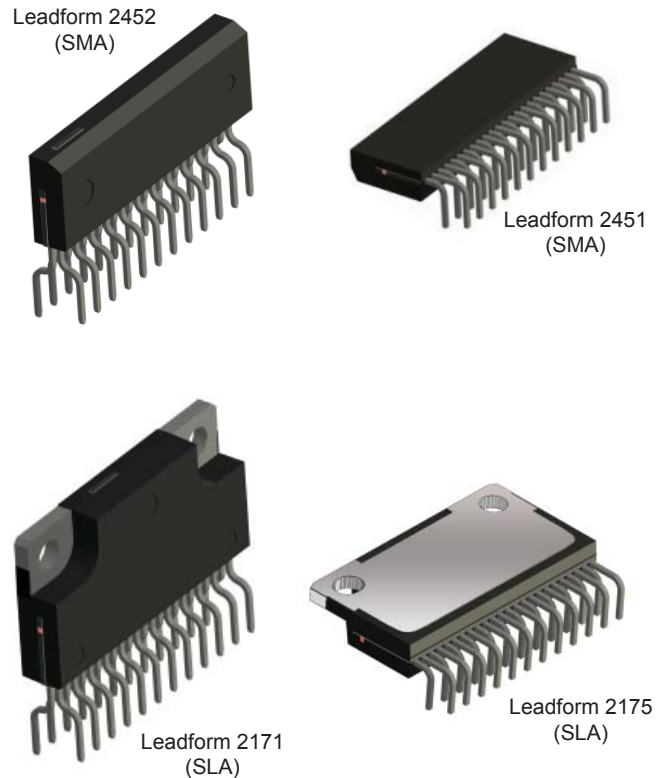


Figure 1. SLA6820M and SMA6820MP Series packages are fully molded SIPs, offering compact configurations both horizontal mount (leadforms 2451 and 2175) and vertical mount (leadforms 2452 and 2171). The SLA packages feature an aluminum heatsink pad for mounting external heatsinks.

Contents

Introduction	1
Functional Description	1
Protection Functions	7
Application Circuit Recommendations	10
Electrical Characteristics Data	10

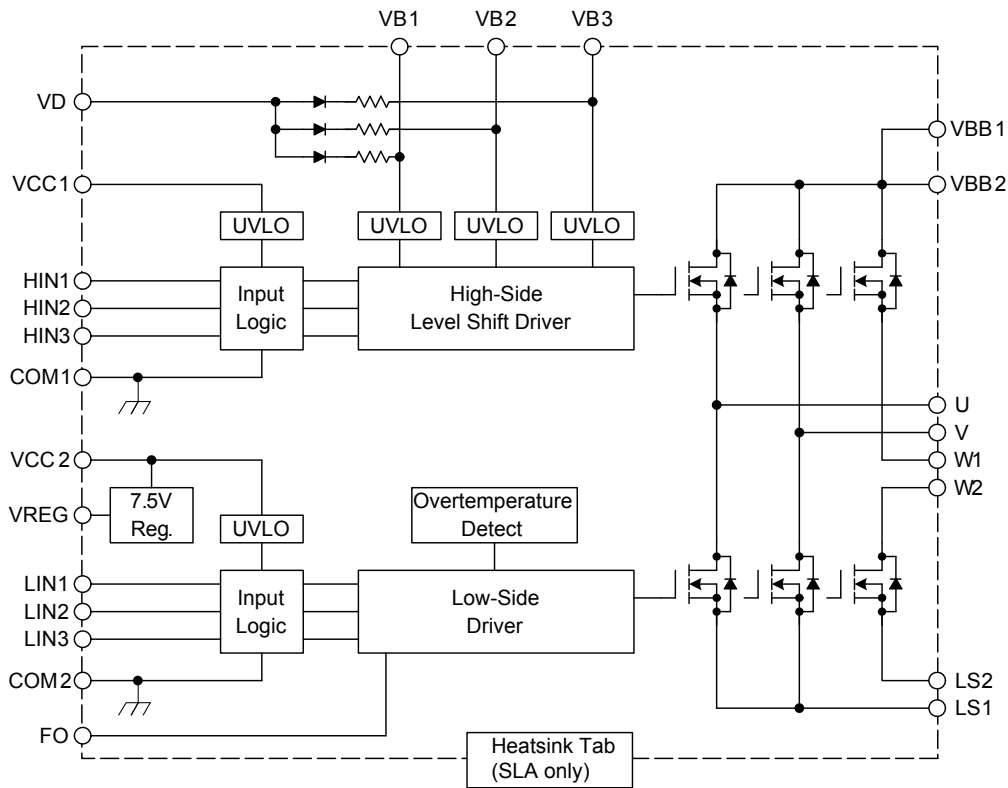


Figure 2. SLA6820M and SMA6820MP Series Functional Block Diagram. These devices support high-side and low-side three-phase MOSFET output drivers.

Terminal List

Number	Name	Function
1	VB1	High-side bootstrap terminal (U phase)
2	VB2	High-side bootstrap terminal (V phase)
3	VD	Bootstrap diodes anode terminal
4	VB3	High-side bootstrap terminal (W phase)
5	VCC1	High-side logic supply voltage
6	COM1	High-side logic GND terminal
7	HIN3	High-side input terminal (W phase)
8	HIN2	High-side input terminal (V phase)
9	HIN1	High-side input terminal (U phase)
10	VBB1	Main supply voltage 1 (connect to VBB2 externally)
11	VBB2	Main supply voltage 2 (connect to VBB1 externally)
12	W1	Output of W phase (connect to W2 externally)
13	V	Output of V phase
14	W2	Output of W phase (connect to W1 externally)
15	LS2	Low-side emitter terminal (connect to LS1 externally)
16	VREG	Internal regulator output terminal
17	LS1	Low-side emitter terminal (connect to LS2 externally)
18	LIN3	Low-side input terminal (W phase)
19	LIN2	Low-side input terminal (V phase)
20	LIN1	Low-side input terminal (U phase)
21	COM2	Low-side GND terminal
22	FO	Overtemperature and low-side UVLO fault-signal output
23	VCC2	Low-side logic supply voltage
24	U	Output of U phase
Tab	-	(SLA only) Electrically isolated heatsink/external heatsink mounting tab

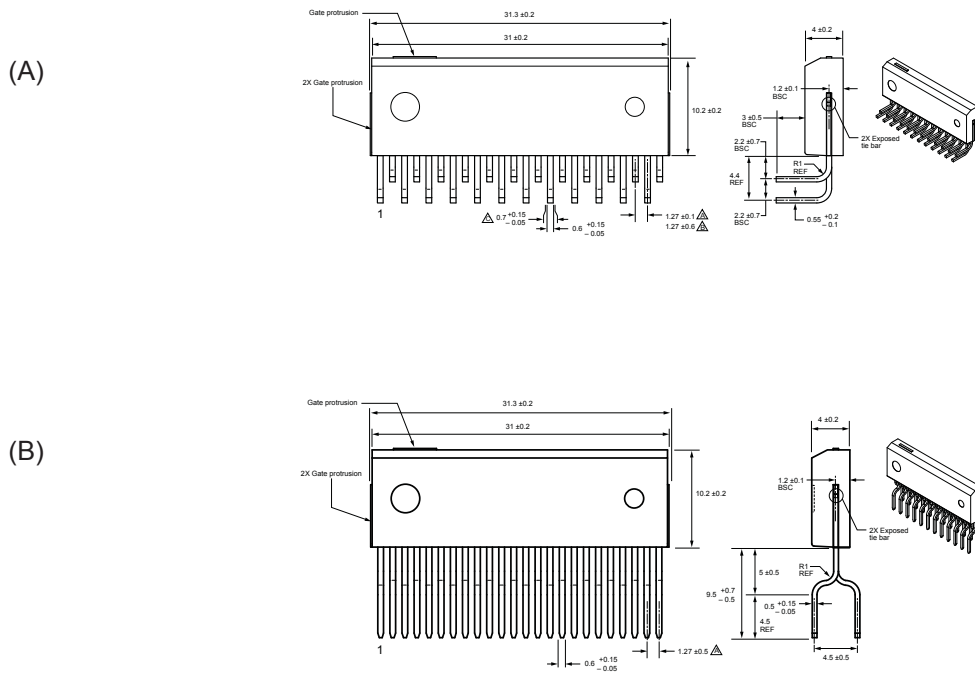


Figure 5. Package Outline Drawings. (A) LF2451, L-bend horizontal mount, (B) LF2452, vertical mount.

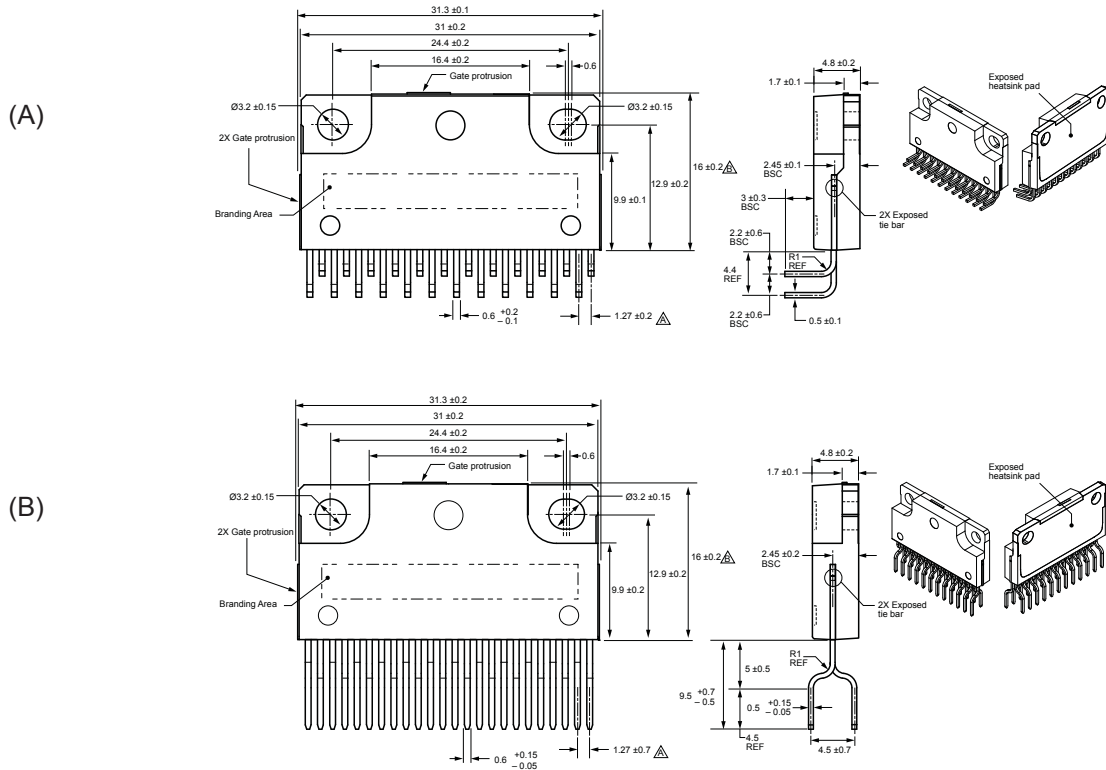


Figure 6. Package Outline Drawings. (A) LF2175, L-bend horizontal mount, (B) LF2171, vertical mount.

SW Frequency (kHz)	Recommended Capacitor Value (μF)
3	2.2
5	1
10	0.47
20	0.22

For two-phase modulation, or 120°C current-carrying topology, several tens of times the values above would be required due to the longer on-time.

Please select capacitors considering the conditions used. When starting-up the IC, the low-side must be turned on first, and the boot capacitor needs to be charged sufficiently. The adequacy of the values shown above needs to be validated by testing in the actual application. Because the VB1, VB2, and VB3 pins connect to UVLO circuits, these terminal voltages must be set such that the UVLO protection does not operate.

VCC1 and VCC2 These are the IC logic supply terminals for the built-in pre-driver IC. VCC1 and VCC2 must be connected together externally on the application PCB. To avoid improper operation because of supply ripples or other factors, a ceramic capacitor of approximately 0.1 μF must be installed near the pins.

Also, there is the possibility of permanent damage to the IC if a voltage greater than 20 V is applied to the IC. To protect against this, adding a Zener diode ($V_Z = 20$ to 23 V) is recommended.

VCC1 and VCC2 have a built-in UVLO circuit, so these terminal voltages need to be regulated within the rated range, so that the UVLO protection does not operate.

COM1 and COM2 These are the logic ground terminals for

the built-in pre-driver IC. COM1 and COM2 must be connected together externally on the application PCB. Varying electric potential may become a cause of improper operation, so careful attention is required to the design of connection points and minimizing the length of the PCB traces.

HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3 These are the input terminals for controlling driver output to the motor. The IC uses a 5 V, CMOS Schmitt trigger circuit configuration. The input logic is active high, and internal pull-down resistors are provided. The value for the pull-down resistors is 100 k Ω on both the HIN side and the LIN side, as shown in figure 7, but an additional input filter (RC filter) or pull-down resistor should be considered in case the application has excessive noise or the input voltage is unstable.

VBB1 and VBB2 These are the main power supply terminals. The VBB1 and VBB2 terminals are connected internally, but it is recommended to also tie them together externally by a short-circuit connection on the PCB, in order to decrease wiring impedance. A snubber capacitor (0.01 μF) should be placed near each of VBB1 and VBB2, connecting to the corresponding COM terminal, for suppressing surge voltages.

LS1 and LS2 These are source terminals for the low-side MOSFETs. LS1 and LS2 must be connected together externally on the PCB. When connecting a shunt resistor to these terminals, such as for overcurrent sensing, the length of the trace between the IC terminals and the shunt resistor must be as short as practicable. Greater length increase the susceptibility to improper operation due to noise.

VREG This is the terminal for the 7.5 V / 35 mA output to an external current regulator. Using an external regulation function is an important consideration for stabilizing the supply voltage.

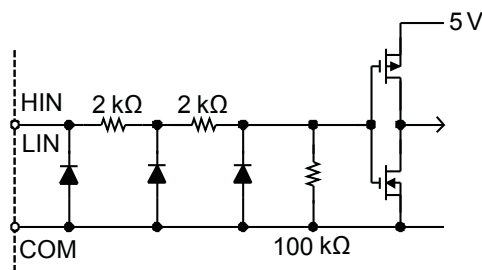


Figure 7. HINx and LINx Terminals Internal Equivalent Circuit

This could include placing an electrolytic capacitor between VREG and COM for avoiding supply ripple, and placing a ceramic capacitor for noise protection. If an external regulator is not required, VREG can be left open.

FO This is the fault signal output terminal used to indicate abnormal operation. Its internal circuit is shown in figure 8. The output logic is shown in the following table

	Overtemperature Detection (TD)	Logic Supply Undervoltage Detection (UVLO VCC2 to COM2)
FO Output	Yes	Yes
IC Shutdown	No	Yes

It outputs a 5 V signal at overtemperature detection (TD) or a UVLO condition between VCC2 and COM2. When a UVLO condition is in effect, the IC shuts down output on the low side, at the same time FO output occurs. When a TD condition occurs, the FO output occurs, but there is no shutdown of the low-side output. The response to a TD condition must be handled by the application system logic. For example, the FO signal could be input into the application microprocessor, which could then turn off the gate control inputs to the IC.

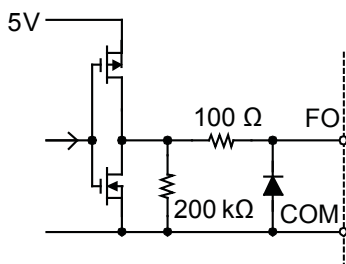


Figure 8. FO Terminal Internal Equivalent Circuit

Protection Functions

This section describes in detail the various device protection features provided in these devices.

Undervoltage Lockout (UVLO) of Control Power Supply

When the gate-driving voltages on the output MOSFETs become too low, the losses of the power MOSFETs increase, and in the worst case the circuits may be damaged. In order to prevent this, undervoltage protection circuits are built into the control power supply.

The high-side driver IC monitors the voltage between VCC1 and COM1, the voltage between VB1 and U, VB2 and V, and VB3 and W. The low-side driver IC monitors the voltage between VCC2 and COM2.

As shown in the timing charts (figure 10), the UVLO functions monitor VB voltage, and if it falls below the V_{UVHL} voltage level, the high-side MOSFETs will be shut down. Similarly, if the VCC1 to COM1 voltage falls below the V_{UVHL} voltage level, the high-side MOSFETs will be shut down. Subsequently, when the supply voltage rises and exceeds V_{UVHH} , the IC resets automatically and resumes outputs according to the input command signal (HIN).

On the low side, if the VCC2 to COM2 voltage falls below the V_{UVLL} voltage, the low-side MOSFETs will be shut down and the FO output goes high. When the supply voltage rises and exceeds the V_{UVLH} voltage level, the low-side MOSFETs will be released from shut down, and the FO output goes low. Subsequently, the low side operates according to the input command signal (LIN).

Overtemperature Detect Function The devices have a built-in overheating detection (TD) circuit. If the device overheats abnormally (exceeds T_{DH}), it outputs 5 V to the FO terminal. The IC does not, however, shut down the output MOSFETs automatically. Instead, the application system logic should respond to the FO output and transmit shutdown commands on the control signals (HIN1, HIN2, and HIN3 and LIN1, LIN2, and LIN3).

When the device temperature falls below the T_{DL} level, the TD shutdown is released. The TD function parameters are as follows:

	Min (°C)	Typ (°C)	Max (°C)
T_{DH}	135	150	185
T_{DL}	105	120	135
T_{Dhys}	25	30	35

T_{Dhys} (Overtemperature Detect Hysteresis) is the difference between T_{DH} and T_{DL} .

This TD function is not intended to completely protect the internal MOSFETs or driver logic ICs. The application logic should monitor temperature conditions, and be designed to minimize the delay to response, particularly in the case of a rapid current increase.

External Regulator Function The devices have a built-in external regulator (7.5 V / 35 mA) output. The fundamental characteristics of the regulator are shown in figure 9.

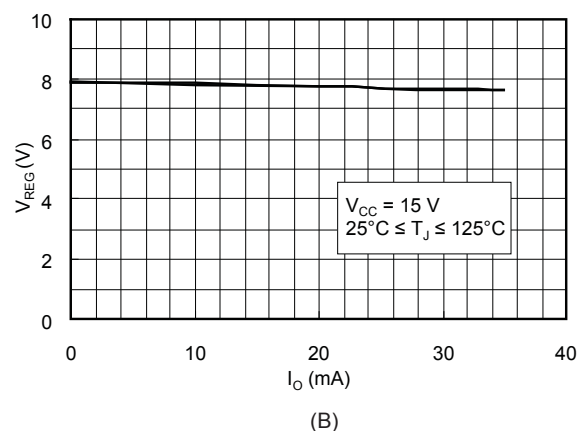
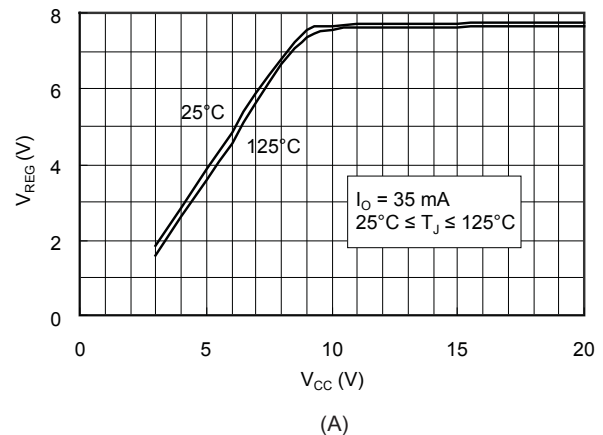


Figure 9. External Regulator Characteristics: (A) line regulation, and (B) load regulation

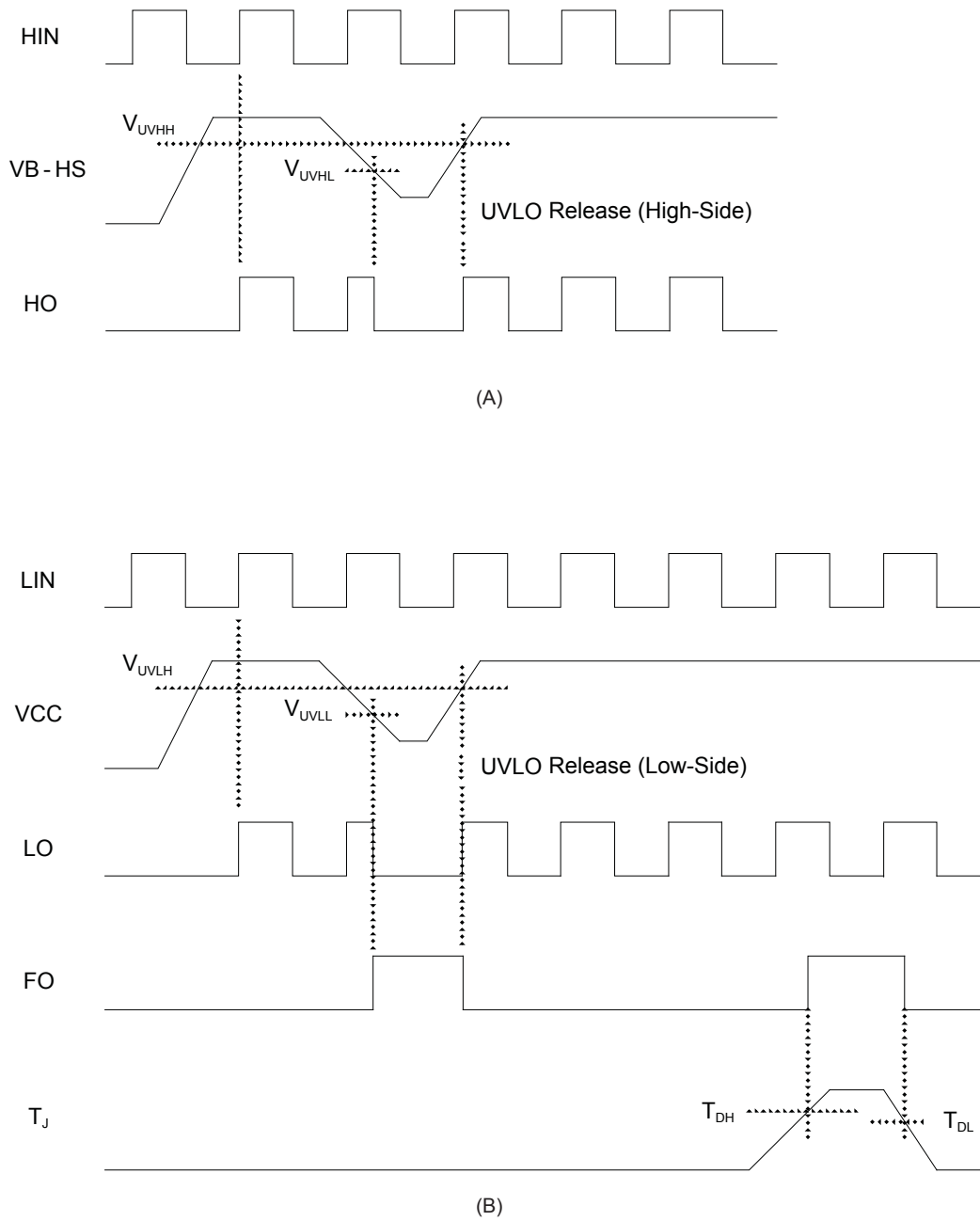


Figure 10. UVLO Protection Circuit Timing (A) high-side, (B) low-side

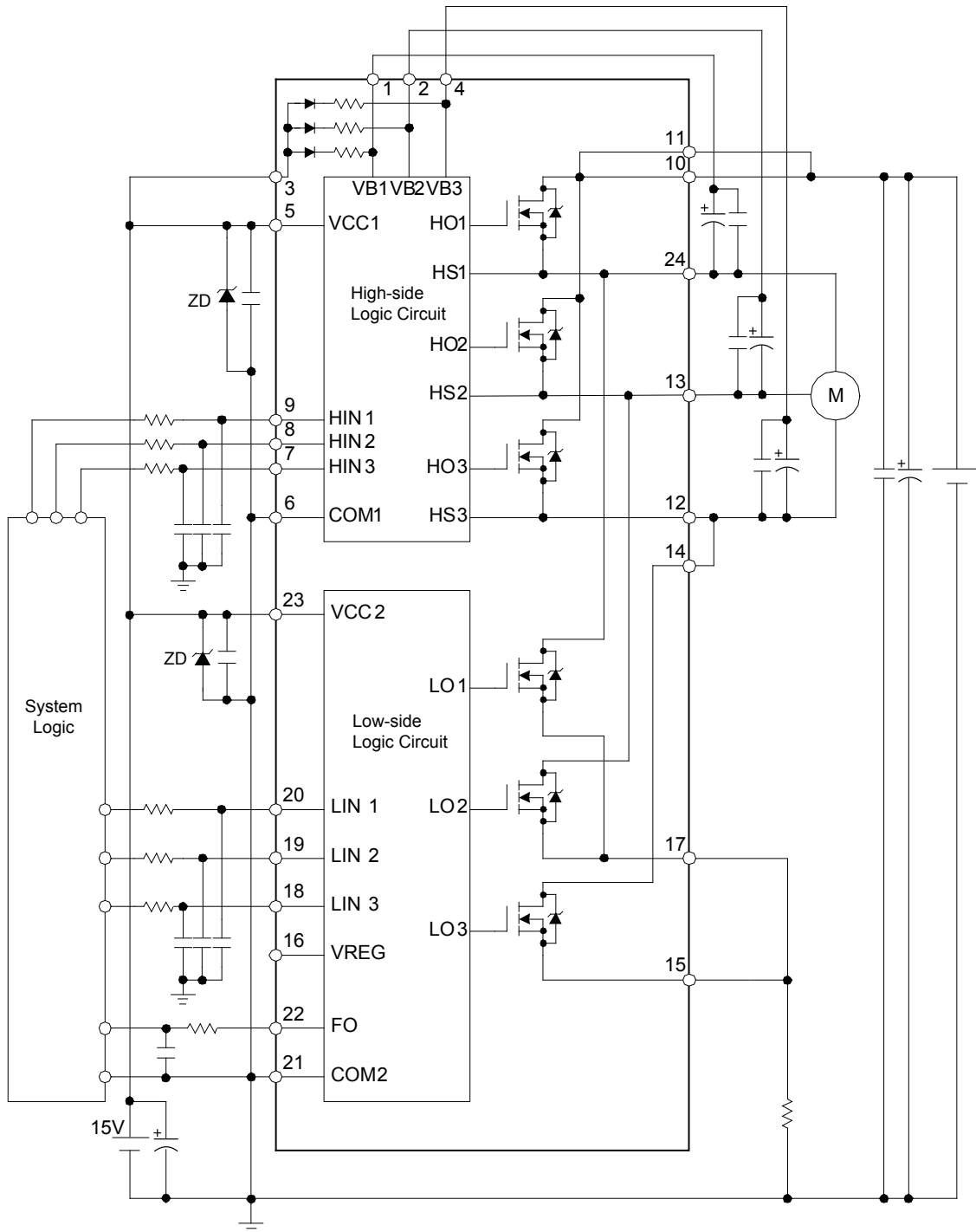


Figure 11. Typical Application

Application Circuit Recommendations

When designing application circuits using these devices, the following should be taken into consideration:

Supply Sequence The load power supply does not have to be provided in any particular sequence. However, commands should not be transmitted on the sequencing signal input terminals, HIN and LIN, until after the logic control power supply, VCC, has reached steady state.

Short Circuit Protection There is no built-in protection circuit against short circuits through the outputs to ground. The application circuit logic should be designed to monitor outputs to detect a short circuit condition.

Pin to Pin Distance The device packages have 24 pins, and a 1.27 mm pin pitch. At operating voltage levels, there may be insufficient creepage and clearance distance, and conformal coating or encapsulation of the application printed board assembly is recommended.

Surge Protection Each terminal should be protected against power surges by isolation using an external component such as a ceramic capacitor or Zener diode. Power surges that impinge on the device may cause critical damage to the IC as well as faulty operation.

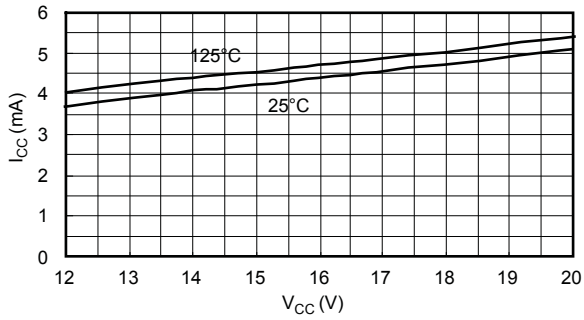
Input Blanking Time In order to avoid a high-side to low-side short-circuit, the HIN and LIN signals must never be in phase. The blanking time, t_{BLANK} , or dead-time, is the delay between rising edges on the HIN and LIN signals. It must be controlled externally by the application system logic, as it is not set internally. A t_{BLANK} of more than 1.5 μs is recommended.

Electrical Characteristics Data

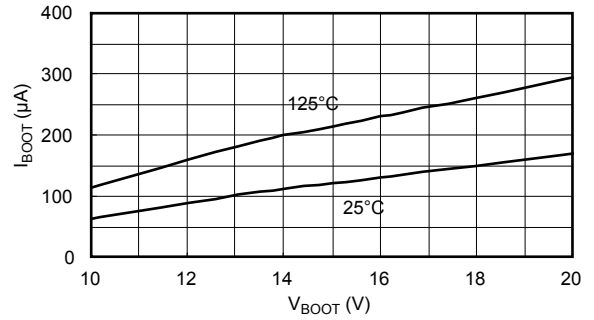
The following pages contain characteristic performance data. The information shown applies to all models of the SLA6820M/SMA6820MP series, unless otherwise specified.

All SLA6820M and SMA6820MP Series Devices

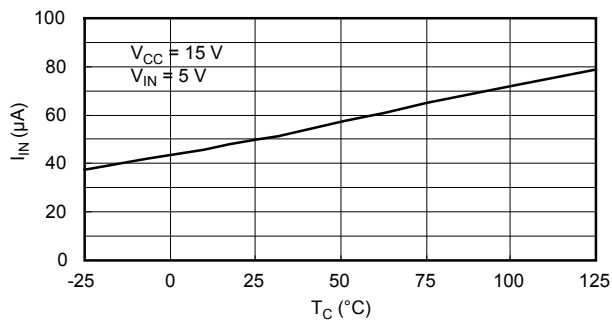
Supply Current versus Supply Voltage



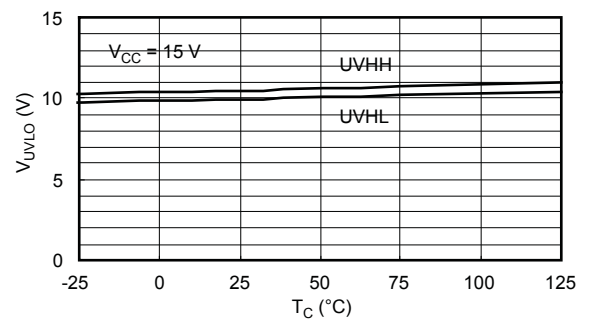
Bootstrap Current versus Bootstrap Voltage



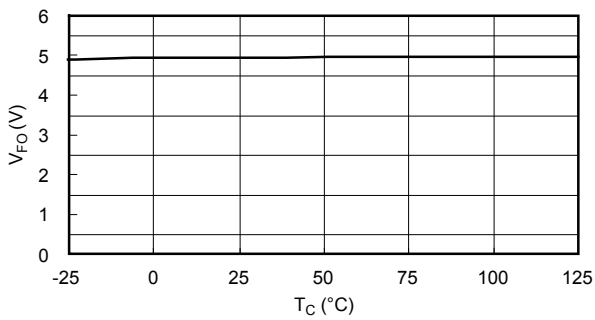
I_{IN} Current versus Case Temperature



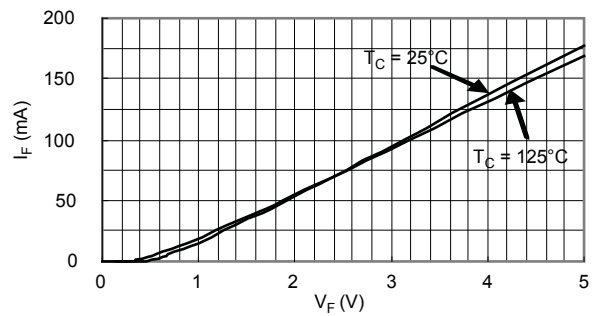
UVLO Voltage versus Case Temperature



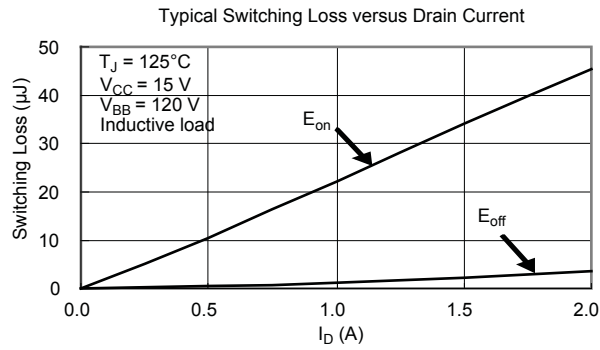
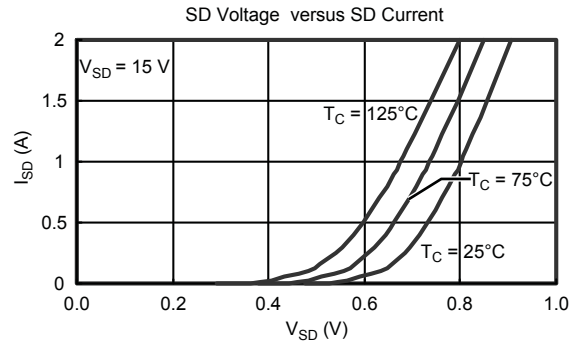
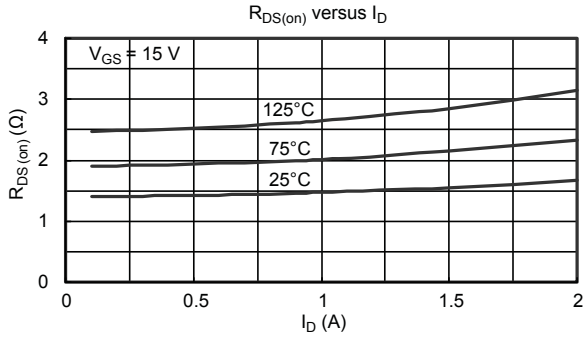
FO Voltage versus Case Temperature



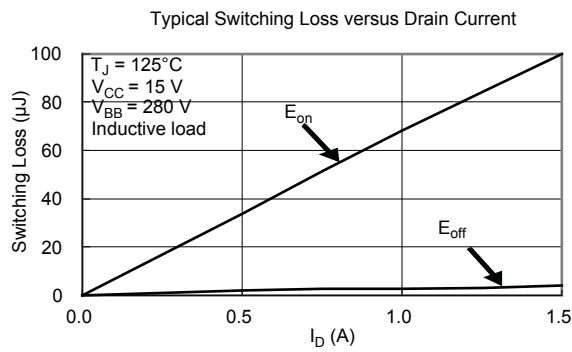
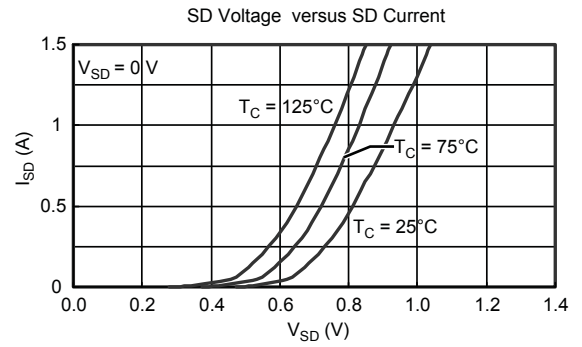
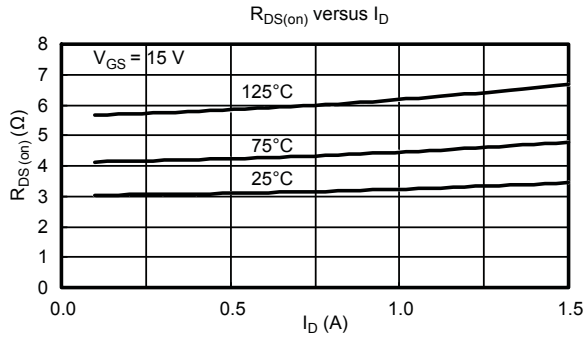
Boot Diode Forward Current versus Forward Voltage
Includes series resistance



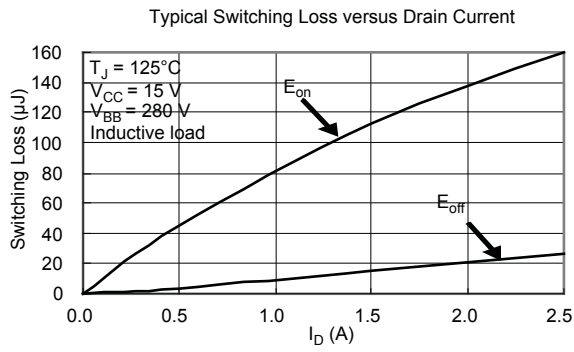
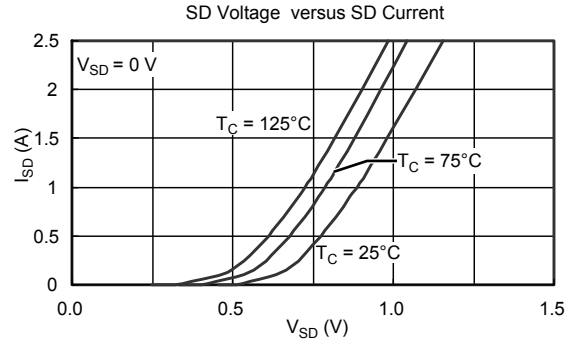
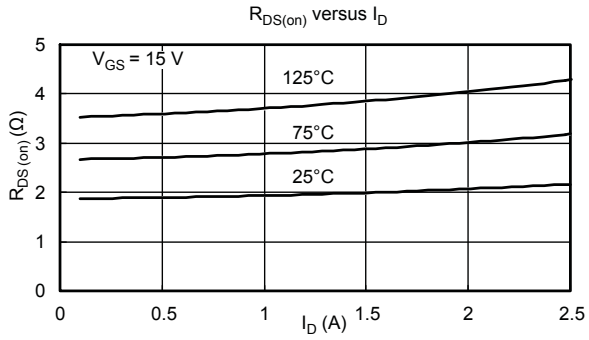
SLA6826M/SMA6821MP MOSFET Characteristics



SLA6827M/SMA6822MP MOSFET Characteristics



SLA6828M/SMA6823MP MOSFET Characteristics



All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

The products described herein are manufactured in Japan by SanKen Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

SanKen and Allegro reserve the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Therefore, the user is cautioned to verify that the information in this publication is current before placing any order.

When using the products described herein, the applicability and suitability of such products for the intended purpose should be reviewed at the users responsibility.

Although SanKen undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.

Users of SanKen products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.

SanKen products listed in this publication are designed and intended for use as components in general-purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Their use in any application requiring radiation hardness assurance (e.g., aerospace equipment) is not supported.

When considering the use of SanKen products in applications where higher reliability is required (transportation equipment and its control systems or equipment, fire- or burglar-alarm systems, various safety devices, etc.), contact a company sales representative to discuss and obtain written confirmation of your specifications.

The use of SanKen products without the written consent of SanKen in applications where extremely high reliability is required (aerospace equipment, nuclear power-control stations, life-support systems, etc.) is strictly prohibited.

The information included herein is believed to be accurate and reliable. Application and operation examples described in this publication are given for reference only and SanKen and Allegro assume no responsibility for any infringement of industrial property rights, intellectual property rights, or any other rights of SanKen or Allegro or any third party that may result from its use.

Anti radioactive ray design is not considered for the products listed herein.