

Applications Information

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Closed-Loop Speed Control for the A3932/A3936

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A low-cost speed control circuit can be implemented by the addition of a few components to provide closed-loop speed control of 3-phase brushless dc motors using the A3932 or A3936. This solution avoids the need for relatively expensive tachometers and requires very little additional board area.

A block diagram of the solution is shown in the figure below. A schematic diagram of the full solution, using an A3932, is shown at the end of this document. The schematic is configured for an 8-pole 2.5 A motor running at speeds in the range of 1500 rpm to 3000 rpm, with varied loads, from no load (V_{BB} current = 120 mA) to a heavy load (V_{BB} current = 1.0 A).

With the extensive feature content of the A3932/A3936 and the flexibility of the speed control circuit, this solution can be used in a myriad of applications where accurate speed control is necessary.

Operating Description

The speed control circuit processes the TACH signal from the A3932/A3936, compares it against a reference voltage, and then produces an appropriate PWM signal to the A3932 (ENABLE signal for the A3936), which controls the A3932/A3936 drivers.

The TACH signal provided from the A3932/A3936 produces a pulse on every Hall transition. This signal is level-shifted from 5 V to V_{REG} and is “pulse-stretched” using a monostable. The pulse-stretched signal is then compared against a speed-reference voltage to produce a speed error signal. The

error signal is used to determine the duty cycle/switching frequency of a fixed off-time pulse width modulator. The resulting signal is level-shifted to 5 V, and fed into the PWM input of the A3932 (ENABLE input for the A3936).

This PWM signal controls the current through the drivers. Therefore, the motor torque is also controlled as $T \propto I$. This torque then accelerates or decelerates the motor to control the speed.

The Pulse Stretching and Fixed Off-Time PWM circuit blocks are provided by a 556 timer IC, which is effectively two 555 timers. For convenience, the VREG supply on the A3932 can be used to power the 556 timer and the error amplifier. In the case of the A3936, an external supply has to be used. More information on using VREG is given in the section Other Considerations.

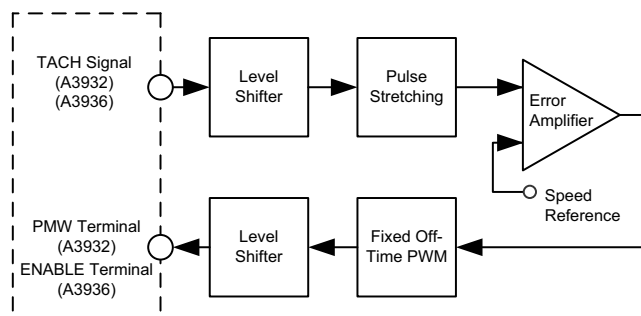
Component Selection

In this section, each block is described in turn, along with considerations for selecting components to use for that block.

TACH-Side Level Shifter. This is a simple transistor circuit, Q1, that converts the TACH signal from a 5 V level to the V_{BB} level, and introduces a signal inversion for correct edge-triggering on the monostable that follows in the circuit. To prevent potential mistripping of Q1 due to PWM switching noise, etc., the threshold switching level of Q1 is increased through the addition of R3. To avoid distorting the waveform in high-noise environments, a small capacitor could be added in parallel with R3.

Pulse Stretcher. This block operates as a monostable, triggered on the negative edge of the TACH signal. The duration of the pulse should be less than one electrical commutation. The timing components can be defined from the following:

- 3000 rpm = 50 rev/sec, therefore, one revolution takes 20 ms
- 8 magnetic poles and 3 phases means that there are 24 electrical commutations per mechanical revolution
- 24 electrical commutations occur in 20 ms, therefore, each electrical commutation lasts for a minimum of 833 μ s
- pulse width duration $t_{WD} = 1.1 \times R5 \times C2$



Speed control block diagram

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In this case, t_{WD} was selected to be 650 μ s and C2 chosen to be 22 nF, making $R5 = 27$ k Ω .

Error Amplifier. This block is configured as a type 1 integrator to obtain a high dc gain for good speed accuracy and a bandwidth lower than the natural frequency of the motor. It is important to ensure that the amplifier has a low output ripple to prevent mistriggering in the PWM stage.

The components were selected to give reasonable settling time with minimum oscillation. For this example, a crossover frequency (0 dB) of 1.5 Hz yielded a good result.

Fixed Off-Time PWM. Operates as an astable with variable duty cycle (frequency) depending on the error voltage appearing on the control pin. The off-time remains constant.

The off-time can be determined by: $t_{off} = 0.693 \times R8 \times C5$.

To achieve good control, it is recommended that the PWM frequency be considerably higher than the commutation frequency. In this case, t_{OFF} was selected to be 12 μ s and C5 to be 2.2 nF, making $R8 = 8.2$ k Ω .

The on-time depends on the values of R7, R8, and C5, as well as the value of the error voltage. The value of R7, in this case 120 k Ω , was optimized in the loop to set up the correct dynamic range of the speed control circuit.

PWM-Side Level Shifter. (On the A3932; ENABLE-side for the A3936.) Converts the PWM signal from a VREG

level to a TTL level. If R10 is selected to be 10 k Ω , then:

$$R9 = (13/5 - 1) \times 10 \text{ k}\Omega = 16 \text{ k}\Omega$$

Results

The results are presented in six waveform plots on the next page. The conditions are summarized in the Test Conditions table.

At a constant voltage $V_{BB} = 24$ V, two different loads were applied: no load (V_{BB} current = 120 mA), and what would be considered a heavy load (V_{BB} current = 1 A). Two motor speeds were used: 3000 rpm (maximum speed) and 1500 rpm.

Plots 1 and 2 have the same speed, but Plot 2 has a higher load. It can be seen that, with the increased load, the error amplifier responds by increasing output (the lowest trace, channel 4), thus widening the duty cycle. The expanding duty cycle in turn increases current (channel 2), and increases torque (channel 1) in order to maintain constant speed (where the commutation period is held at a constant 840 μ s).

The same conditions are maintained for Plots 3 and 4, which were made using an expanded time dimension to see the individual PWM cycles. In these plots, the pulse measurement (channel 3) is taken at the input to the A3932 PWM signal.

Plot 4 has a higher load (channel 2) than Plot 3. From these waveforms, it can be seen that the PWM duty cycle (channel 3) in Plot 4 is wider in comparison with Plot 3, and the frequency reduced. This is the result of having a fixed off-time (the low limit of channel 3). It can be seen that the PWM fixed off-time is maintained at a constant 12 μ s, with the on-time (the high limit of channel 3) varying between 22 μ s (Plot 3) and 32 μ s (Plot 4). The corresponding PWM switching frequencies are 29.4 kHz and 22.7 kHz.

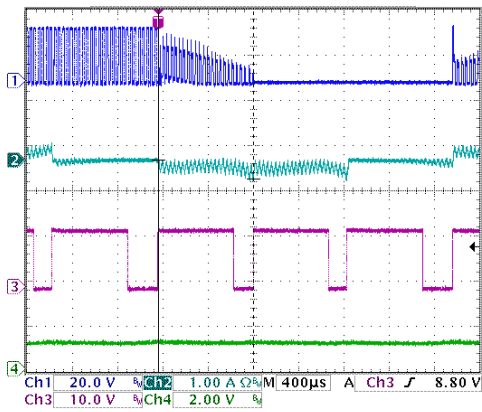
Plots 5 and 6 are similar to Plots 1 and 2, except for the speed being halved to 1500 rpm. Note that as the speed has decreased, the output of the error amplifier (channel 4) also has decreased. This reduces the PWM duty cycle (plots not shown), and thus reduces the motor current, torque, and motor speed. Again, it can be seen that constant speed is maintained when the load is increased.

Test Conditions

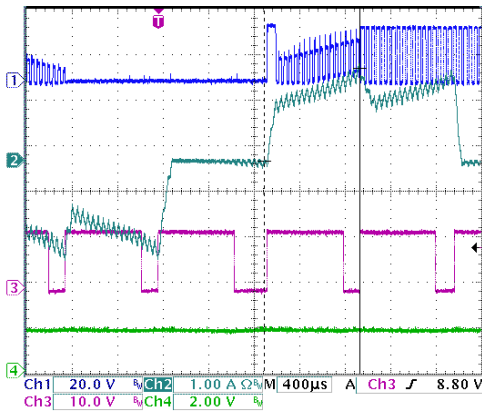
Plot	Pulse (Channel 3) Measured At	Load (mA)	Speed (rpm)
1	Pulse Stretcher Out	120	3000
2	Pulse Stretcher Out	1000	3000
3	PWM/ENABLE In	120	3000
4	PWM/ENABLE In	1000	3000
5	Pulse Stretcher Out	120	1500
6	Pulse Stretcher Out	1000	1500

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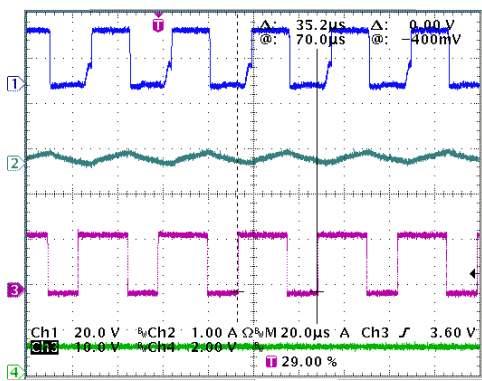
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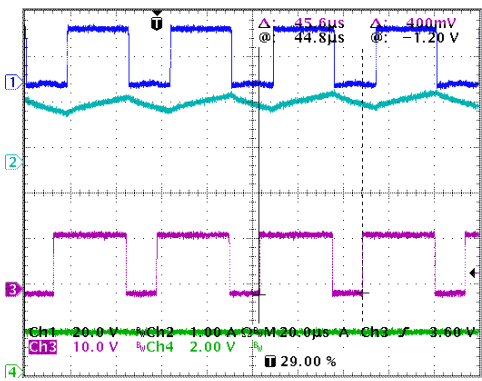
Plot 1: No Load, Maximum speed
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- 'stretched' TACH pulse Ch4- error amplifier output



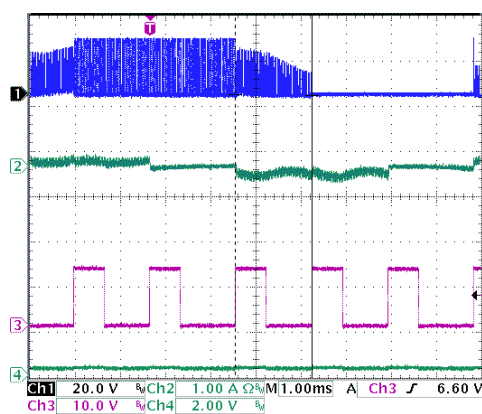
Plot 2: Heavy Load, Maximum speed
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- 'stretched' TACH pulse Ch4- error amplifier output



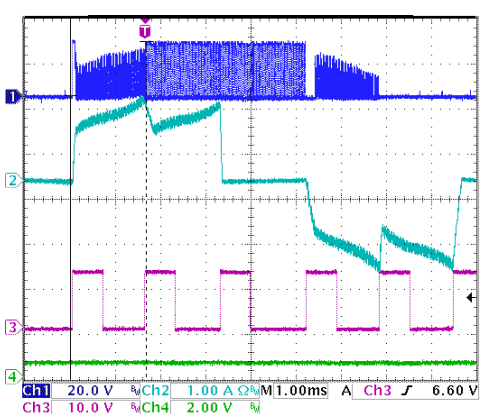
Plot 3: No Load, Maximum speed, Zoom on PWM
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- PWM signal Ch4- error amplifier output



Plot 4: Heavy Load, Maximum speed, Zoom on PWM
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- PWM signal Ch4- error amplifier output



Plot 5: No Load, Half speed
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- 'stretched' TACH pulse Ch4- error amplifier output



Plot 6: Heavy Load, Half speed
 Ch1- motor winding voltage Ch2- motor winding current
 Ch3- 'stretched' TACH pulse Ch4- error amplifier output

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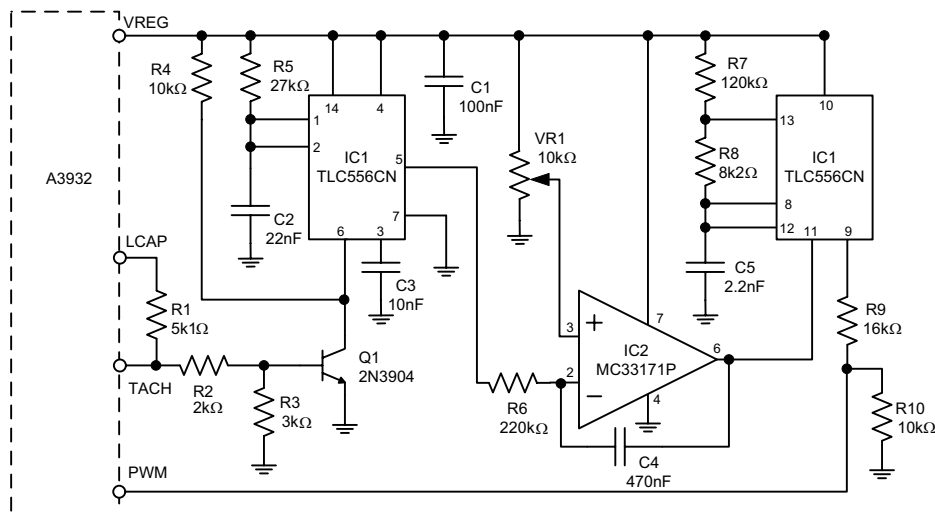
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Other Considerations

- In the above example, a type 1 integrator solution was used as it provides high gain at dc and reasonable component values can be chosen to close the control loop at low frequencies. When “closing the loop” with the amplifier, it is important to ensure a balance between preventing the loop response being over-damped (long response to changes in either speed or load) and the loop response being under-damped (causing transient speed oscillations in the motor due to speed or load changes). In solutions where very high dc gains and low bandwidths are required, it may be necessary to use two amplifiers, one for producing a high gain error signal and the other amplifier for introducing the correct control shaping.
- Also in the example, the stretched pulse was set to around 80% of the commutation period. The reason for such a wide pulse is that it blanks out any erroneous TACH signals and it provides more dynamic range in the control loop when applying wide ranging loads. However, in certain applications, for example, where a small motor with low inertia is used, the run-up time can be faster than the loop can respond. This means that the wide stretched pulse can blank some of the commutations, making the loop think it is running slower than it actually is. In this case, a smaller stretched pulse should be used.

- There are a few points worth noting when using the VREG supply of the A3932:
 - The maximum current that can be drawn from the VREG supply is 30 mA, which should provide sufficient drive current for the external MOSFETs and the speed control circuit.
 - A CMOS version of the 556 timer is recommended, to minimize current consumption. With the values used in the schematic diagram, the VREG current for the speed control circuit was measured at approximately 5 mA.
 - Because of the additional current drawn by the speed control circuit, it is important to consider the power dissipation in the linear regulator, especially in applications where high V_{BB} values are used. For example, with a $V_{BB} = 50$ V, the additional power dissipated due to the speed control circuit would be approximately 250 mW.
 - VREG is only regulated to 13 V when V_{BB} is above 18 V. If V_{BB} is less than 18 V, $V_{REG} = V_{BB} - 2.5$ V.
 - High frequency switching noise from V_{BB} can appear on VREG. Attention must be given to both good layout practice and filtering to ensure that none of the timers mistrigger.
- When using the A3936, an external supply must be used to power the speed control circuit.

Schematic Diagram of Speed Control Circuit for A3932



Reference	Manufacturer	Part Number
IC1	Texas Instruments	TLC556CN
IC2	Motorola	MC33171P

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