Product Description

STR-A6100 Series Flyback Switching Regulators

Introduction

The STR-A6100 series integrates a PRC (fixed off-time) control IC and a MOSFET with avalanche guarantee. These elements allow power supply system designs that are highly reliable and simple, with fewer peripheral components. These ICs also provide Auto Standby mode operation, lowering input power requirements at light loads, and improving efficiency over the entire load range and universal input range.

Note: PRC stands for Pulse Ratio Control (on-pulse-width control with fixed off-time).

The off-time of the STR-A6100 series is shown in table 1, on the next page.

Figure 1. The STR-A6000 series is provided in fully-molded mini DIP-8 packages, with one pin removed for improved isolation.

Features

- Small size (8-pin DIP) fully-molded package (suitable to low-profile SMPS)
- Built-in avalanche-energy-guaranteed power MOSFET (to simplify surge-absorption circuit; no V_{DSS} derating is required.)
- Built-in start-up circuit (to alleviate power loss by cutting the circuit off after the start-up)
- Auto Standby mode (to realize $P_I \leq 0.1$ W at no load)
- Auto bias function (stable burst operation with no affect from transformer), except STR-A6153E
- Built-in constant-voltage drive circuit, which is not affected by V_{CC}
- Low circuit current in non-operation (circuit current before start-up), $I_{CC(OFF)} = 50$ µA (max)
- Two operational modes by auto-switching functions
  - In normal operation: PRC mode (on-pulse-width control with fixed off-time)
  - In stand-by operation (at light load): burst oscillation mode (intermittent operation)
- Built-in leading-edge blanking function
- Various protection functions
  - Pulse-by-pulse overcurrent protection (OCP)
  - Overload protection (OLP) → auto restart
  - Overvoltage protection (OVP) → latch mode
  - Thermal shutdown (TSD) → latch mode

Terminal Functions

Start-up (Pin 5)

Figure 2 shows the external start-up circuit. The start-up pin can be directly connected to the rectified high DC voltage. Also, the pin is internally connected to the source of constant current (790 µA). At start-up, the source of constant current charges C2 through the VCC pin and the IC starts its operation when the VCC pin voltage reaches an operation start voltage ($V_{CC(ON)}$ = 17.5 V). After that, the source of constant current will

Contents

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

Table 1. Selection Guide

Part Number	MOSFET V_{DSS} (V)	$R_{DS(on)}$(Max) (Ω)	VAC Input (V)	P_{OUT}* (W)	Off-Time (µs)	Package
STR-A6131	500	3.95	100	13	8	DIP-8
			120	15		
STR-A6132	500	2.62	100	16		
			120	18		
STR-A6151	650	3.95	220	15		
			Wide	13		
STR-A6159	650	6	220	13		
			Wide	10		
STR-A6169	800	19.2	220	8		
			Wide	5		
STR-A6131M	500	3.95	100	13	11.5	
			120	15		
STR-A6151M	650	3.95	220	15		
			Wide	13		
STR-A6153E	650	1.9	220	22		
			Wide	18		
STR-A6159M	650	6	220	13		
			Wide	10		

*The listed output power represents thermal ratings, and the peak output power, P_{OUT}, is obtained by 120% to 140% of the thermal rating value. In case of low output voltage and narrow on-duty cycle, the P_{OUT} (W) becomes lower than the above.

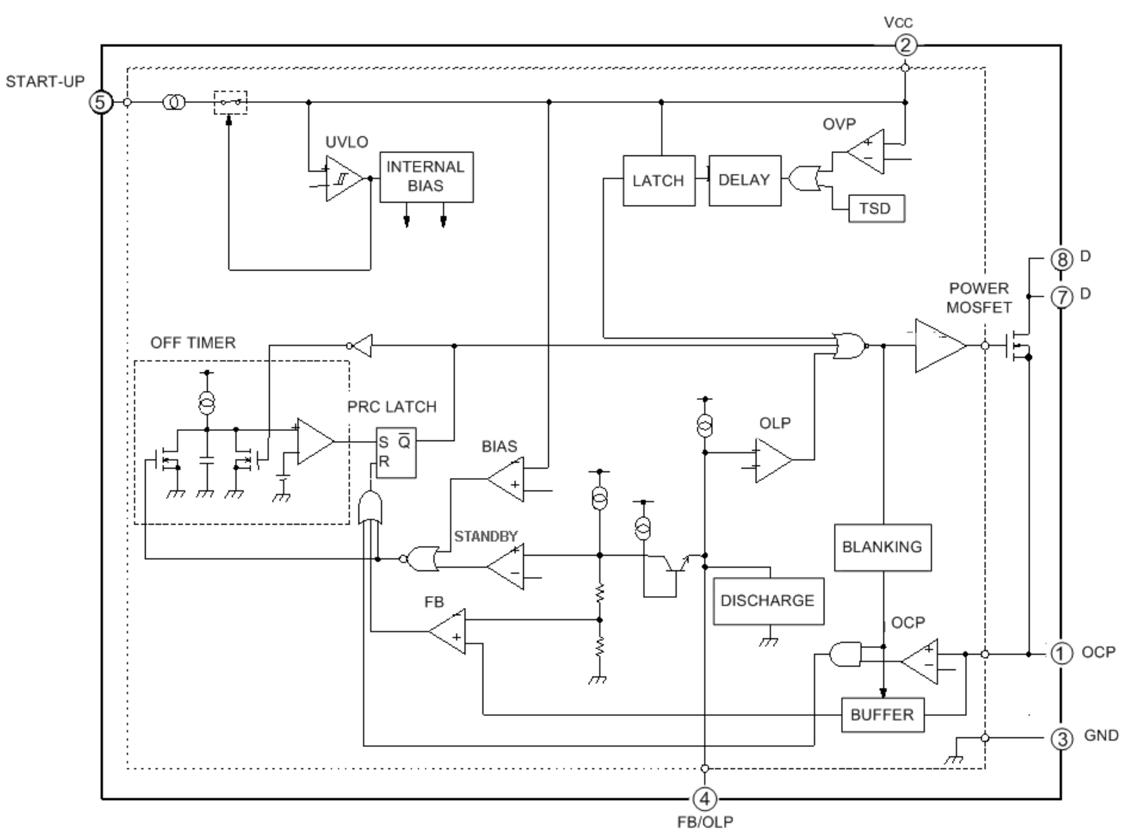

Figure 2. Functional block diagram

stop its operation and lower its power consumption to a few milliwatts. Start-up time in seconds depends on the source of constant current, obtained by the following formula. For example:

$$t_{start} = C2 \times (V_{CC(ON)} - V_{CC(INT)}) / I_{start}$$
$$= 22 \times 10^{-6} \times 17.5/(790 \times 10^{-6}) = 0.487$$

where C2 = 4.7 to 22 µF, recommended.

A default voltage of C2 is hypothesized as 0 V.

Note: R4 connected to the start-up pin is to prevent malfunction by external noise. 10 kΩ to 47 kΩ is recommended.

VCC (Pin 2)

Figure 4 shows a relationship between the V_{CC} voltage and the circuit current (I_{CC}). The I_{CC} is low until the control circuit starts its operation ($I_{CC(OFF)}$ = 50 µA at V_{CC} = 15 V, T_A = 25°C), but it goes up rapidly when the VCC pin voltage reaches $V_{CC(ON)}$ = 17.5 V and the IC starts up its operation. After that, the VCC pin voltage falls to $V_{CC(OFF)}$ = 10 V, the IC stops its operation and returns to the initial state.

Figure 5 shows the behavior of V_{CC} after start-up. As explained, the V_{CC} increases by an internal constant-current source, but it decreases for awhile after the IC starts its operation because the bias winding voltage does not go up enough to charge C2. V_{CC} keeps falling until the bias winding voltage exceeds the falling V_{CC}, then being able to charge C2 and supply power to the IC. Thereafter, V_{CC} is stabilized by the bias winding voltage.

Note: In order to avoid a start-up fault, either the C2 value or the bias winding voltage must be set so that the bottom of the V_{CC} can have a margin, not less than 1 V, against the operation-stop voltage of the $V_{CC(OFF)}$ (10 V).

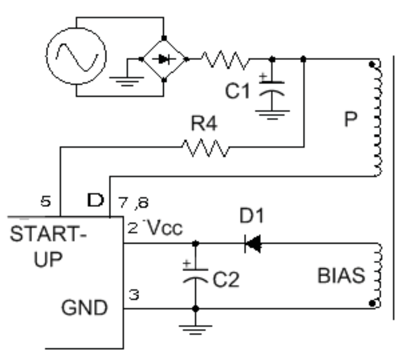

Figure 3. External start-up circuit

Bias Winding and R2 (Figure 6) The number of turns in the bias winding should be set so as to allow the $V_{CC(OFF)}$ = 10 V< V_{CC} < $V_{CC(OVP)}$ = 31.2 V. In general, the bias winding voltage is set between 15 V and 20 V.

As shown in Figure 6, in an actual power supply circuit, the V_{CC} is susceptible to the secondary load. This happens because the primary winding surge voltage is superimposed onto the bias winding, charging the C2 to the peak right after the MOSFET is turned off. In order to prevent C2 from charging, as shown in

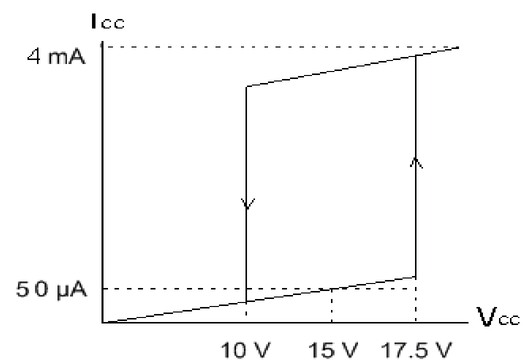

Figure 4. I_{CC} vs. V_{CC}

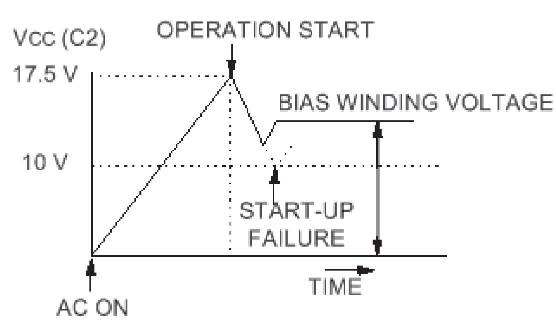

Figure 5. V_{CC} after start-up

figure 7, R2 is added. Because a surge voltage is dependent on the structure of the transformer, the winding position of the bias winding also needs to be examined carefully. Furthermore, the optimum value of the resistor should be verified on the bench, which is generally a couple of ohms to tens of ohms.

OFF timer and constant-voltage control (FB/OLP, Pin 4)

Figure 2 is a functional block diagram of the STR-A6100 device. Unlike PWM operation, the PRC mode of operation is based on a fixed off time and an on-width (or on-time) variation. The off-timer circuit inside the IC generates the fixed off-time of the MOSFET and the timing pulse signal for on starting. The on period starts right after the end of the fixed off-period, and terminates when the PRC latch circuit is reset by the on-period termination signal from the OCP or the FB comparator. Thereafter, the off-timer circuit starts its operation and shifts to off-period.

Figure 8 shows the operating waveforms for the capacitor voltage inside the off-timer circuit and for an OCP pin voltage. The OCP pin voltage is detected across R1. The internal capacitor is charged with a fixed slope. If the charged voltage reaches the reference voltage (to negative terminal side) of the comparator, the output ($\overline{Q}$) of the PRC latch turns "low". Immediately after this happens, the MOSFET turns on, and at the same time the capacitor is discharged rapidly down to 0 V and keeps the state. In this period, the output MOSFET stays on, and the drain current I_D runs through the external R1, generating a voltage with the same sawtooth waveform as I_D, the voltage being fed into the OCP pin (pin 1). This voltage is detected at pin 1, and when the voltage reaches the OCP threshold voltage V_{OCP} = 0.77 V, the OCP comparator resets the PRC latch. Then, the PRC latch output ($\overline{Q}$) turns "high" and the capacitor in the off-timer circuit shifts to constant-current charging. From this point of charging to the point of rapid discharge as described above, the off-time is fixed. Thus, when the PRC latch output ($\overline{Q}$) is "high", the output MOSFET turns off. The above-mentioned on-period determining operation by the OCP comparator works only during start-up. This operation continues until the IC shifts to a constant-voltage control operation mode after start-up. The FB comparator will be explained next because it relates to the on period, as well.

Figure 9 illustrates a circuit connecting a photocoupler to the FB/OLP pin and explains the feedback operation by the STR-A6100 series current-mode control. The photocoupler pulls the feedback current (I_{FB}), which is proportional to the signal of the secondary-side error-amplifier (inversely proportional to the secondary-side output voltage), out of the FB/OLP pin. This

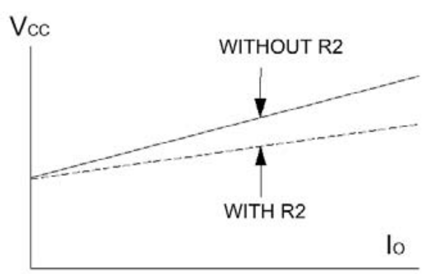

Figure 6. V_{CC} vs. I_O (secondary load)

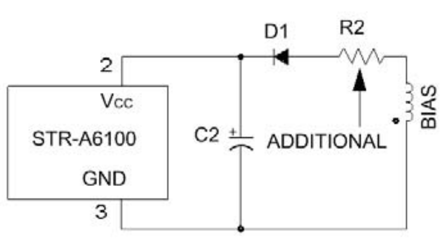

Figure 7. V_{CC} peripheral circuit with R2

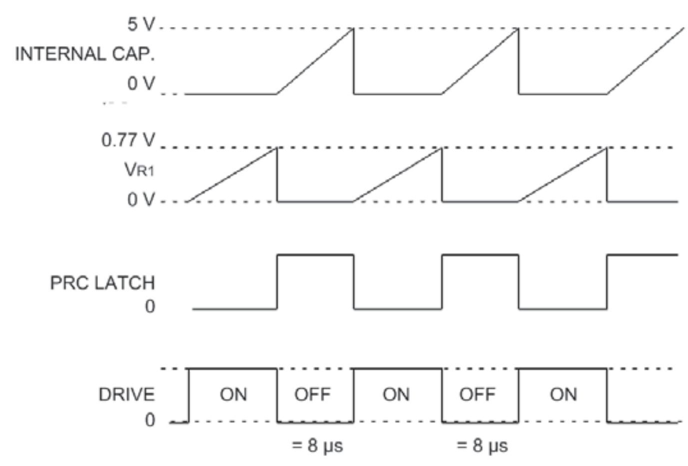

Figure 8. Internal waveforms

I_{FB} is obtained through the following procedure: I_{FB} is added to another constant current (I_X), converted to voltage by RFB, and fed into the inverting input of comparator FB as V_{RFB}. Meanwhile, the voltage waveform of R1 (current-sense resistor) is fed into the non-inverting input of FB via the Buffer block as V_{OCPM}. The FB comparator compares V_{FB1} with V_{OCPM} to reset the PRC latch circuit and to turn off the output MOSFET.

In general, a current-mode control makes phase compensation easy and operational stability excellent. On the other hand, it has a drawback of possible malfunction caused by noises from surge current when the output MOSFET is switched on.

In order to avoid this, the leading spike is blanked out with a time constant of t_b = 320 ns.

Overcurrent protection (OCP, Pin 1)

A pulse-by-pulse circuit configuration, which detects peak drain current in every pulse, is used in an OCP circuit. The maximum output power is determined by the OCP and AC input voltages.

Figure 10 shows the dependence of V_O and I_O upon AC input voltage during an OCP operation (an overload state). The falling slope shows an OCP operation area where V_O decreases as I_O

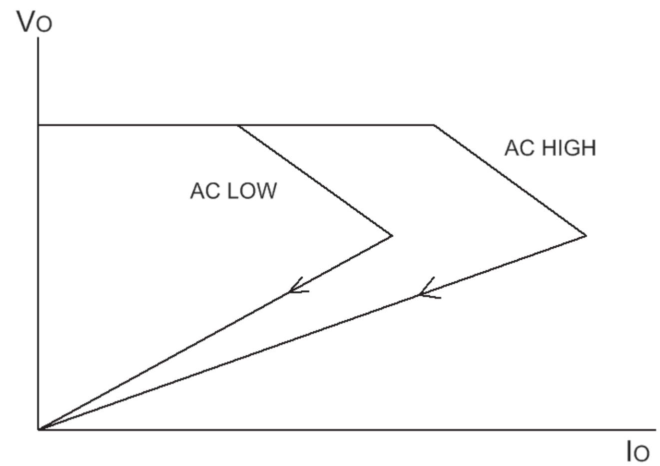

Figure 10. V_O vs. I_O (secondary)

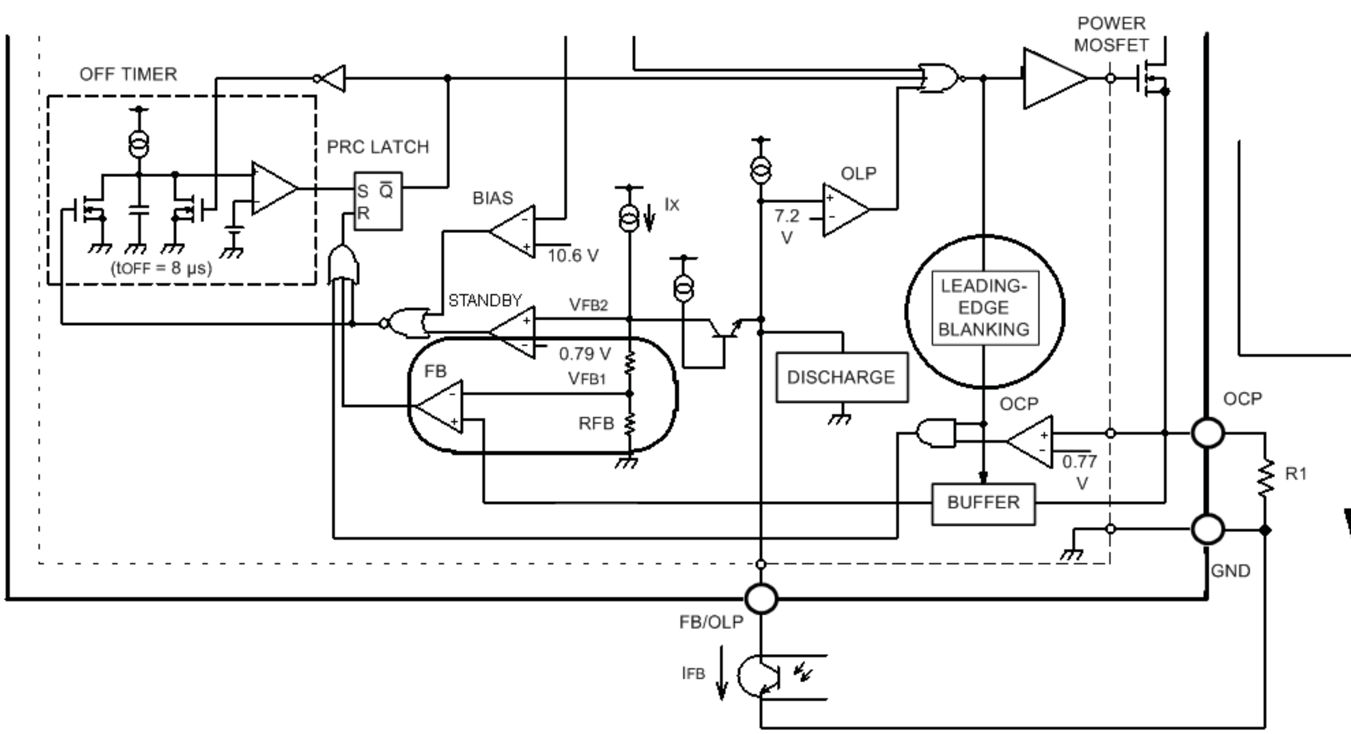

Figure 9. Current-mode control

increases, and proportionally, the bias winding voltage decreases. When V_{CC} becomes lower than the operation stop voltage (10 V), the IC stops its operation. After that, the internal constant-current source is turned on again, and V_{CC} increases, reaching the operation-start voltage, the IC is activated again. However, in case the overload state continues, V_{CC} decreases, and the IC goes into an operation-stop state again. As long as this overload state continues, the aforementioned chain of operation will be repeated (intermittent operation of UVLO).

When the coupling structure of the transformer is not good between the secondary-side winding and the primary-side bias winding, there are cases where bias winding voltage does not drop and the intermittent operation mode does not begin, even if the output voltage drops at the overload state. Overload protection (OLP) circuitry is incorporated in order to prevent this and to protect the power supply.

Overload protection (FB/OLP, Pin 4)

The STR-A6100 series incorporates an overload protection (OLP) circuit. This circuit will stop oscillation when the overload state continues for a certain period (the drain current is limited by the OCP operation).

The peripheral circuit of the OLP is shown in figure 11. I_{OLP} = 26 µA from the constant-current source is fed into the FB/OLP pin. In the overload state, output voltage at the secondary side drops, and I_{FB} would not be drawn from the error amplifier at the secondary side. Then, C3 is charged by I_{OLP} through the Zener diode. The switching operation is halted until the voltage at C3 goes up to the OLP threshold voltage, V_{OLP} = 7.2 V. After the OLP operation, the aforementioned intermittent operation of the UVLO will be repeated as long as the overload state continues.

Voltage Setup of Zener Diode In normal operation, the voltage at the FB/OLP pin varies within a voltage range determined by I_{OLP} and I_{FB}. Conduction of the Zener diode within this range means that C3 is connected to the optotransistor in parallel. As a result, the load response becomes worse. In general, the recommended value of the Zener diode is 4.7 to 6.2 V so it cannot be conducted in a normal operation mode.

Setup of C3 The value of C3 can be obtained by determining the time from an overload state to an oscillation stop and by getting the delay time, t_d, in seconds from the following:

$$t_d = C3 \times (V_{OLP}(min) - V_Z - V_F) / I_{OLP}(max)$$

where

V_Z = Zener diode voltage, and
V_F = Zener diode forward voltage

Notes:

- t_d should be set to be longer than the start-up time because the start-up mode is considered to be an overload state.
- Selection of C3 and the Zener diode should be taken into account on the bench.

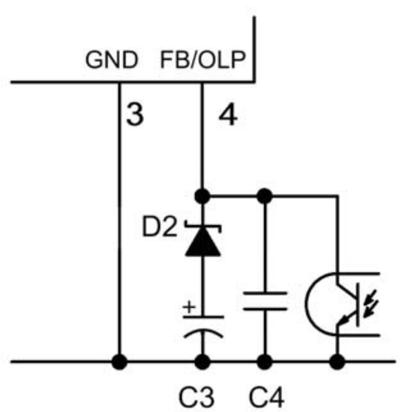

Figure 11. External OLP circuit

Auto Standby mode (FB/OLP, Pin 4)

During periods of light loads, Auto Standby mode maintains constant regulated output voltage, V_O, by using the burst voltage control method. The IC toggles between normal switching operation (during which the average current control method is used) and Auto Standby operation according to the voltage at the FB/OLP pin, V_{FB}. In turn, I_{FB} is modulated by the external OLP feedback circuit (see the optotransistor in figure 11).

The operation of Auto Standby is illustrated by the typical waveforms shown in figure 12. At light I_O current loads, I_{FB} increases and V_{FB} falls accordingly. If V_{FB} decreases to $V_{FB(standby)}$ = 0.79 V, the internal standby comparator changes state and the capacitor in the off-timer circuit is shorted to stop the IC normal switching operation (A in figure 12).

When switching operation stops, V_O at the secondary side decreases slightly. Accordingly, I_{FB} decreases, V_{FB} rises again, the standby comparator again changes state, and the shorted state of the capacitor in the off-timer circuit is released. The burst voltage control function restarts IC switching, with a fixed off-time. restoring V_O (B in figure 12). If the load is still light, however, I_{FB} rises again and the cycle repeats. This Auto Standby repetition continues until the load returns to normal, and switching returns to normal (C in figure 12).

When Auto Standby operation occurs at a low frequencies, there could be audible noise from the transformer. In order to avoid this noise, during Auto Standby mode the IC limits the peak drain current, $I_{D(pk)}$, to 25% of normal operation level, I_{OCP}.

Auto-bias function

If coupling between the secondary-side winding and the bias winding is poor from the standpoint of transformer structure, the voltage at VCC might drop during Auto Standby mode to the operation-stop voltage, and the IC begins to work in the intermittent operation mode of UVLO.

In order to avoid this, the IC implements Auto-bias, which forces the IC to work in PRC (Pulse Ratio Control) operation mode when V_{CC} drops to the $V_{CC(bias)}$ = 10.6 V as shown in figure 13.

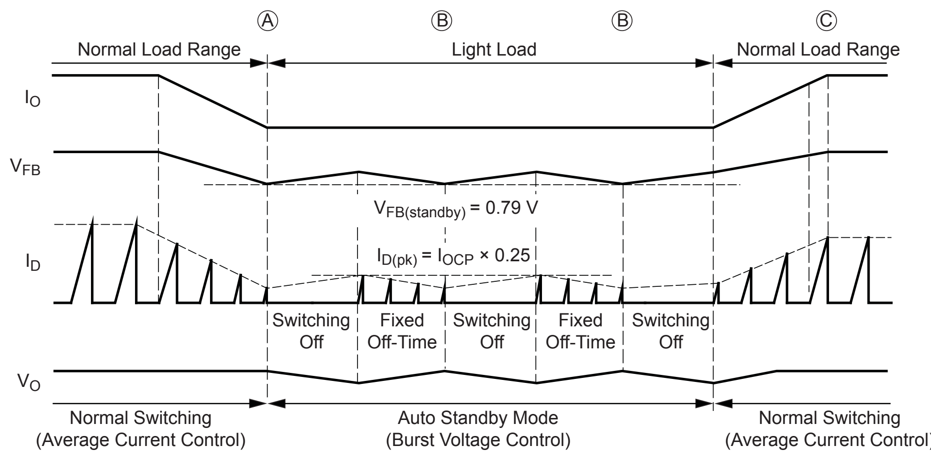

Figure 12. Auto Standby-mode waveforms

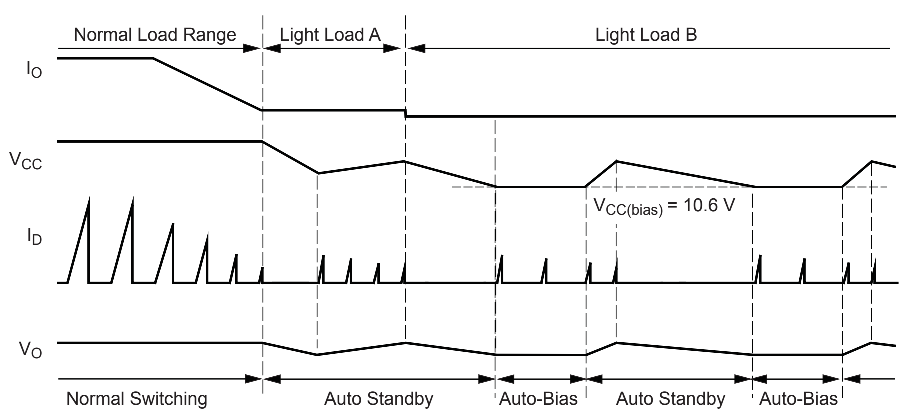

Figure 13. Auto-bias waveforms

A frequent auto-bias implementation results in high power consumption. Thus, it is recommended that the transformer is designed such that V_{CC} does not often drop until the operation stop voltage.

Latch circuit

OVP and TSD failure modes are latched by the latch circuit, and the MOSFET is shut down. In order to prevent erroneous mode operation from extraneous noises, a delay time is programmed so that the latch mode can be set only after a certain period of either OVP or TSD operation.

Even in a latched state, the constant-voltage (regulator) circuit is active, circuit current staying at a high level, and the VCC pin voltage decreases. When the VCC pin voltage goes down below the operation-stop voltage, $V_{CC(off)}$ = 10 V, the circuit current goes lower than 50 μA (at T_A = 25°C) and the VCC pin voltage rises again by means of the constant-current source. Then, the IC is activated again, the circuit current increasing, and the VCC pin voltage begins to drop. In this way, in a latched mode of operation, the VCC pin voltage goes up and down between 10 and 17.5 V so it can avoid an abnormal VCC pin voltage rise. Please refer to figure 14.

The latched mode is released by decreasing V_{CC} to the latch circuit releasing voltage, $V_{CC(LaOff)}$ = 7.3 V. In general, once the AC input is cut off, re-booting is needed.

Thermal shutdown (TSD)

Thermal shutdown (TSD) failure mode of operation is latched when the internal frame temperature exceeds 135°C (min).

Overvoltage protection (OVP)

The overvoltage-protection (OVP) mode of operation is latched when V_{CC} goes up to the $V_{CC(OVP)}$ = 31.2 V. Generally, the VCC pin is connected to the transformer bias winding. Because VCC is proportional to the output voltage, the OVP circuit is effective when the feedback circuit is open and the output voltage rises. The approximate output voltage at OVP operation is obtained from the following formula:

$$V_{O(OVP)}\ (\text{V}) = \frac{V_O\ (\text{V})}{V_{CC}\ (\text{V})} \times 31.2 \text{ typical (V)}$$

with VCC in normal operation.

Circuit Design Considerations

External components

- Selecting the optimum value of each external component must depend on an actual load and its variations.
- High-frequency current flows through the current-sense resistor (R1); thus, it is recommended that R1 have a small internal

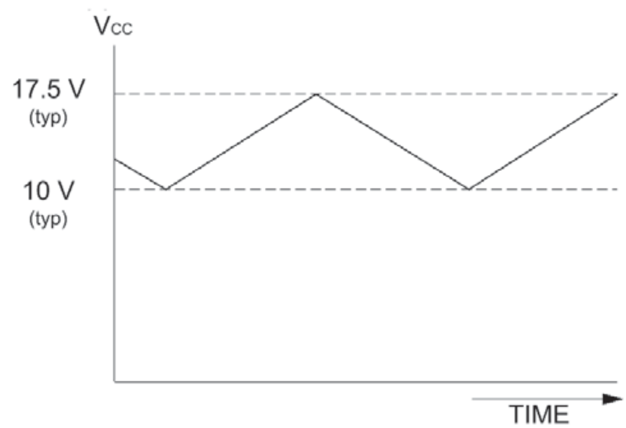

Figure 14. Latched mode of operation

inductance.

- Smoothing capacitors in the primary and secondary side should be high ripple-current types and be intended for switch-mode power supply applications.
- Temperature rise of each component should be allowed for; in particular, the life of the electrolytic capacitor needs to be considered.

Protection against negative input at start-up pin

If there is a possibility that the start-up voltage is more negative than -0.3 V, either a diode or a resistor (33 kΩ) must be added. See figure 15.

Appropriate diode specifications are:

- Peak reverse voltage (V_{RM}) > 35 V
- Forward current (I_F) > 1.5 mA
- Reverse recovery time (t_{rr}) < 27 μs
- Reverse current (I_R) < 100 μA

Phase correction

- Current-mode control topology of the STR-A6100 series does not require any special phase correction. However, in case of an unstable operation due to unique load requirements or high ripple voltage on the smoothing capacitors, a capacitor (C4 of approximately 680 pF) is inserted as shown in figure 16.
- Sanken's error-amplifier ICs (series SE), which feature phase correction to give consideration to transient response, enable reduction or simplification of the external phase-correction circuit.

Layout Considerations for PRC Operation

As shown in figure 17, all traces in the loop from the OCP pin to the drain pins (7 and 8) through R1, C1, and T1, where high current flows, should be kept as thick and short as possible. To eliminate common impedance, the GND pin and its peripheral components should be located as close to R1 as possible.

Component placement considerations in SMPS circuit

As pattern layout and component placement cause malfunction of the device, EMI noise, or power losses in the IC, the following guidelines should be followed:

- Traces where high frequency and high current flow should be kept thick and short to lower line impedance.

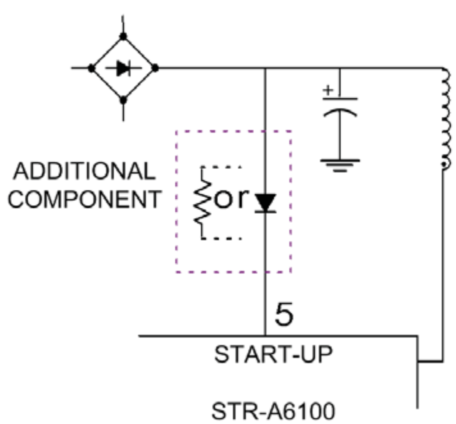

Figure 15. Added diode or resistor

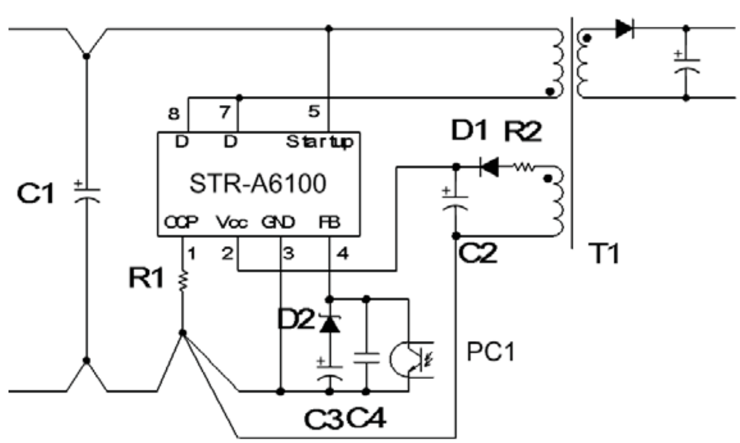

Figure 16. Typical connections

- As shown in figure 17, the hatched area where high frequency and high current create a loop should be kept as small as possible.
- GND and earth lines should be kept as thick and short as possible.
- In SMPS (Switch-Mode Power Supply) circuitry, as traces and paths of high voltage exist, component layout and trace length should be carefully considered, followed by safety requirements.
- Take into account the positive thermal coefficiency of the MOSFET $R_{DS(on)}$ when preparing the thermal design.

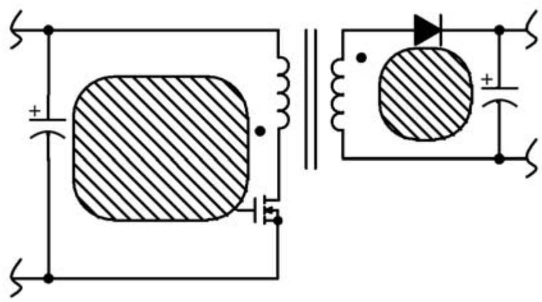

Figure 17. High-frequency, high-current loops

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

The products described herein are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

Sanken and Allegro reserve the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Therefore, the user is cautioned to verify that the information in this publication is current before placing any order.

When using the products described herein, the applicability and suitability of such products for the intended purpose shall be reviewed at the users responsibility.

Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.

Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.

Sanken products listed in this publication are designed and intended for use as components in general-purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Their use in any application requiring radiation hardness assurance (e.g., aerospace equipment) is not supported.

When considering the use of Sanken products in applications where higher reliability is required (transportation equipment and its control systems or equipment, fire- or burglar-alarm systems, various safety devices, etc.), contact a company sales representative to discuss and obtain written confirmation of your specifications.

The use of Sanken products without the written consent of Sanken in applications where extremely high reliability is required (aerospace equipment, nuclear power-control stations, life-support systems, etc.) is strictly prohibited.

The information included herein is believed to be accurate and reliable. Application and operation examples described in this publication are given for reference only and Sanken and Allegro assume no responsibility for any infringement of industrial property rights, intellectual property rights, or any other rights of Sanken or Allegro or any third party that may result from its use.

Anti radioactive ray design is not considered for the products listed herein.

This document is based on EF19EI.

Worldwide Contacts

Asia-Pacific

China

Sanken Electric Hong Kong Co., Ltd.
Suite 1026, Ocean Centre, Canton Road
Tsimshatsui, Kowloon, Hong Kong
Tel: 852-2735-5262, Fax: 852-2735-5494

Sanken Electric (Shanghai) Co., Ltd.
Room 3202, Maxdo Centre, Xingyi Road 8
Changning District, Shanghai, China
Tel: 86-21-5208-1177, Fax: 86-21-5208-1757

Taiwan Sanken Electric Co., Ltd.
Room 1801, 18th Floor, 88 Jung Shiau East Road
Sec. 2, Taipei 100, Taiwan R.O.C.
Tel: 886-2-2356-8161, Fax: 886-2-2356-8261

Japan

Sanken Electric Co., Ltd.
Overseas Sales Headquarters
Metropolitan Plaza Building, 1-11-1 Nishi-Ikebukuro
Toshima-ku, Tokyo 171-0021, Japan
Tel: 81-3-3986-6164, Fax: 81-3-3986-8637

Korea

Sanken Electric Korea Co., Ltd.
Mirae Asset Life Building, 6F
168 Kongduk-dong, Mapo-ku
Seoul 121-705, Korea
Tel: 82-2-714-3700, Fax: 82-2-3272-2145

Singapore

Sanken Electric Singapore Pte. Ltd.
150 Beach Road, #14-03 The Gateway West
Singapore 189720
Tel: 65-6291-4755, Fax: 65-6297-1744

Europe

Sanken Power Systems (UK) Limited
Pencoed Technology Park
Pencoed, Bridgend CF35 5HY, United Kingdom
Tel: 44-1656-869-100, Fax: 44-1656-869-162

North America

United States

Allegro MicroSystems, Inc.
115 Northeast Cutoff
Worcester, Massachusetts 01606, U.S.A.
Tel: 1-508-853-5000, Fax: 1-508-853-7895

Allegro MicroSystems, Inc.
14 Hughes Street, Suite B105
Irvine, California 92618, U.S.A.
Tel: 1-949-460-2003, Fax: 1-949-460-7837