

A6279 Timing Requirement

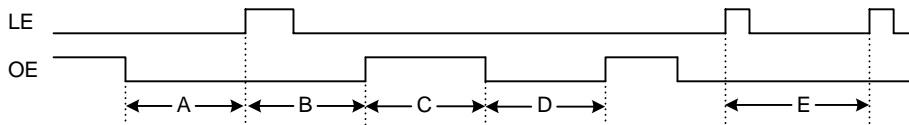
This application note describes implementation methods for the A6279 in certain customer application configurations.

The staggered delay circuit implemented in the A6279 results in some special timing restrictions, applicable if a system has asynchronous timing between OE and serial port programming of the outputs. In such a case, ignoring the timing restrictions (A...E below) would result in unpredictable LED operation. Essentially, if the outputs are given a command to change state, and the timing rule is violated, the instruction to change state will be ignored.

When the LED outputs are given commands to change, three different methods can be used:

1. Serial Port Latched Mode – Change command on rising edge of LE (diagram 1).
2. Serial Port Non-latched Mode – Change command on rising edge of CLK (diagram 2).
3. PWM of OE pin – (see both diagrams).

Diagram 1. Latched Mode

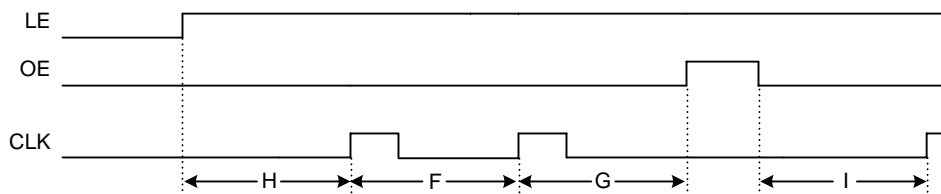


- A. Minimum OE falling to LE rising1200 ns
- B. Minimum LE rising to OE rising.....1200 ns
- C. Minimum OE high pulse width1200 ns
- D. Minimum OE low pulse width1200 ns
- E. Minimum LE period1200 ns

Note: If it is not possible to control the timing relationship between LE and a free running OE PWM signal, the end effect on the system can be minimized by:

1. Decreasing LE update frequency, to reduce the number of events where OE edges align with LE rising edge.
2. Increasing OE frequency. In the case of an A or B timing violation above, the data provided by the LE will be missed for only one PWM cycle. Therefore if the PWM is changed, from 100 Hz to 10 kHz for example, the outputs would only be in danger of having incorrect data for 100 μ s (10 kHz) instead of 10 ms (100 Hz). Having the LEDs at an incorrect state for short durations may not be noticeable.

Diagram 2. Non-Latched Mode



- F. Minimum CLK period1200 ns
- G. Minimum CLK rising to OE rising ...1200 ns
- H. Minimum LE rising to CLK rising1200 ns
- I. Minimum OE falling to CLK rising ..1200 ns

Note: The typical value for the staggered delay is typically in range 680 ns to 850 ns. The 1200 ns value was chosen to add some margin.

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