Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: June 2, 2014

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.
The A1174 is a micro-power, Hall-effect latch for use in portable devices that employ rotational detection systems, and have a power supply voltage between 1.65 and 3.5 V. The device has a single push-pull output structure and requires no external pull-up resistor for reliable operation.

When a sufficient positive magnetic field is present on the device, the device output transitions to the low state and is latched in this state until a negative field of sufficient strength latches the device output into the high state. The latched output is ideal when using multiple sensors in rotational speed and direction sensing systems (for example, track ball and scroll bar systems in portable devices).

The device includes an innovative clocking scheme that satisfies the micro-power needs of almost any application, including track balls for PDAs and cell phones. Using the EXTERNAL_CLK and DUAL_CLK pins as described in this datasheet, the device can be set into various working modes.

In Dual Clock mode, the device switches between predefined slow and fast sampling rates. The average current consumption of the device is extremely low when rotation is not detected. In External Clock mode, the user sets the clock rate for the device to achieve the required on and off times for controlling average power. This user-determined clocking also helps to

---

**Features and Benefits**

- Micro-power latch operation
- 1.65 to 3.5 V battery operation
- Push-pull output eliminates the need for an external pull-up resistor
- User configured, internally or externally controlled sample and sleep periods
  - Floating the two clock pins results in the use of a fixed sampling clock internal to the device
  - Toggling the clock pins allows the user to control the sampling and sleep times of the device for extreme low power operation
- External control of the clock pins allows the user to implement synchronous sampling of multiple sensors in direction detection systems
- Chopper stabilization
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Solid state reliability
- Small size

**Package:** 6-contact MLP/DFN (suffix EW)

1.5 mm × 2 mm × 0.40 mm

---

**Description**

The A1174 is a micro-power, Hall-effect latch for use in portable devices that employ rotational detection systems, and have a power supply voltage between 1.65 and 3.5 V. The device has a single push-pull output structure and requires no external pull-up resistor for reliable operation.

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**Figure 1. Timing diagram for output switching**

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A1174-DS, Rev. 7
Ultrasensitive Hall Effect Latch
with Internally or Externally Controlled Sample and Sleep Periods
for Track Ball and Scroll Wheel Applications

Description (continued)

achieve synchronous clocking of multiple devices. This allows a
defined phase relationship between the output transitions of each
device in direction detection systems.

Improved stability is made possible through dynamic offset
cancellation using chopper stabilization, which reduces the residual
offset voltage normally caused by device overmolding, temperature
dependencies, and thermal stress. Solid state reliability is provided
by integrating, on a single silicon chip, a Hall-voltage generator,
a small-signal amplifier, chopper stabilization, a latch, and a
MOSFET output.

The device package is a 6-contact, 1.5 mm × 2 mm, 0.40 mm nominal
overall height MLP/DFN, with exposed pad for enhanced thermal
dissipation. It is lead (Pb) free, with NiPdAu leadframe plating.

Selection Guide

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Packing¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1174EEWLT-P²</td>
<td>DFN/MLP 1.5×2 mm; 0.40 mm maximum height</td>
<td>3000 pieces per 7-inch reel</td>
</tr>
</tbody>
</table>

¹Contact Allegro™ for additional packing options.
²Allegro products sold in DFN package types are not intended for automotive applications.

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Notes</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Supply Voltage</td>
<td>V_DD</td>
<td></td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Supply Voltage</td>
<td>V_DDR</td>
<td></td>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>V_OUT</td>
<td></td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Output Voltage</td>
<td>VROUT</td>
<td></td>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>EXTERNAL_CLK and DUAL_CLK Pins Input Voltage</td>
<td>V_IN</td>
<td></td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>EXTERNAL_CLK and DUAL_CLK Pins Reverse Input Voltage</td>
<td>VR_IN</td>
<td></td>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>I_OUT(sink)</td>
<td></td>
<td>–1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I_OUT(source)</td>
<td></td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>Magnetic Flux Density*</td>
<td>B</td>
<td>Unlimited</td>
<td>G</td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>T_A</td>
<td>Range E</td>
<td>–40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>T_J(MAX)</td>
<td></td>
<td>165</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_STG</td>
<td></td>
<td>–65 to 170</td>
<td>°C</td>
</tr>
</tbody>
</table>

²1G = 0.1 mT (millitesla)

Terminal List

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>No connect</td>
</tr>
<tr>
<td>3</td>
<td>VOUT</td>
<td>Output</td>
</tr>
<tr>
<td>4</td>
<td>EXTERNAL_CLK</td>
<td>In combination with DUAL_CLK, allows external control of the device sampling period and duty cycle</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>DUAL_CLK</td>
<td>In combination with EXTERNAL_CLK, drives the part in Dual Clock mode</td>
</tr>
</tbody>
</table>
Ultrasensitive Hall Effect Latch with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

Functional Block Diagram
**Ultrasonic Hall Effect Latch**

with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

**Operating Characteristics** Valid over full operating voltage and ambient temperature ranges (unless otherwise specified)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Electrical Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage2</td>
<td>VDD</td>
<td>TA = 25°C</td>
<td>1.65</td>
<td>–</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–40°C ≥ TA ≥ 85°C</td>
<td>1.8</td>
<td>–</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>Output On Voltage</td>
<td>VOUT(SAT)</td>
<td>NMOS on, IOUT = 1 mA</td>
<td>–</td>
<td>100</td>
<td>300</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>VOUT(HIGH)</td>
<td>PMOS on, IOUT = 1 mA</td>
<td>VDD–300</td>
<td>VDD–100</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>Supply Current</td>
<td>IDD(EN)</td>
<td>Chip in awake state (enabled)</td>
<td>–</td>
<td>–</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>IDD(DIS)</td>
<td>Chip in sleep state (disabled)</td>
<td>–</td>
<td>–</td>
<td>8.0</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>IDD(AV)</td>
<td>Normal Clock mode, VDD = 2.5 V</td>
<td>–</td>
<td>–</td>
<td>71</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Normal Clock mode, VDD = 3.0 V</td>
<td>–</td>
<td>–</td>
<td>82</td>
<td>μA</td>
</tr>
<tr>
<td>Internal Chopper Stabilization Clock Frequency</td>
<td>fC</td>
<td>–</td>
<td>200</td>
<td>–</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_CLK and DUAL_CLK Pins Input Current</td>
<td>IIN</td>
<td>VEXTERNALCLK = VDD, VDUALCLK = VDD</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>EXTERNAL_CLK and DUAL_CLK Pins Leakage Current</td>
<td>IOFF</td>
<td>VEXTERNALCLK = 0 V, VDUALCLK = 0 V</td>
<td>–</td>
<td>0.02</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td>Supply Slew Rate3</td>
<td>SR</td>
<td>tOFF = 100 ms</td>
<td>0.1</td>
<td>–</td>
<td>–</td>
<td>V/ms</td>
</tr>
<tr>
<td><strong>Normal Clock Mode Characteristics4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal Mode Awake Duration</td>
<td>tawake_norm</td>
<td>–</td>
<td>25</td>
<td>46</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Normal Mode Period</td>
<td>tperiod_norm</td>
<td>–</td>
<td>0.7</td>
<td>1.05</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td><strong>External Clock Mode Characteristics4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_CLK and DUAL_CLK Pins Threshold</td>
<td>VB(HIGH)</td>
<td>–</td>
<td>–</td>
<td>0.75×VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VB(LOW)</td>
<td>0.25×VDD</td>
<td>–</td>
<td>–</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>External Clock Mode Awake Duration</td>
<td>tawake_ext</td>
<td>VEXTERNALCLK &gt; VB(HIGH)</td>
<td>46</td>
<td>–</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td>External Clock Mode Period</td>
<td>tperiod_ext</td>
<td>VEXTERNALCLK &gt; VB(HIGH)</td>
<td>80</td>
<td>–</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td>State Transition Delay5</td>
<td>tdelay_ext</td>
<td>–</td>
<td>25</td>
<td>46</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td><strong>Dual Clock Mode Characteristics4</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Clock Mode Awake Duration</td>
<td>tawake_dual</td>
<td>–</td>
<td>25</td>
<td>46</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Dual Clock Mode Fast Sampling Period</td>
<td>tperiod_fast</td>
<td>–</td>
<td>8× tawake_dual</td>
<td>–</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Dual Clock Mode Slow Sampling Period</td>
<td>tperiod_slow</td>
<td>–</td>
<td>28</td>
<td>–</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Dual Clock Mode Timeout6</td>
<td>ttimeout</td>
<td>–</td>
<td>100× tperiod_slow</td>
<td>–</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td><strong>Magnetic Characteristics2</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operate Point</td>
<td>BOP</td>
<td>South pole to device branded side</td>
<td>5</td>
<td>36</td>
<td>55</td>
<td>G</td>
</tr>
<tr>
<td>Release Point</td>
<td>BOP</td>
<td>North pole to device branded side</td>
<td>–55</td>
<td>–36</td>
<td>–5</td>
<td>G</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>BHY</td>
<td>BOP – BOP</td>
<td>–</td>
<td>72</td>
<td>110</td>
<td>G</td>
</tr>
</tbody>
</table>

---

1Typical values are at TA = 25°C and VDD = 2.75 V. Performance may vary for individual units, within the specified maximum and minimum limits.
2Magnetic operate and release points vary with supply voltage.
3If the device power supply is chopped, power-up slew rate dVDD / dt has to be adjusted to ensure correct functioning of the device. tOFF is the time of the power cycle when VDD < VDD(min).
4Defined in the Functional Description section of this datasheet.
5Time between external clock transition and resulting transition of the device between the awake and sleep states. See Functional Description section.
6If no output transition is detected during the timeout interval, the device goes back into slow sampling. See Functional Description section.
Characteristic Performance

Saturation Voltage versus Temperature

Saturation Voltage versus Supply Voltage

Average Supply Current versus Temperature

Average Supply Current versus Supply Voltage

Normal Mode Period versus Temperature

Normal Mode Period versus Supply Voltage
Ultrasensitive Hall Effect Latch
with Internally or Externally Controlled Sample and Sleep Periods
for Track Ball and Scroll Wheel Applications
Ultrasensitive Hall Effect Latch
with Internally or Externally Controlled Sample and Sleep Periods
for Track Ball and Scroll Wheel Applications

Release Point versus Temperature

Release Point versus Supply Voltage

Hysteresis versus Temperature

Hysteresis versus Supply Voltage

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Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com
Ultrasensitive Hall Effect Latch with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

Functional Description

Output State Operation
The output state (VOUT pin) of this device switches to low (on) when an incident magnetic field, perpendicular to the Hall element, exceeds the operate point threshold, B_{OP}. After turn-on, the output voltage is V_{OUT(SAT)} (see figure 2). When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (off), V_{OUT(HIGH)}. The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field leaves the device output latched low (on) if the last crossed switchpoint is B_{OP}, or latched high (off) if the last crossed switchpoint is B_{RP}.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) gives an indeterminate output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

Micro-power Operation
Micro-power operation of the device involves duty cycle control achieved by:

- powering all circuits in the chip and latching the device output state at the end of awake state periods, and
- turning off the bias current to most circuits in the chip and maintaining the device output state through sleep state periods.

This is illustrated in figure 3. The awake state duration, t_{awake_x}, is common in all defined modes of operation. The sleep state duration is set at a longer duration than the awake period in order to conserve power. During the sleep state, current consumption is insignificant (equal to I_{DD(DIS)}), but the device output does not switch in response to changing incident magnetic fields.

The device shows maximum current consumption, I_{DD(EN)}, during the awake state and minimal current consumption, I_{DD(DIS)}, during the sleep state. Average current, I_{DD(AV)}, for micro-power operation is derived from following formula:

$$I_{DD(AV)} = \frac{I_{DD(EN)} \times t_{awake_x} + I_{DD(DIS)} \times t_{sleep_x}}{t_{period_x}}.$$

Three micro-power control modes are available:

- Normal Clock mode
- External Clock mode
- Dual Clock mode

Selection of clock mode is determined by the configuration of the EXTERNAL_CLK pin and the DUAL_CLK pin, and applied voltages as illustrated in figure 4 and table 1.

Normal Clock Mode When both device clock pins are left floating or are grounded, the internal timing circuitry activates the device for t_{awake_norm} and deactivates it for the remainder, t_{sleep}, of the duty cycle period, t_{period_norm}. The short awake time

Figure 2. Device output switching logic

Figure 3. Micro-power behavior of the device
allows stabilization prior to the IC sampling and data latching on the falling edge of the timing pulse. The output during the sleep time, $t_{\text{sleep}}$, is latched in the last sampled state.

**External Clock Mode** Applying a voltage greater than $V_{\text{th(HIGH)}}$ to both clock pins puts the device into the awake state (without automatic cycling through the sleep state). The device uses the maximum defined supply current, reaching maximum power consumption.

Applying a voltage greater than $V_{\text{th(HIGH)}}$ to the EXTERNAL_CLK pin and a voltage lower than $V_{\text{th(LOW)}}$ to the DUAL_CLK pin puts the device into the sleep state (without automatic cycling through the awake state), and latches the device output in the output state determined during the prior awake state.

The duration of the awake and sleep periods can be controlled externally by applying a voltage greater than $V_{\text{th(HIGH)}}$ to the EXTERNAL_CLK pin and applying an external clock to the DUAL_CLK pin. The user can define the input sampling time and frequency to reach a target consumption current level, but the minimum sample time must remain longer than $t_{\text{awake,ext}}$. Note that the device should be periodically put into the awake state in order to update the device output state.

State Transition Delay, $t_{\text{ext, delay}}$, appears as the time between an external clock transition and the resulting transition of the device between the awake and the sleep state. This is illustrated in figure 5.

**Dual Clock Mode** When the EXTERNAL_CLK pin is left floating, or is grounded, and the DUAL_CLK pin is pulled to a voltage greater than $V_{\text{th(HIGH)}}$, the device enters Dual Clock mode. Figure 6 gives an overview of the device operation algorithm in Dual Clock mode.

<table>
<thead>
<tr>
<th>Table 1. Clock Mode Selection Options</th>
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<tbody>
<tr>
<td><strong>Connection</strong></td>
</tr>
<tr>
<td>EXTERNAL_CLK Pin</td>
</tr>
<tr>
<td>Low / NC</td>
</tr>
<tr>
<td>High</td>
</tr>
<tr>
<td>Low / NC</td>
</tr>
<tr>
<td>Low / NC</td>
</tr>
</tbody>
</table>

$V_{\text{th(HIGH)}} > V \geq V_{\text{th(LOW)}}$, NC = no connect (float or connect to ground)

Figure 4. Clock mode selection algorithm; determined by clock pins connections in the application

Figure 5. External Clock mode clocking; $t_{\text{delay, ext}}$ corresponding to the device transition delay into the awake or sleep states after an external clock transition
Initially, the device operates in the slow sampling state with a typical sleep time duration, \( t_{\text{sleep, slow}} \). The awake time duration, \( t_{\text{awake}} \), is common in all defined modes of operation. After the first output state transition, the device switches into the fast sampling state, with a sleep time duration, \( t_{\text{sleep, fast}} \), of \( 8 \times t_{\text{awake, dual}} \). Fast input sampling ensures that the device does not miss any subsequent transitions of the incident magnetic field. This is advantageous in applications such as track ball monitoring, when the track ball can be rotated at very high speeds. If there is no output switching for the duration of the specified timeout, \( t_{\text{timeout}} \), then the device switches back into the slow sampling state to conserve battery life in handheld devices.

Figure 7 shows the case in which the field does not change within the \( t_{\text{timeout}} \) period. The behavior of the device in the presence of a rapidly changing magnetic field is shown in figure 8.

![Figure 6. Dual Clock mode operation algorithm](image)
Ultrasensitive Hall Effect Latch
with Internally or Externally Controlled Sample and Sleep Periods
for Track Ball and Scroll Wheel Applications

Figure 7. Device output response in Dual Clock mode with no change of the magnetic field for the duration of timeout

Figure 8. Device output response in Dual Clock mode with a rapid change of the magnetic field
Application Information

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique (0.1 μF is a typical value). Additionally, it is recommended that, when possible, pins be tied to either the VDD pin or ground potential in order to improve the EMC performance of the device. However, it is feasible to float the EXTERNAL_CLK and DUAL_CLK pins in the application. In the case where these pins are floating, care should be taken to locate the device as far as possible from system antennas and transceivers.

The schematics on this page represent typical application circuits.

(A) Device is working in Normal Clock mode. Power consumption is determined by device internal clock.

(B) Device is working in Dual Clock mode. Power consumption is determined by device internal clock; frequent usage of device in fast sampling state.

(C) Device is working in External Clock mode; externally-controlled power consumption.

(D) Device is working in External Clock mode; high power consumption.
Ultrasensitive Hall Effect Latch with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications

Package EW 6-Contact MLP/DFN

For Reference Only, not for tacking use (reference DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

Terminal #1 mark area
Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
Reference land pattern layout (reference IPC7351 SONSJP200X200X100-9M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JEDEC51-5)

Coplanarity includes exposed thermal pad and terminals
Active Area Depth 0.15 mm REF
Hall Element (not to scale)
Branding scale and appearance at supplier discretion

N = Last two digits of device part number
Y = Last digit of year of manufacture
W = Week of manufacture
# A1174

**Ultrasensitive Hall Effect Latch**

*with Internally or Externally Controlled Sample and Sleep Periods for Track Ball and Scroll Wheel Applications*

## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Revision Date</th>
<th>Description of Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev. 7</td>
<td>October 26, 2011</td>
<td>Update Selection Guide</td>
</tr>
</tbody>
</table>

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