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## *Chopper-Stabilized Hall-Effect Bipolar Switch*

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### **Not for New Design**

These parts are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: January 30, 2012

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, refer to the Allegro A1250.*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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*Allegro MicroSystems, Inc. reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.*

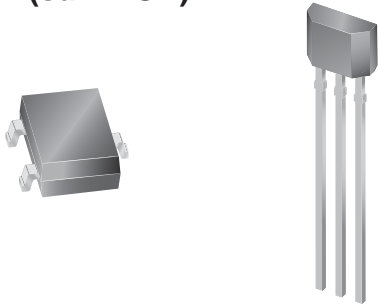
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# Chopper-Stabilized Hall-Effect Bipolar Switch

## Features and Benefits

- Chopper stabilization
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Reverse battery protection
- Output short circuit protection
- Solid state reliability
- Small size
- Robust EMC capability
- High ESD ratings (HBM)

**Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)**



Not to scale

## Description

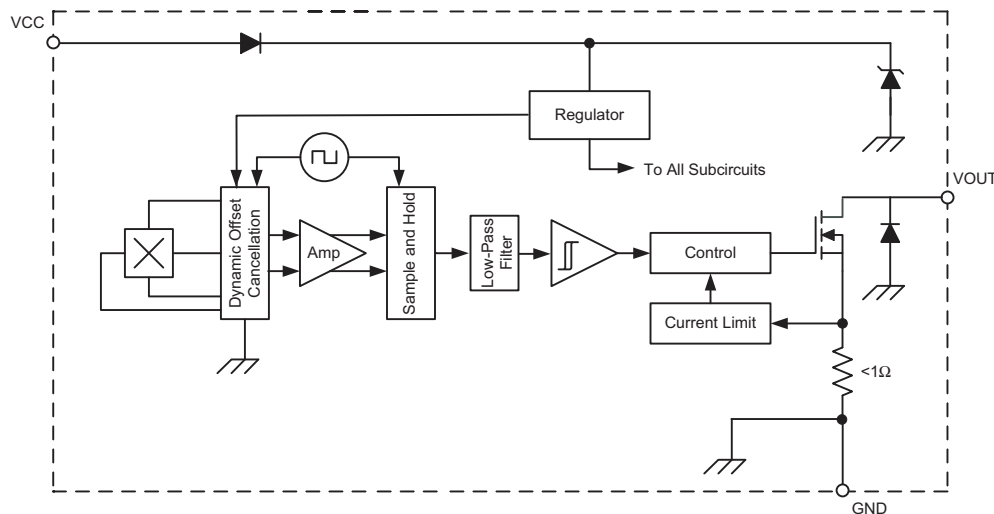
The A3230 Hall-effect sensor IC is a temperature stable, stress-resistant bipolar switch. This device is the most sensitive Hall-effect device in the Allegro® bipolar switch family and is intended for ring-magnet sensing. Superior high-temperature performance is made possible through an Allegro patented dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The A3230 includes the following on a single silicon chip: a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short circuit protected open-drain output. Advanced BiCMOS wafer fabrication processing takes advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

The A3230 Hall-effect bipolar switch turns on in a south polarity magnetic field of sufficient strength and switches off in a north polarity magnetic field of sufficient strength. Because the output state is not defined if the magnetic field is

*Continued on the next page...*

## Functional Block Diagram



# A3230

# Chopper-Stabilized Hall Effect Bipolar Switch

## Description (continued)

diminished or removed, to ensure that the device switches, Allegro recommends using magnets of both polarities and of sufficient strength in the application.

The A3230 is rated for operation between the ambient temperatures  $-40^{\circ}\text{C}$  and  $85^{\circ}\text{C}$  for the E temperature range, and  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$

for the L temperature range. Two A3230 package styles provide magnetically optimized solutions for most applications. Package LH is a SOT23-W, a miniature low-profile surface-mount package, while package UA is a three-lead ultramini SIP for through-hole mounting. Each package is available in a lead (Pb) free version, with 100% matte tin plated leadframes.



## Selection Guide

Part Number	Packing <sup>1</sup>	Mounting	Ambient, $T_A$ ( $^{\circ}\text{C}$ )	$B_{RP(MIN)}$ (G)	$B_{OP(MAX)}$ (G)
<del>A3230ELHLT-T<sup>2</sup></del>	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	-40 to 85	-25	25
<del>A3230EUA-T<sup>2</sup></del>	Bulk, 500 pieces/bag	3-pin SIP through hole			
<del>A3230LLHLT-T<sup>3</sup></del>	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	-40 to 150		
<del>A3230LUA-T<sup>3</sup></del>	Bulk, 500 pieces/bag	3-pin SIP through hole			

<sup>1</sup>Contact Allegro for additional packing options.

<sup>2</sup>Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change October 31, 2011. Deadline for receipt of LAST TIME BUY orders is April 27, 2012.

<sup>3</sup>Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change January 30, 2012. Deadline for receipt of LAST TIME BUY orders is April 27, 2012.

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{CC}$		28	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Output Off Voltage	$V_{OUT}$		26.5	V
Output Current	$I_{OUTSINK}$		Internally Limited	-
Reverse-Output Current	$I_{ROUT}$		-10	mA
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	$^{\circ}\text{C}$
		Range L	-40 to 150	$^{\circ}\text{C}$
Maximum Junction Temperature	$T_J(max)$		165	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$		-65 to 170	$^{\circ}\text{C}$

**OPERATING CHARACTERISTICS** valid over full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
<b>Electrical Characteristics</b>						
Supply Voltage <sup>1</sup>	$V_{CC}$	Operating, $T_J < 165^\circ\text{C}$	3.6	–	24	V
Output Leakage Current	$I_{OUTOFF}$	$V_{OUT} = 24\text{ V}$ , $B < B_{RP}$	–	–	10	$\mu\text{A}$
Output On Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$ , $B > B_{OP}$	–	250	500	mV
Output Current Limit	$I_{OM}$	$B > B_{OP}$	30	–	60	mA
Power-On Time	$t_{PO}$	$V_{CC} > 3.6\text{ V}$	–	8	50	$\mu\text{s}$
Chopping Frequency	$f_c$		–	200	–	kHz
Output Rise Time <sup>2</sup>	$t_r$	$R_{LOAD} = 820\ \Omega$ , $C_S = 20\text{ pF}$	–	0.2	1	$\mu\text{s}$
Output Fall Time <sup>2</sup>	$t_f$	$R_{LOAD} = 820\ \Omega$ , $C_S = 20\text{ pF}$	–	0.2	1	$\mu\text{s}$
Supply Current	$I_{CCON}$	$B > B_{OP}$	–	1.6	3.5	mA
	$I_{CCOFF}$	$B < B_{RP}$	–	1.6	3.5	mA
Reverse Battery Current	$I_{RCC}$	$V_{RCC} = -18\text{ V}$	–	–	-2	mA
Supply Zener Clamp Voltage	$V_Z$	$I_{CC} = 6.5\text{ mA}$ ; $T_A = 25^\circ\text{C}$	28	–	–	V
Supply Zener Current <sup>3</sup>	$I_Z$	$V_S = 28\text{ V}$	–	–	6.5	mA
<b>Magnetic Characteristics<sup>4</sup></b>						
Operate Point	$B_{OP}$	South pole adjacent to branded face of device	-10	7.5	25	G
Release Point	$B_{RP}$	North pole adjacent to branded face of device	-25	-7.5	10	G
Hysteresis	$B_{HYS}$	$B_{OP} - B_{RP}$	5	15	25	G

<sup>1</sup> Maximum voltage must be adjusted for power dissipation and junction temperature, see *Power Derating* section.

<sup>2</sup>  $C_S$  = oscilloscope probe capacitance.

<sup>3</sup> Maximum current limit is equal to the maximum  $I_{CC(MAX)} + 3\text{ mA}$ .

<sup>4</sup> Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a -100 G field and a 100 G field have equivalent strength, but opposite polarity).

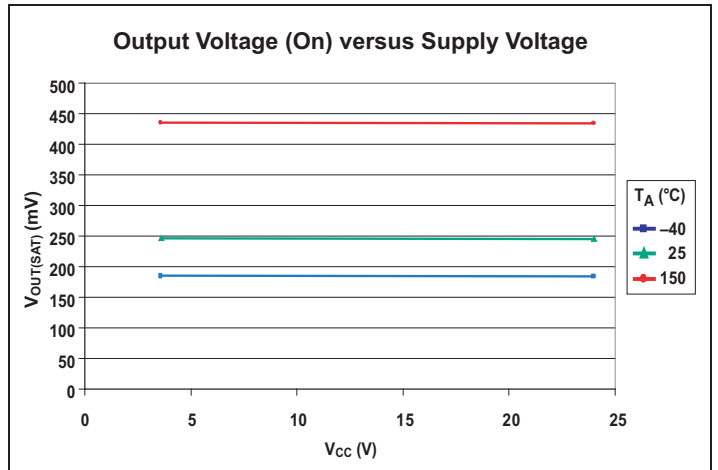
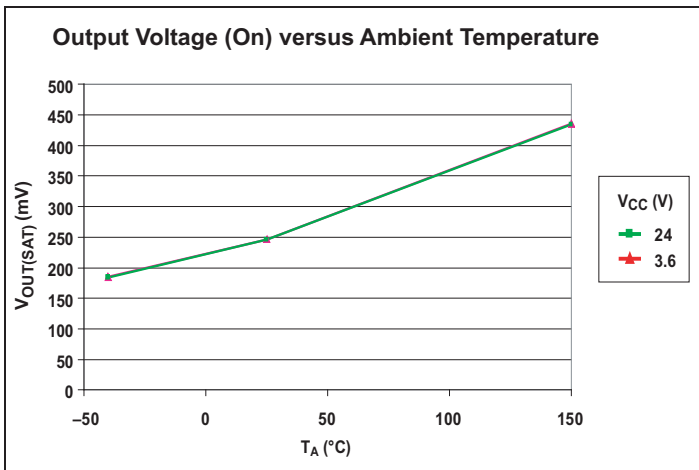
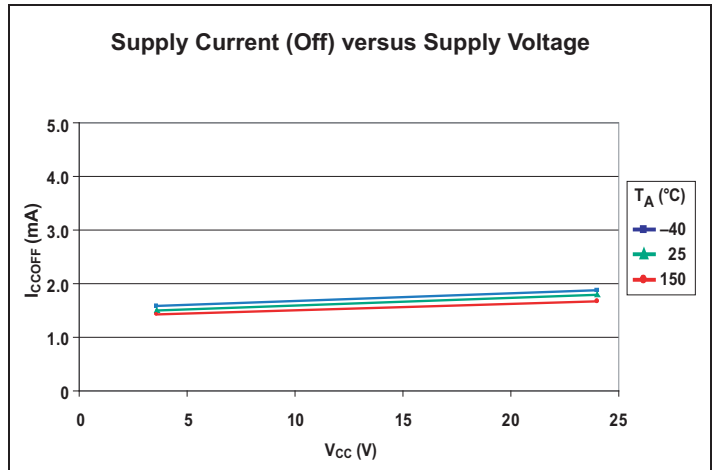
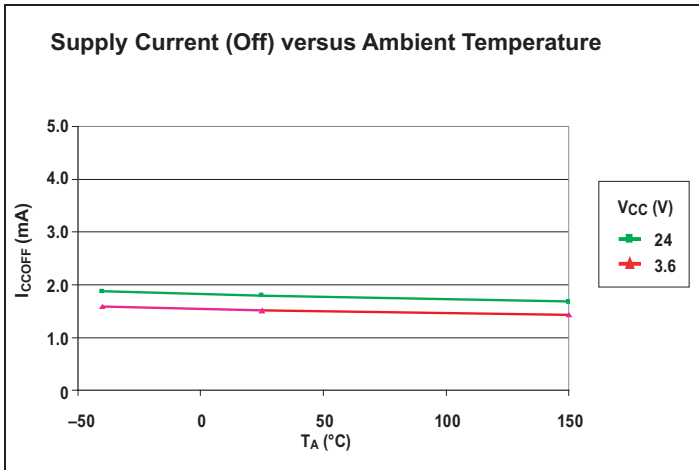
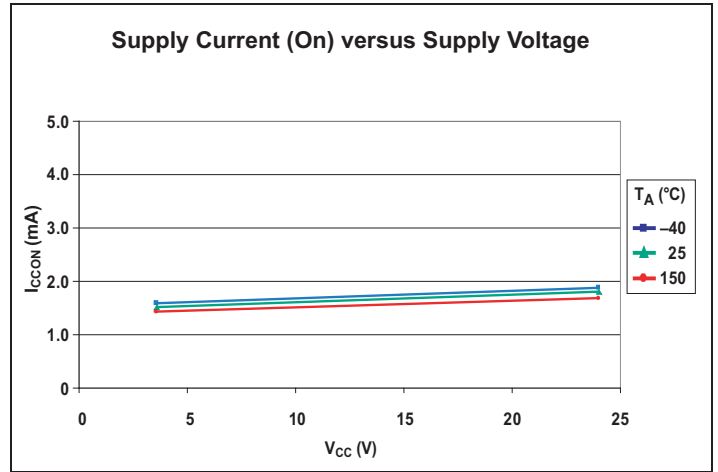
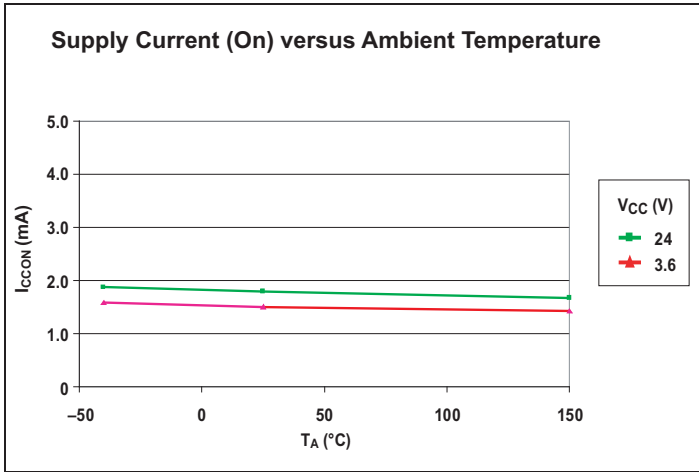
#### DEVICE QUALIFICATION PROGRAM

Contact Allegro for information.

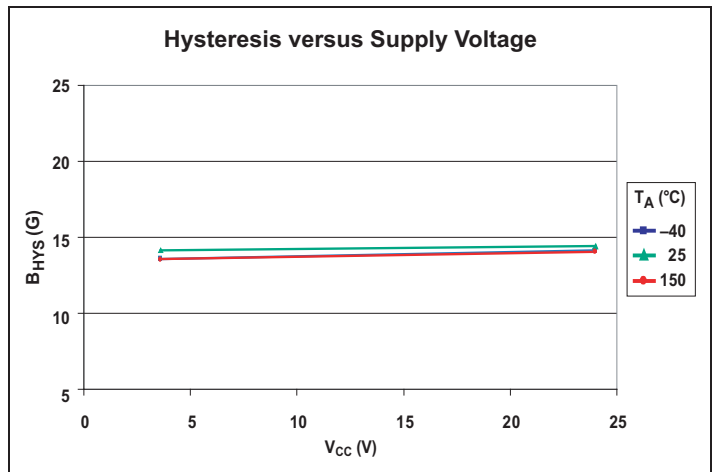
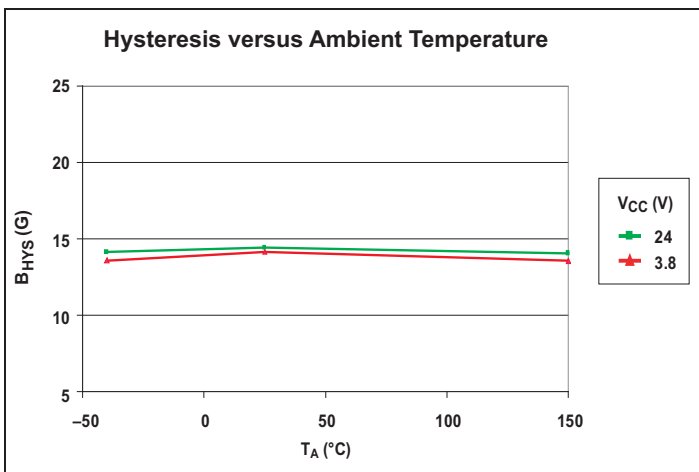
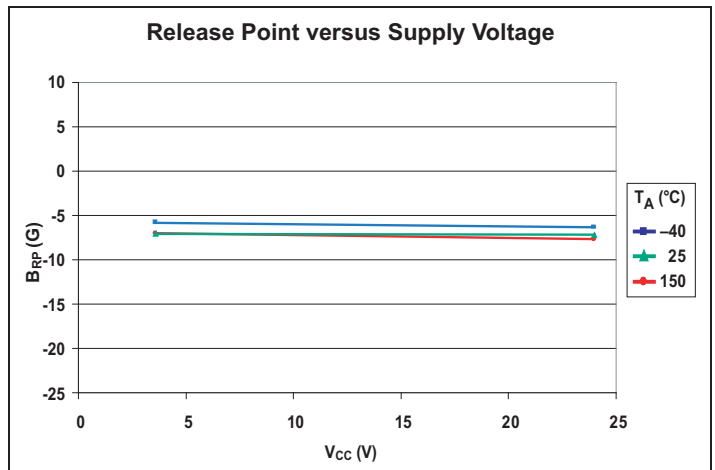
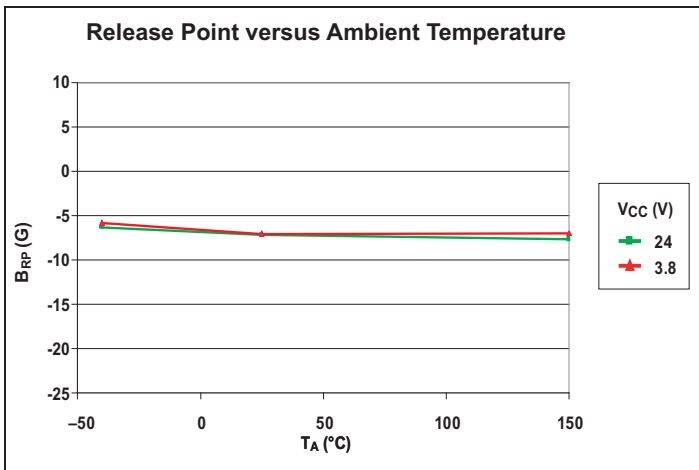
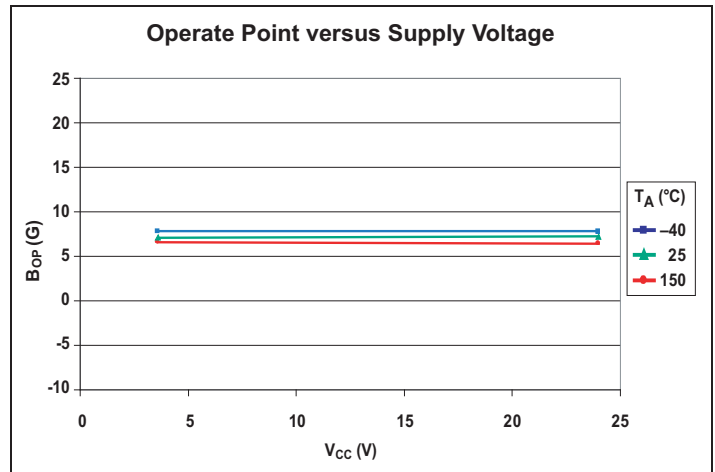
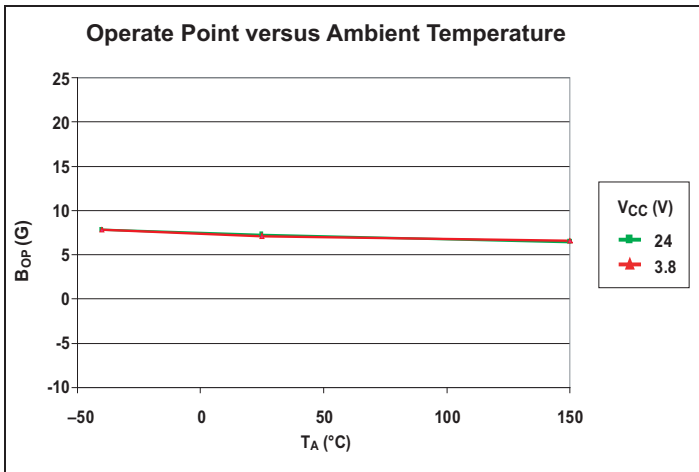
#### EMC (Electromagnetic Compatibility) REQUIREMENTS

Contact Allegro for information.

Electrical Characteristic Data



Magnetic Characteristic Data

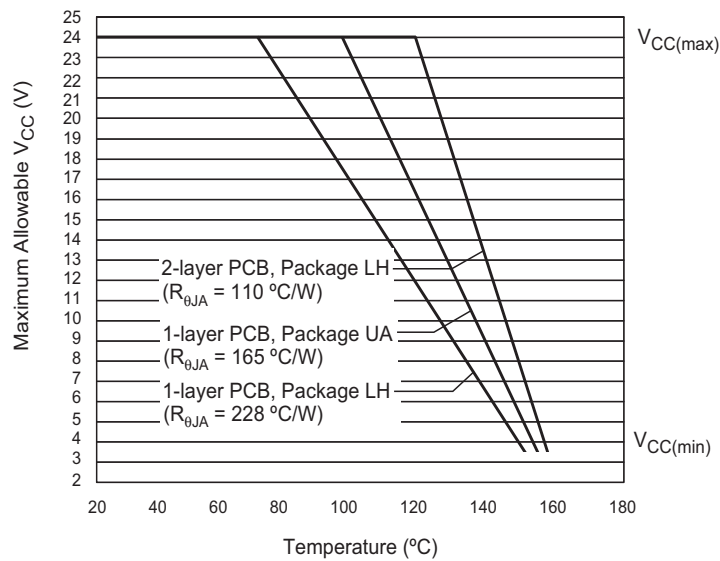


THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

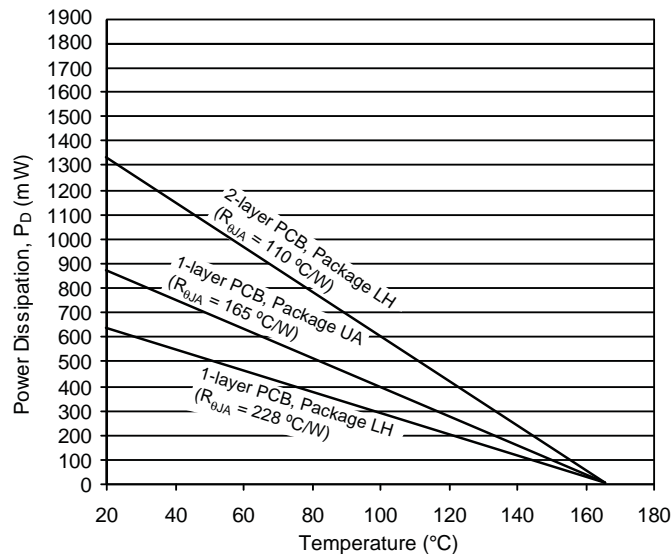
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	$^{\circ}\text{C}/\text{W}$
		Package LH, 2-layer PCB with 0.463 in. <sup>2</sup> of copper area each side connected by thermal vias	110	$^{\circ}\text{C}/\text{W}$
		Package UA, 1-layer PCB with copper limited to solder pads	165	$^{\circ}\text{C}/\text{W}$

\*Additional thermal information available on Allegro Web site.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

Operation

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold,  $B_{OP}$ . After turn-on, the output voltage is  $V_{OUT(SAT)}$ . The output transistor is capable of sinking current up to the short circuit current limit,  $I_{OM}$ , which is a minimum of 30 mA. When the magnetic field is reduced below the release point,  $B_{RP}$ , the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis,  $B_{HYS}$ , of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

There are three switching modes for bipolar devices, referred to as *latch*, *unipolar switch*, and *negative switch*. Mode is determined by the switchpoint characteristics of the individual device. Note that, as shown in figure 1, these switchpoints can lie in either north or south polarity ranges. The values of the magnetic parameters for the A3230 are specified in the Magnetic Characteristics table, on page 3.

Bipolar devices typically behave as latches (although these devices are not guaranteed to do so). In this mode, magnetic fields of opposite polarity and equivalent strengths are needed to switch the output. When the magnetic fields are removed ( $B \rightarrow 0$ ) the device remains in the same state until a magnetic

field of the opposite polarity and of sufficient strength causes it to switch. The hysteresis of latch mode behavior is shown in panel A of figure 1.

In contrast to latching, when a device exhibits unipolar switching, it only responds to a south magnetic field. The field must be of sufficient strength,  $> B_{OP}$ , for the device to operate. When the field is reduced beyond the  $B_{RP}$  level, the device switches back to the high state, as shown in panel B of figure 1. Devices

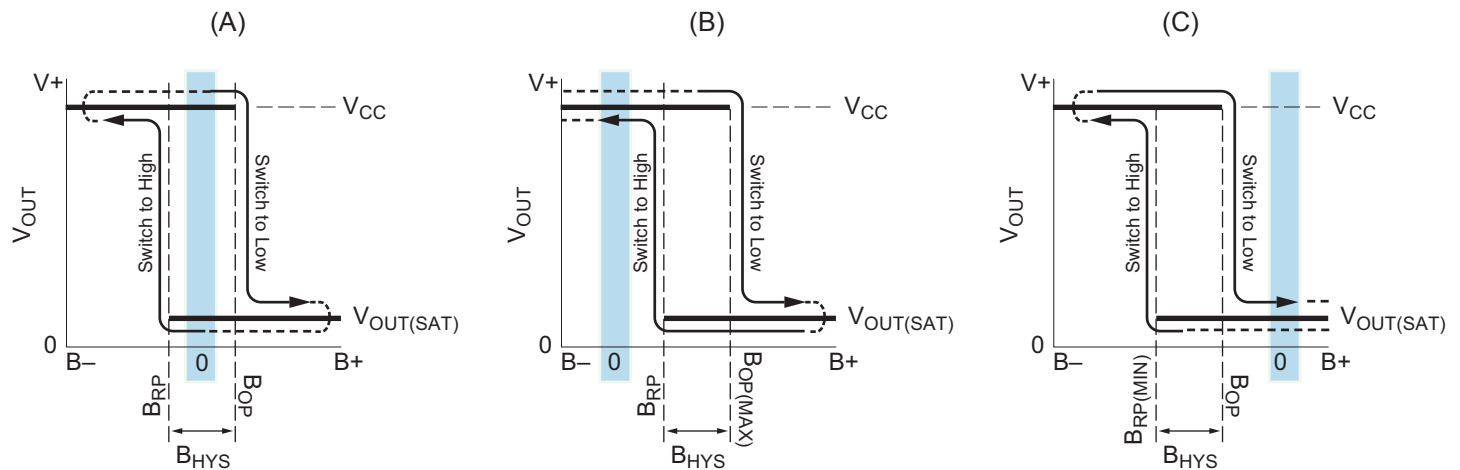
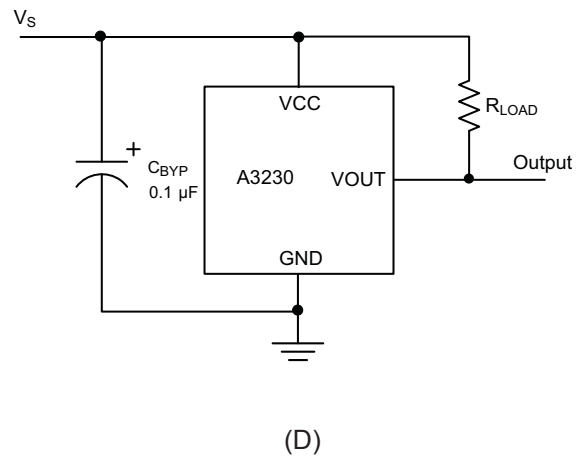


Figure 1. Bipolar Device Output Switching Modes. These behaviors can be exhibited when using a circuit such as that shown in panel D. Panel A displays the hysteresis when a device exhibits latch mode (note that the  $B_{HYS}$  band incorporates  $B = 0$ ), panel B shows unipolar switch behavior (the  $B_{HYS}$  band is more positive than  $B = 0$ ), and panel C shows negative switch behavior (the  $B_{HYS}$  band is more negative than  $B = 0$ ). Bipolar devices, such as the A3230, can operate in any of the three modes.

exhibiting negative switch behavior operate in a similar but opposite manner. A north polarity field of sufficient strength,  $> B_{RP}$ , (more north than  $B_{RP}$ ) is required for operation, although the result is that  $V_{OUT}$  switches high, as shown in panel C. When the field is reduced beyond the  $B_{OP}$  level, the device switches back to the low state.

The A3230 is designed to attain a small hysteresis, and thereby provide more sensitive switching. Although this means that true latching behavior cannot be guaranteed in all cases, proper switching can be ensured by use of both south and north magnetic fields, as in a ring magnet.

Bipolar devices adopt an indeterminate output state when powered-on in the absence of a magnetic field or in a field that lies within the hysteresis band of the device. The correct state is attained after the first excursion beyond  $B_{OP}$  or  $B_{RP}$ .

For more information on Bipolar switches, refer to Application Note 27705, *Understanding Bipolar Hall Effect Sensor ICs*.

### **Applications**

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in Panel B of figure 1, a  $0.1\mu\text{F}$  capacitor is typical.

Extensive applications information on magnets and Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide*, AN27701,
- *Hall-Effect Devices: Gluing, Potting, Encapsulating, Lead Welding and Lead Forming*, AN27703.1
- *Soldering Methods for Allegro's Products – SMT and Through-Hole*, AN26009

All are provided in *Allegro Electronic Data Book*, AMS-702 and the Allegro Web site: [www.allegromicro.com](http://www.allegromicro.com)

**Chopper Stabilization Technique**

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic-field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic-field-induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic-field-induced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed. This configuration is illustrated in figure 2.

The chopper stabilization technique uses a 200 kHz high-frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic-field-induced switching is affected slightly by a chopper technique. However, the Allegro high-frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital device families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

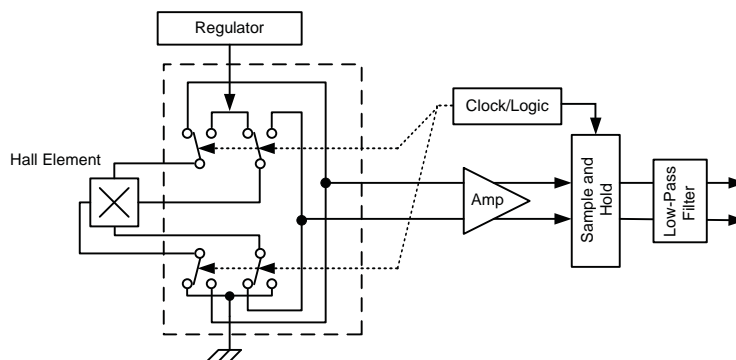


Figure 2. Chopper Stabilization Circuit (Dynamic Quadrature Offset Cancellation)

### Power Derating

The device must be operated below the maximum junction temperature of the device,  $T_{J(\max)}$ . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance,  $R_{\theta JA}$ , is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity,  $K$ , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case,  $R_{\theta JC}$ , is relatively small component of  $R_{\theta JA}$ . Ambient air temperature,  $T_A$ , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $I_{CC} = 1.5\text{ mA}$ , and  $R_{\theta JA} = 165\text{ }^\circ\text{C/W}$ , then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 1.5\text{ mA} = 18\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 18\text{ mW} \times 165\text{ }^\circ\text{C/W} = 3^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 3^\circ\text{C} = 28^\circ\text{C}$$

A worst-case estimate,  $P_{D(\max)}$ , represents the maximum allowable power level ( $V_{CC(\max)}$ ,  $I_{CC(\max)}$ ), without exceeding  $T_{J(\max)}$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for  $V_{CC}$  at  $T_A = 150^\circ\text{C}$ , package LH, using a low-K PCB.

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 228\text{ }^\circ\text{C/W}$ ,  $T_{J(\max)} = 165^\circ\text{C}$ ,  $V_{CC(\max)} = 24\text{ V}$ , and  $I_{CC(\max)} = 5\text{ mA}$ .

Calculate the maximum allowable power level,  $P_{D(\max)}$ . First, invert equation 3:

$$\Delta T_{\max} = T_{J(\max)} - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(\max)} = \Delta T_{\max} \div R_{\theta JA} = 15^\circ\text{C} \div 228\text{ }^\circ\text{C/W} = 66\text{ mW}$$

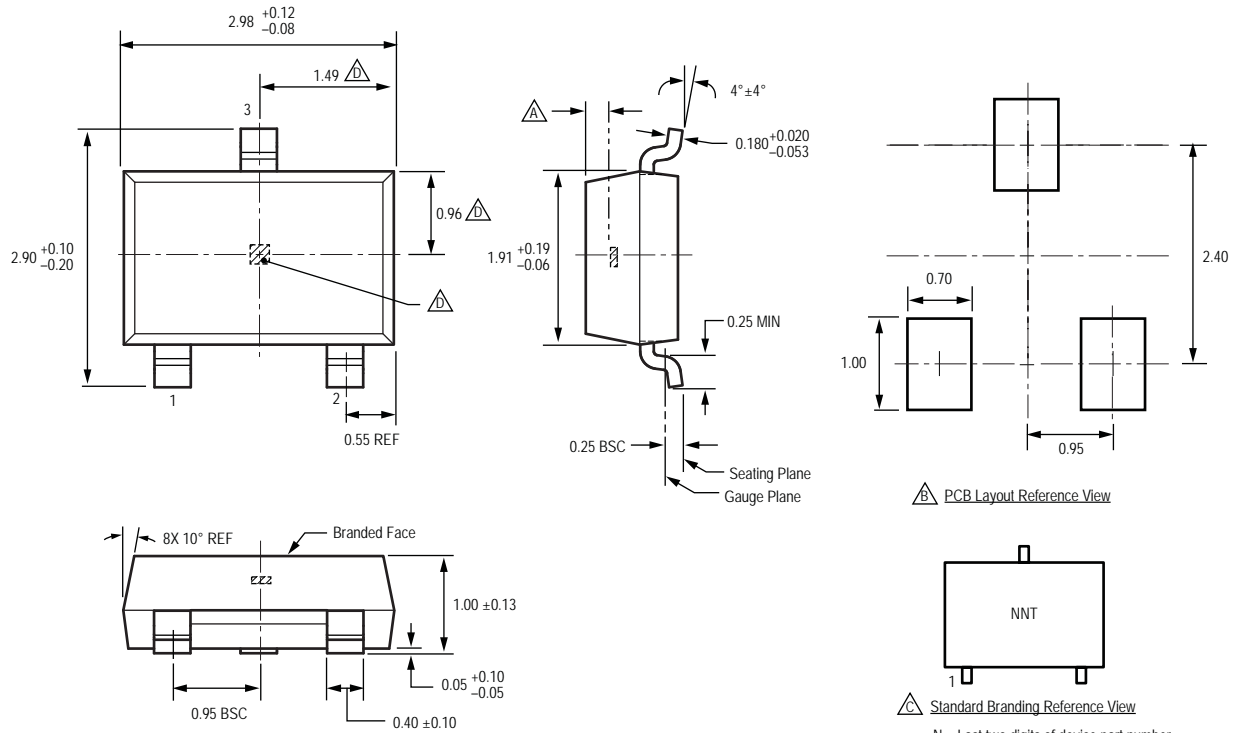
Finally, invert equation 1 with respect to voltage:

$$V_{CC(\text{est})} = P_{D(\max)} \div I_{CC(\max)} = 66\text{ mW} \div 5\text{ mA} = 13\text{ V}$$

The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(\text{est})}$ .

Compare  $V_{CC(\text{est})}$  to  $V_{CC(\max)}$ . If  $V_{CC(\text{est})} \leq V_{CC(\max)}$ , then reliable operation between  $V_{CC(\text{est})}$  and  $V_{CC(\max)}$  requires enhanced  $R_{\theta JA}$ . If  $V_{CC(\text{est})} \geq V_{CC(\max)}$ , then operation between  $V_{CC(\text{est})}$  and  $V_{CC(\max)}$  is reliable under these conditions.

## Package LH, 3-Pin SOT23-W

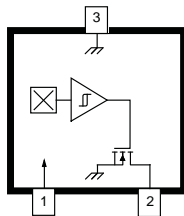


For Reference Only; not for tooling use (reference dwg. 802840)  
 Dimensions in millimeters  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

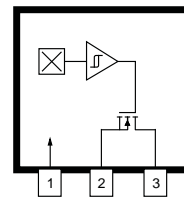
- Active Area Depth, 0.28 mm REF
- Reference land pattern layout  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
- Branding scale and appearance at supplier discretion
- Hall element, not to scale

## Pin-out Drawings

Package LH



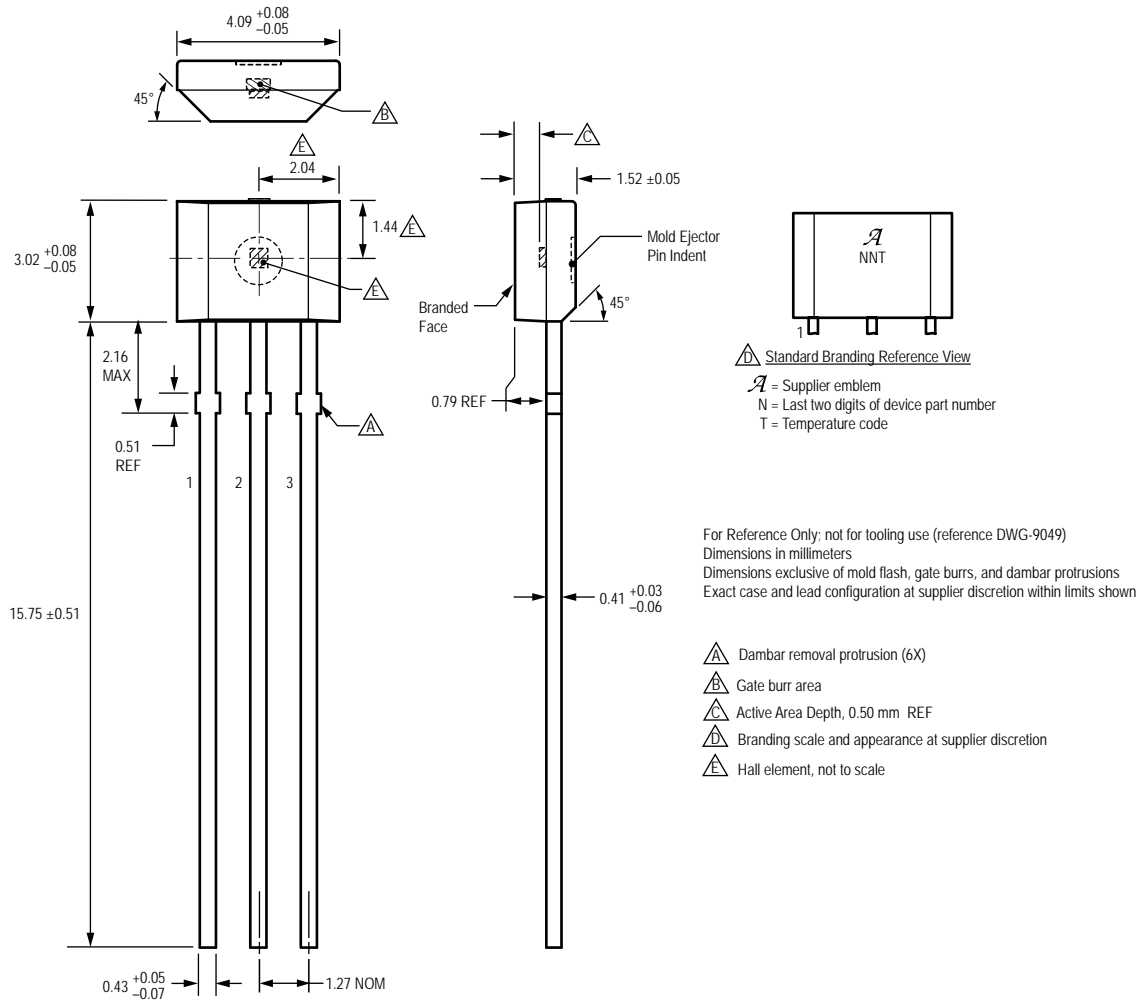
Package UA



## Terminal List

Name	Description	Number	
		Package LH	Package UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Ground	3	2

Package UA, 3-Pin SIP



**Revision History**

Revision	Revision Date	Description of Revision
Rev. 8	January 30, 2012	Update product availability

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