

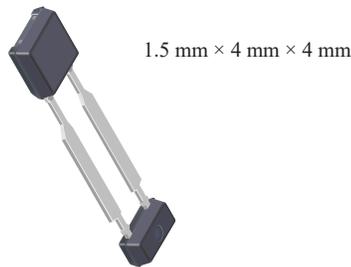
## Chopper-Stabilized Two-Wire Hall-Effect Switches

### FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- Factory-set temperature coefficient (TC) for use with ferrite magnets
- High-speed, 4-phase chopper stabilization
- Low switchpoint drift throughout temperature range
- Low sensitivity to thermal and mechanical stresses
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
  - On-board voltage regulator
  - 3 to 24 V operation
- Solid-state reliability

*Continued on the next page...*

### PACKAGE: 2-Pin, Ultra-Mini SIP (suffix UB)



*Not to scale*

### DESCRIPTION

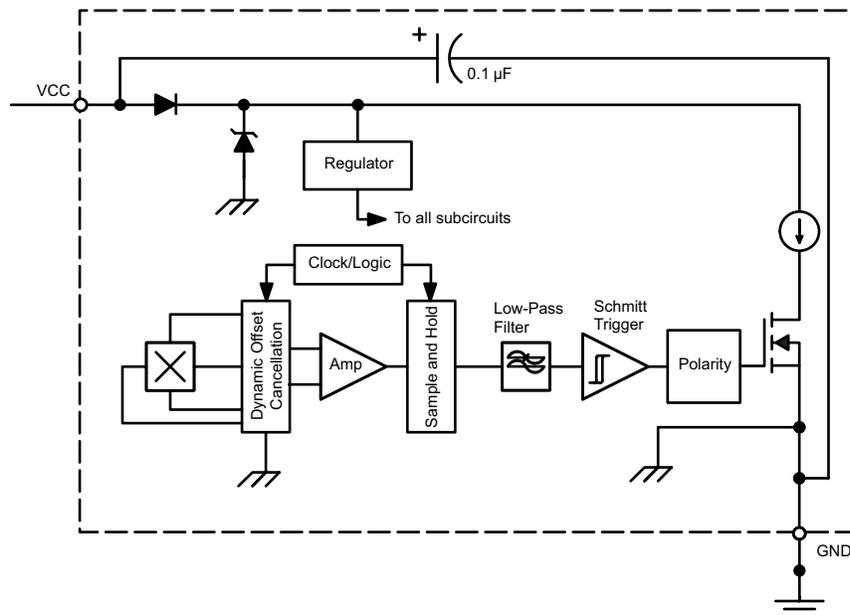
The A1152-F, A1153-F, A1155-F, and A1156-F comprise a family of two-wire, unipolar, Hall-effect switches, which are factory-trimmed to optimize magnetic switchpoint accuracy. These devices are produced on the Allegro™ advanced BiCMOS wafer fabrication process, which implements a high-frequency, 4-phase, chopper stabilization technique. This technique achieves magnetic stability over the full operating temperature range, and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh application environments.

The A115x family has a number of automotive applications. These include sensing seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position.

Two-wire unipolar switches are particularly advantageous in cost-sensitive applications because they require one less wire for operation versus the more traditional open-collector output switches. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition.

*Continued on the next page...*

### Functional Block Diagram



**FEATURES AND BENEFITS (CONTINUED)**

- Robust EMC and ESD performance
- Industry-leading ISO 7637-2 performance through use of proprietary, 40 V clamping structures
- Extended Operating Ambient temperature range, -40°C to 150°C
- UB package with integrated 0.1  $\mu$ F bypass capacitor

**DESCRIPTION (CONTINUED)**

The UB is a 2-pin, ultra-mini, single inline package (SIP) for through-hole mounting, and it is lead (Pb) free, with 100% matte-tin leadframe plating.

**SELECTION GUIDE**

Part Number	Packing	Package	Output ( $I_{CC}$ ) in South Polarity Field	Supply Current at $I_{CC(L)}$ (mA)	Magnetic Operate Point, $B_{OP}$ , at $T_A = 25^\circ\text{C}$ (G)
A1152LUBTN-F-T	13-in. reel, 4000 pieces/reel	2-pin SIP through-hole	Low	5 to 6.9	58 to 100
A1153LUBTN-F-T	13-in. reel, 4000 pieces/reel	2-pin SIP through-hole	High	5 to 6.9	58 to 100
A1155LUBTN-F-T	13-in. reel, 4000 pieces/reel	2-pin SIP through-hole	Low	5 to 6.9	16 to 60
A1156LUBTN-F-T	13-in. reel, 4000 pieces/reel	2-pin SIP through-hole	High	5 to 6.9	16 to 60

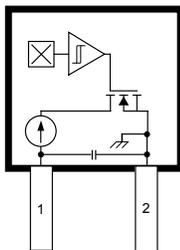
**ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC}$		28	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	$T_A$	Range L	-40 to 150	°C
Maximum Junction Temperature	$T_J(max)$		165	°C
Storage Temperature	$T_{stg}$		-65 to 170	°C

**INTERNAL DISCRETE CAPACITOR RATINGS**

Characteristic	Symbol	Notes	Rating	Unit
Rated Normal Capacitance	$C_{SUPPLY}$	Connected between VCC and GND	0.1	$\mu F$
Rated Voltage	$V_{CSUPPLY}$		50	V
Rated Capacitor Tolerance			$\pm 10$	%
Temperature Designator			X7R	-

**Pinout Diagram**



UB Package

**Terminal List Table**

Number	Name	Function
1	VCC	Input power supply
2	GND	Ground terminal

**ELECTRICAL CHARACTERISTICS:** Valid at  $T_A = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ,  $T_J < T_{J(\text{max})}$ ,  $C_{\text{BYP}} = 0.01 \mu\text{F}$  (excluding UB), through operating supply voltage range, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Supply Voltage [1][2]	$V_{\text{CC}}$	Operating, $T_J \leq 165^{\circ}\text{C}$		3.0	–	24	V
Supply Current	$I_{\text{CC(L)}}$	A1152, A1155	$B > B_{\text{OP}}$	5	–	6.9	mA
		A1153, A1156	$B < B_{\text{RP}}$				
	$I_{\text{CC(H)}}$	A1152, A1155	$B < B_{\text{RP}}$	12	–	17	mA
		A1153, A1156	$B > B_{\text{OP}}$				
Supply Zener Clamp Voltage	$V_{\text{Z(sup)}}$	$I_{\text{CC(L)(max)}} + 3 \text{ mA}$ , $T_A = 25^{\circ}\text{C}$		28	–	–	V
Supply Zener Clamp Current	$I_{\text{Z(sup)}}$	$V_{\text{Z(sup)}} = 28 \text{ V}$		–	–	$I_{\text{CC(L)(max)}} + 3 \text{ mA}$	mA
Reverse Supply Current	$I_{\text{RCC}}$	$V_{\text{RCC}} = -18 \text{ V}$		–	–	-1.6	mA
Output Slew Rate [3]	di/dt	Integrated bypass capacitor, capacitance of probe $C_S = 20 \text{ pF}$		–	0.22	–	mA/ $\mu\text{s}$
Chopping Frequency	$f_c$			–	700	–	kHz
Power-Up Time [4][5]	$t_{\text{on}}$	A1152, A1155	$B > B_{\text{OP}} + 10 \text{ G}$	–	–	25	$\mu\text{s}$
		A1153, A1156	$B < B_{\text{RP}} - 10 \text{ G}$				
Power-Up State [2][4][6][7]	POS	$t_{\text{on}} < t_{\text{on(max)}}$ , $V_{\text{CC}}$ slew rate $> 25 \text{ mV}/\mu\text{s}$		–	$I_{\text{CC(H)}}$	–	–

[1]  $V_{\text{CC}}$  represents the generated voltage between the VCC pin and the GND pin.

[2] The  $V_{\text{CC}}$  slew rate must exceed 600 mV/ms from 0 to 3 V. A slower slew rate through this range can affect device performance.

[3] Measured without bypass capacitor between VCC and GND. Use of a bypass capacitor results in slower current change.

[4] Power-Up Time is measured without and with bypass capacitor of 0.01  $\mu\text{F}$ . Adding a larger bypass capacitor would cause longer Power-Up Time.

[5] Guaranteed by characterization and design.

[6] Power-Up State as defined is true only with a  $V_{\text{CC}}$  slew rate of 25 mV/ $\mu\text{s}$  or greater.

[7] For  $t > t_{\text{on}}$  and  $B_{\text{RP}} < B < B_{\text{OP}}$ , Power-Up State is not defined.

**MAGNETIC CHARACTERISTICS** [1]: Valid at  $T_A = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  ( $T_J < T_J(\text{max})$ ), unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]	
<b>MAGNETIC CHARACTERISTICS</b>							
Magnetic Operating Point	$B_{OP}$	1152, 1153	$T_A = -40^{\circ}\text{C}$	72	–	118	G
			$T_A = 25^{\circ}\text{C}$	58	–	100	G
			$T_A = 150^{\circ}\text{C}$	37	–	68	G
		1155, 1156	$T_A = -40^{\circ}\text{C}$	23	–	73	G
			$T_A = 25^{\circ}\text{C}$	16	–	60	G
			$T_A = 150^{\circ}\text{C}$	9	–	49	G
Magnetic Release Point	$B_{RP}$	1152, 1153	$T_A = -40^{\circ}\text{C}$	56	–	103	G
			$T_A = 25^{\circ}\text{C}$	46	–	85	G
			$T_A = 150^{\circ}\text{C}$	22	–	58	G
		1155, 1156	$T_A = -40^{\circ}\text{C}$	6	–	53	G
			$T_A = 25^{\circ}\text{C}$	4	–	45	G
			$T_A = 150^{\circ}\text{C}$	4	–	39	G
Hysteresis	$B_{HYS}$	1152, 1153, 1155, 1156	$T_A = -40^{\circ}\text{C}$	5	–	30	G
			$T_A = 25^{\circ}\text{C}$	5	–	30	G
			$T_A = 150^{\circ}\text{C}$	5	–	30	G

[1] Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).

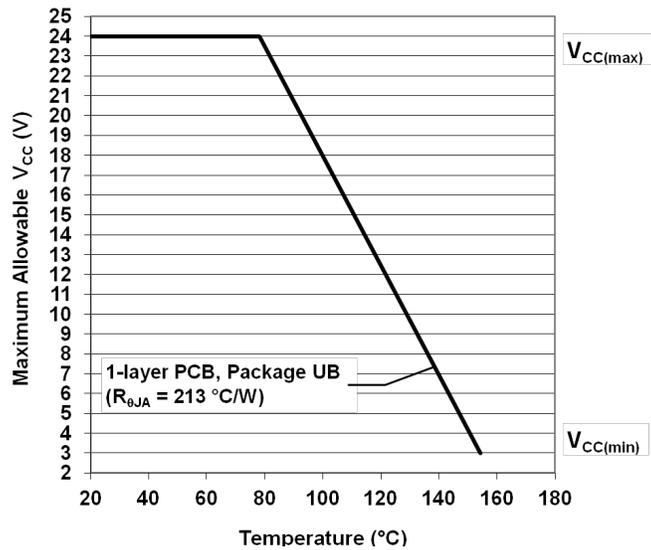
[2] 1 G (gauss) = 0.1 mT (millitesla).

**THERMAL CHARACTERISTICS:** may require derating at maximum conditions; see application information

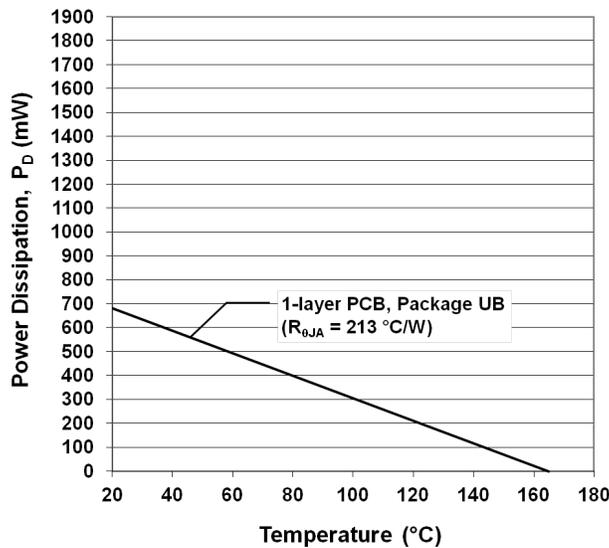
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package UB, on 1-layer PCB with copper limited to solder pads	213	$^{\circ}C/W$

\*Additional thermal information available on the Allegro website

UB Power Derating Curve

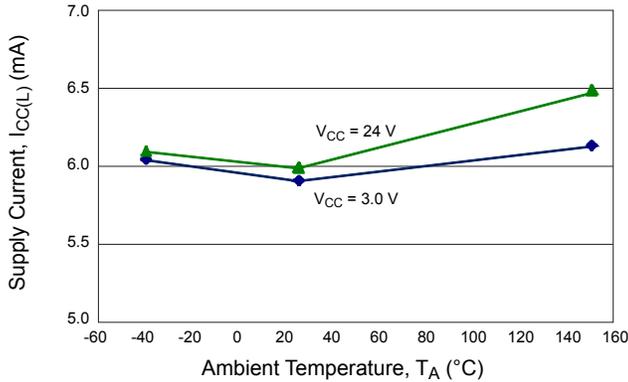


UB Power Dissipation versus Ambient Temperature

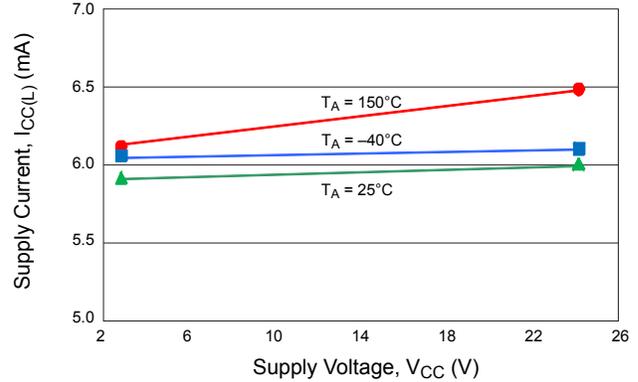


CHARACTERISTIC PERFORMANCE

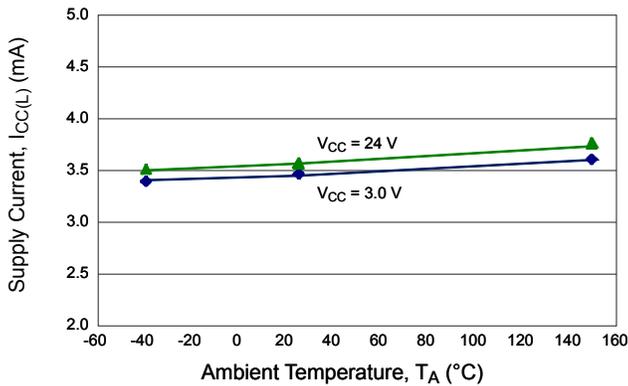
A1152-F/A1153-F  
Average Supply Current (Low) versus Temperature



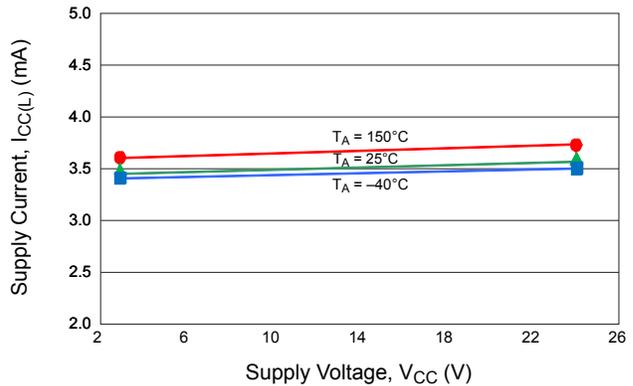
A1155-F/A1156-F  
Average Supply Current (Low) versus Supply Voltage



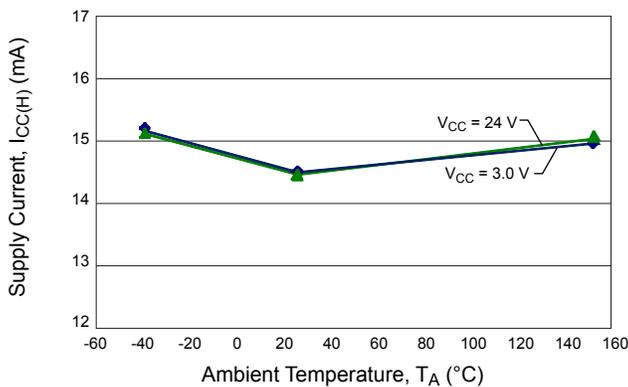
A1152-F/A1153-F  
Average Supply Current (Low) versus Temperature



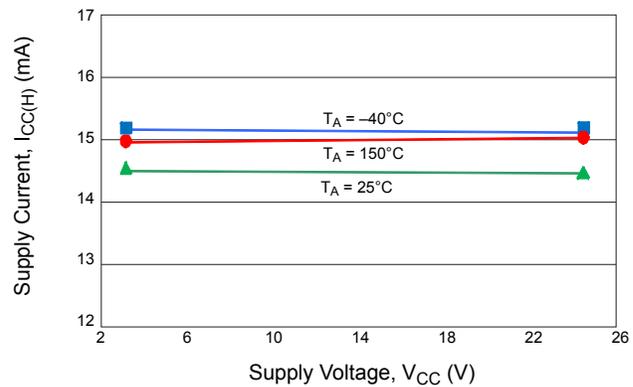
A1155-F/A1156-F  
Average Supply Current (Low) versus Supply Voltage



A1152-F/A1153-F  
Average Supply Current (High) versus Temperature

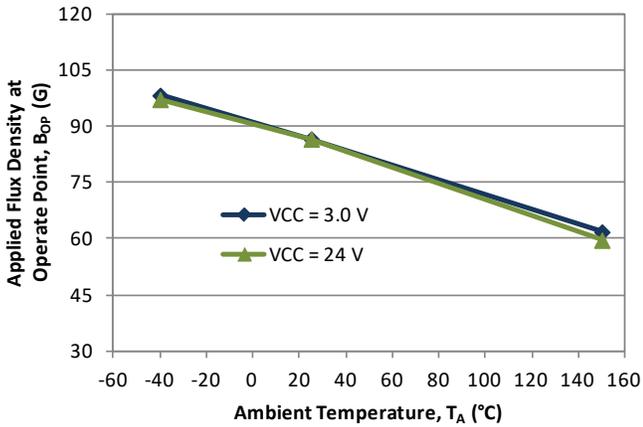


A1155-F/A1156-F  
Average Supply Current (High) versus Supply Voltage



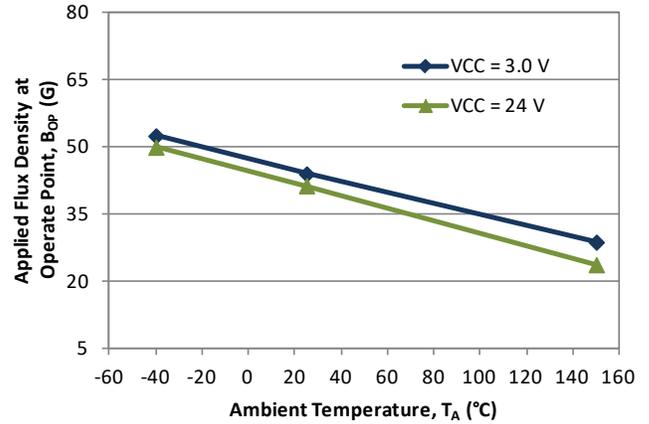
A1152-F/A1153-F

Average Operate Point versus Temperature



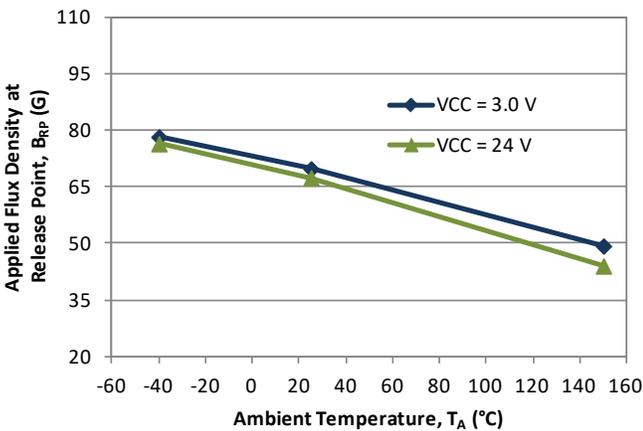
A1155-F/A1156-F

Average Operate Point versus Temperature



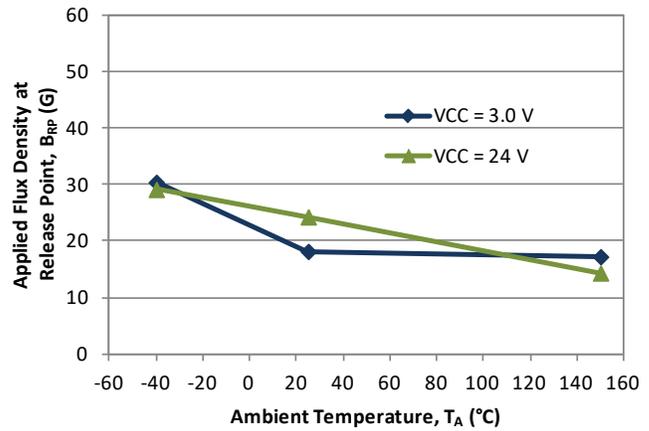
A1152-F/A1153-F

Average Release Point versus Temperature



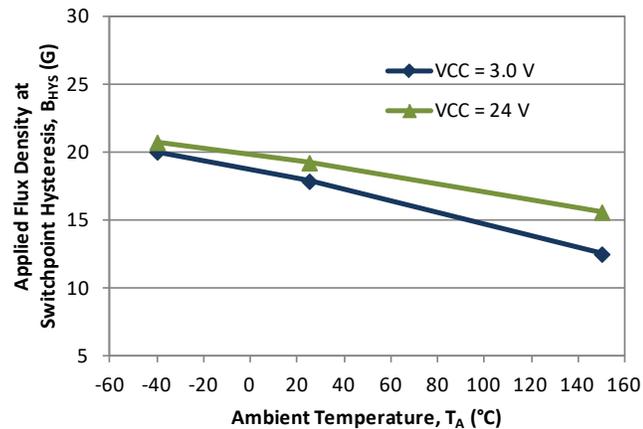
A1155-F/A1156-F

Average Release Point versus Temperature



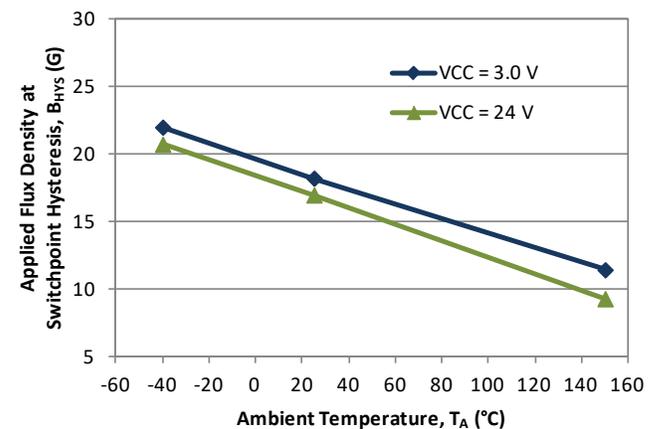
A1152-F/A1153-F

Average Switchpoint Hysteresis versus Temperature



A1155-F/A1156-F

Average Switchpoint Hysteresis versus Temperature



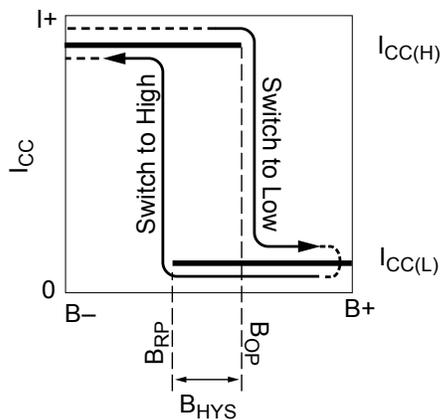
FUNCTIONAL DESCRIPTION

The A1152 and A1155 output,  $I_{CC}$ , switches low after the magnetic field at the Hall sensor IC exceeds the operate point threshold,  $B_{OP}$ . When the magnetic field is reduced to below the release point threshold,  $B_{RP}$ , the device output goes high. This is shown in Figure 1, panel A.

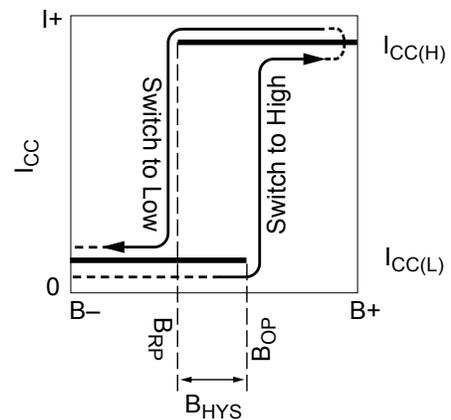
In the case of the reverse output polarity, as in the A1153 and A1156, the device output switches high after the magnetic field

at the Hall sensor IC exceeds the operate point threshold,  $B_{OP}$ . When the magnetic field is reduced to below the release point threshold,  $B_{RP}$ , the device output goes low (panel B).

The difference between the magnetic operate and release points is called the hysteresis of the device,  $B_{HYS}$ . This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.



(A) Hysteresis curve for A1152 and A1155



(B) Hysteresis curve for A1153 and A1156

Figure 1: Alternative Switching Behaviors Available in the A115x Device Family.

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B- direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

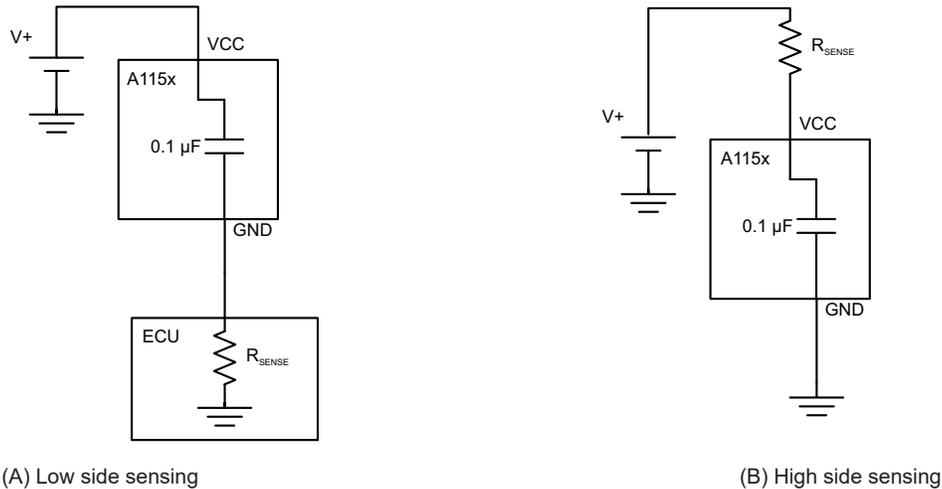


Figure 2: Typical Application Circuits

**Chopper Stabilization Technique**

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum

at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 350 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

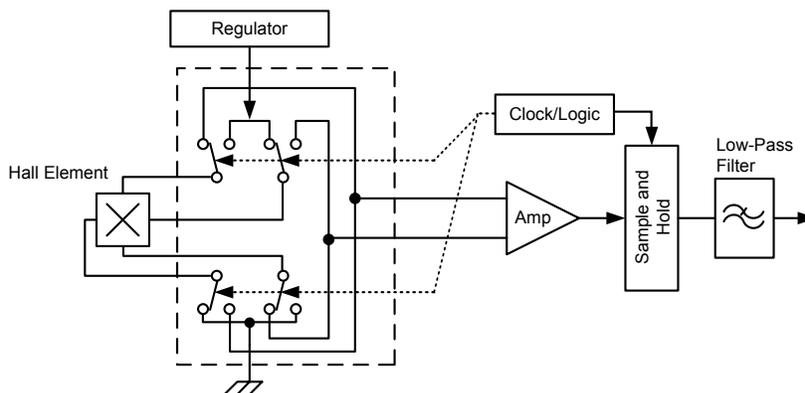


Figure 3: Chopper Stabilization Circuit (Dynamic Quadrature Offset Cancellation)

**Power Derating**

The device must be operated below the maximum junction temperature of the device,  $T_J(\text{max})$ . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance,  $R_{\theta JA}$ , is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity,  $K$ , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case,  $R_{\theta JC}$ , is relatively small component of  $R_{\theta JA}$ . Ambient air temperature,  $T_A$ , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For example, given common conditions such as:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $I_{CC} = 4\text{ mA}$ , and  $R_{\theta JA} = 140\text{ }^\circ\text{C/W}$ , then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 4\text{ mA} = 48\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 48\text{ mW} \times 140\text{ }^\circ\text{C/W} = 7^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 7^\circ\text{C} = 32^\circ\text{C}$$

A worst-case estimate,  $P_D(\text{max})$ , represents the maximum allowable power level ( $V_{CC}(\text{max})$ ,  $I_{CC}(\text{max})$ ), without exceeding  $T_J(\text{max})$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for  $V_{CC}$  at  $T_A = 150^\circ\text{C}$ , package UA, using a low-K PCB.

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 213\text{ }^\circ\text{C/W}$ ,  $T_J(\text{max}) = 165^\circ\text{C}$ ,  $V_{CC}(\text{max}) = 24\text{ V}$ , and  $I_{CC}(\text{max}) = 17\text{ mA}$ .

Calculate the maximum allowable power level,  $P_D(\text{max})$ . First, invert equation 3:

$$\Delta T_{\text{max}} = T_J(\text{max}) - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_D(\text{max}) = \Delta T_{\text{max}} \div R_{\theta JA} = 15^\circ\text{C} \div 213\text{ }^\circ\text{C/W} = 70.5\text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(\text{est})} = P_D(\text{max}) \div I_{CC}(\text{max}) = 70.5\text{ mW} \div 17\text{ mA} = 4.15\text{ V}$$

The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(\text{est})}$ .

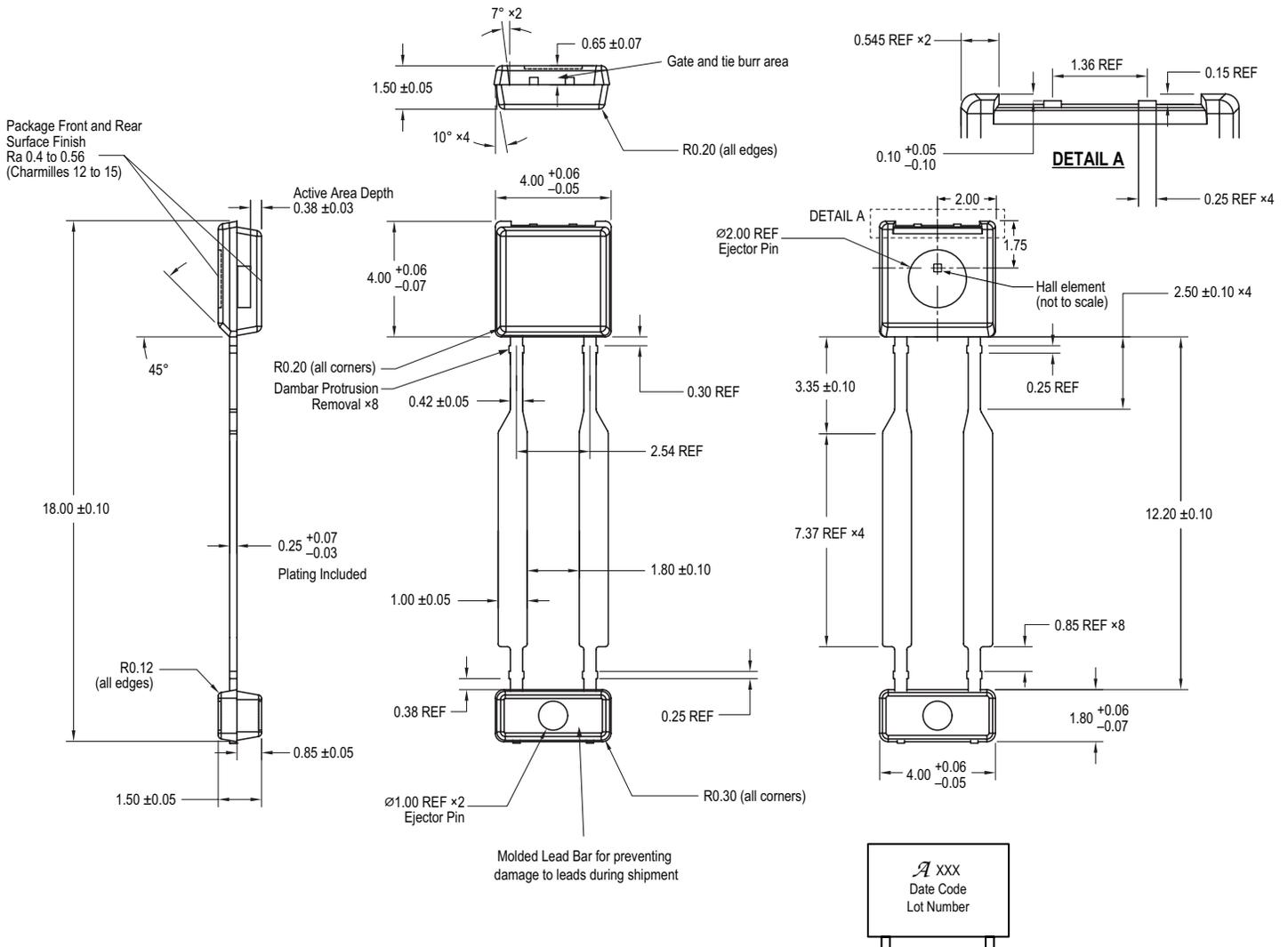
- (1) Compare  $V_{CC(\text{est})}$  to  $V_{CC}(\text{max})$ . If  $V_{CC(\text{est})} \leq V_{CC}(\text{max})$ , then reliable operation between  $V_{CC(\text{est})}$  and  $V_{CC}(\text{max})$  requires enhanced  $R_{\theta JA}$ .
- (2) If  $V_{CC(\text{est})} \geq V_{CC}(\text{max})$ , then operation between  $V_{CC(\text{est})}$  and  $V_{CC}(\text{max})$  is reliable under these conditions.

**Package UB, 2-Pin SIP**

**For Reference Only – Not for Tooling Use**

(Reference DWG-0000408, Rev. 4)  
Dimensions in millimeters – NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown



Standard Branding Reference View

Line 1 = Logo A, 3 characters  
Lines 2, 3 = 5 characters

Line 1: Logo A, 3-digit Part Number  
Line 2: 4-digit Date Code  
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Branding scale and appearance at supplier discretion

Revision History

Number	Date	Description
–	September 29, 2014	Initial release
1	April 2, 2015	Updated branding info on package drawing
2	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
3	June 21, 2016	Corrected internal discrete capacitor ratings
4	January 16, 2019	Minor editorial updates
5	January 22, 2020	Minor editorial updates
6	February 3, 2022	Updated package drawing (page 12)

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