A4989

Dual Full-Bridge MOSFET Driver with Microstepping Translator

FEATURES AND BENEFITS

- 2-wire step and direction interface
- Dual full-bridge gate drive for N-channel MOSFETs
- Operation over 12 to 50 V supply voltage range
- Synchronous rectification
- Cross-conduction protection
- Adjustable mixed decay
- Integrated sinusoidal DAC current reference
- Fixed off-time PWM current control
- Enhanced low current control when microstepping
- Pin compatible with the A3986

PACKAGE: 38 pin TSSOP (suffix LD)

Approximate footprint

DESCRIPTION

The A4989 is a dual full-bridge gate driver with integrated microstepping translator suitable for driving a wide range of higher power industrial bipolar two-phase stepper motors (typically 30 to 500 W). Motor power is provided by external N-channel power MOSFETs at supply voltages from 12 to 50 V.

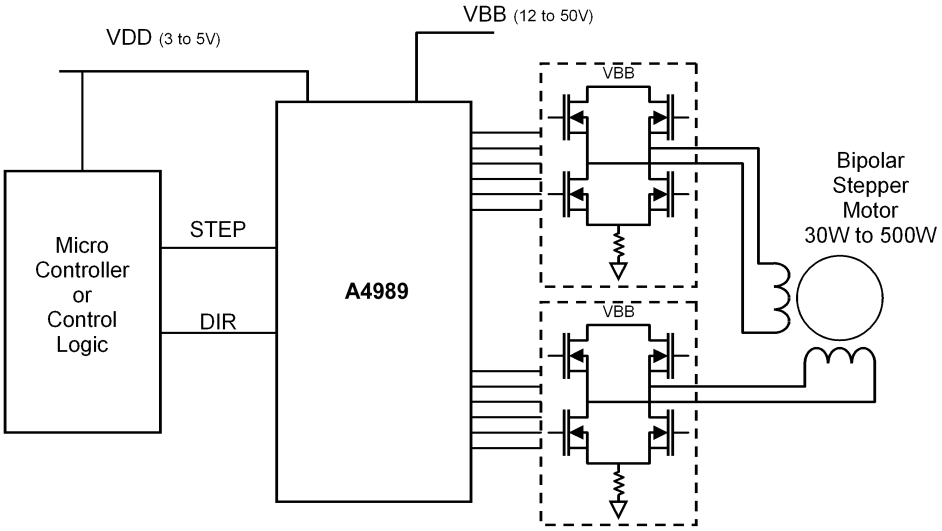
This device contains two sinusoidal DACs that generate the reference voltage for two separate fixed off-time PWM current controllers. These provide current regulation for external power MOSFET full bridges.

Motor stepping is controlled by a two-wire step and direction interface, providing complete microstepping control at full-, half-, quarter-, and sixteenth-step resolutions. The fixed-off time regulator has the ability to operate in slow-, mixed-, or fast-decay modes, which results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of this IC. Simply inputting one pulse on the STEP input drives the motor one step (full, half, quarter, or sixteenth depending on the microstep select input). There are no phase-sequence tables, high frequency control lines, or complex interfaces to program. This reduces the need for a complex microcontroller.

Continued on the next page…

Typical Application Diagram



DESCRIPTION (continued)

The above-supply voltage required for the high-side N-channel MOSFETs is provided by a bootstrap capacitor. Efficiency is enhanced by using synchronous rectification and the power FETs are protected from shoot-through by integrated crossover control and programmable dead time.

In addition to crossover current control, internal circuit protection provides thermal shutdown with hysteresis and undervoltage lockout. Special power-up sequencing is not required.

This component is supplied in a 38-pin TSSOP (package LD). The package is lead (Pb) free, with 100% matte tin leadframe plating.

SELECTION GUIDE

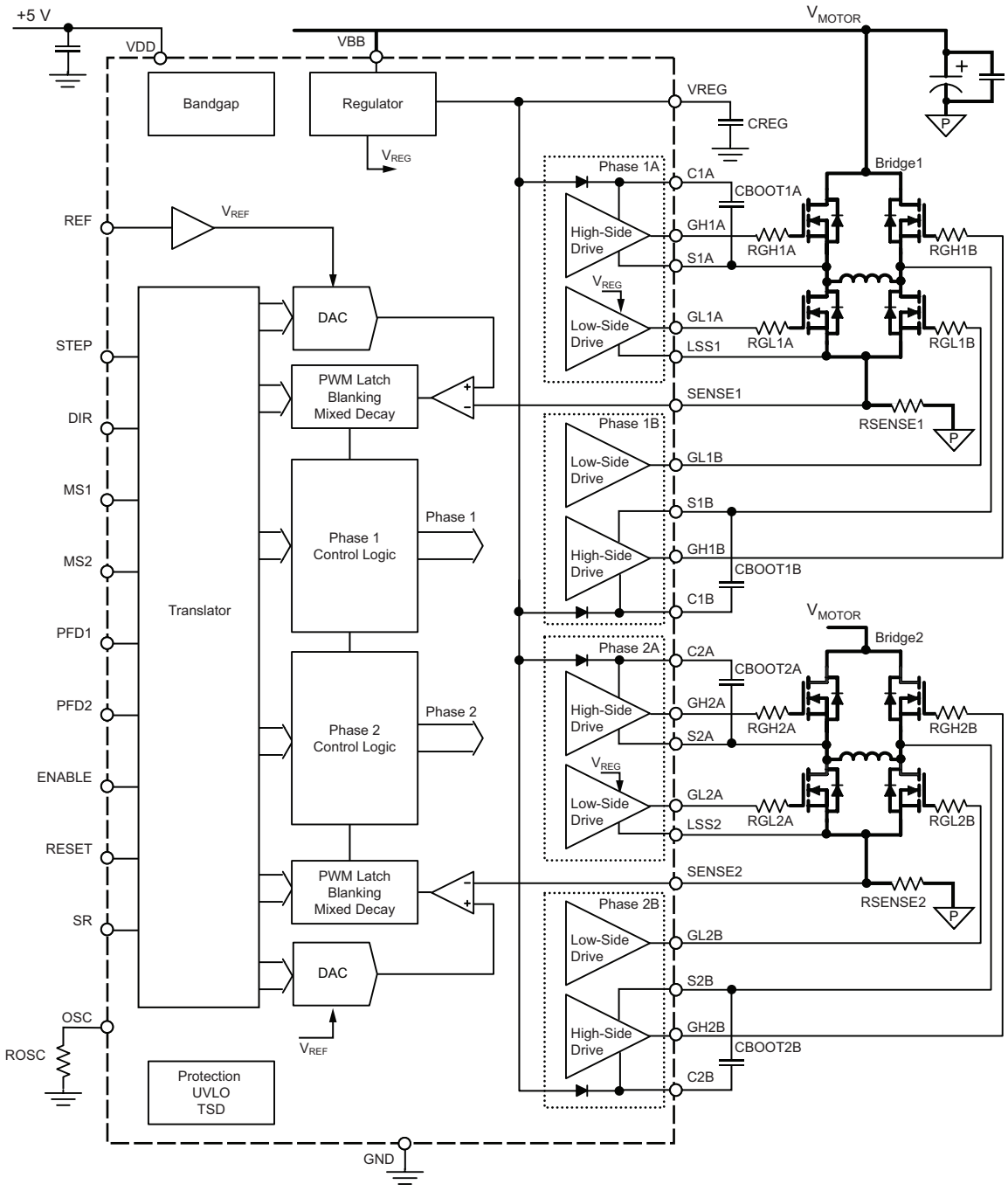
Part Number	Packing
A4989SLDTR-T	Tape and reel, 4000 pieces per reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 7	V
Logic Inputs and Outputs			–0.3 to 7	V
SENSE*x* pins			–1 to 1	V
S*xx* pins			–2 to 55	V
LSS*x* pins			–2 to 5	V
GH*xx* pins			S*xx* to S*xx*+15	V
GL*xx* pins			–2 to 16	V
C*xx* pins			–0.3 to S*xx*+15	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Functional Block Diagram



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 12 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY AND REFERENCE						
Load Supply Voltage Range	V_{BB}		12	–	50	V
Load Supply Current	I_{BB}	R_{OSC} = 10 kΩ, C_{LOAD} = 1000 pF	–	–	10	mA
		ENABLE = High, outputs disabled	–	–	6	mA
Load Supply Idle Current	I_{BBQ}	RESET = 0	–	–	100	µA
Logic Supply Voltage Range	V_{DD}		3.0	–	5.5	V
Logic Supply Current	I_{DD}		–	–	10	mA
Logic Supply Idle Current	I_{DDQ}	RESET = 0	–	–	300	µA
Regulator Output	V_{REG}	I_{REGInt} = 30 mA	11.25	–	13	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_{fBOOT} = 10 mA	0.6	0.8	1	V
GATE OUTPUT DRIVE						
Turn-On Rise Time	t_r	C_{LOAD} = 1000 pF, 20% to 80%	80	120	160	ns
Turn-Off Fall Time	t_f	C_{LOAD} = 1000 pF, 80% to 20%	40	60	80	ns
Turn-On Propagation Delay	$t_{p(on)}$	ENABLE low to gate drive on	–	180	–	ns
Turn-Off Propagation Delay	$t_{p(off)}$	ENABLE high to gate drive off	–	180	–	ns
Crossover Dead Time	t_{DEAD}	R_{OSC} = 10 kΩ,	0.6	–	1.2	µs
Pull-Up On Resistance	$R_{DS(on)UP}$	I_{GH} = –25 mA	30	40	55	Ω
Pull-Down On Resistance	$R_{DS(on)DN}$	I_{GL} = 25 mA	14	19	24	Ω
Short-Circuit Current – Source [1]	$I_{SC(source)}$		–140	–110	–80	mA
Short-Circuit Current – Sink	$I_{SC(sink)}$		160	200	250	mA
GH*x* Output Voltage	V_{GHx}	CBOOT*x* fully charged	V_C – 0.2	–	–	V
GL*x* Output Voltage	V_{GLx}		V_{REG} – 0.2	–	–	V
LOGIC INPUTS						
Input Low Voltage	V_{IL}		–	–	0.3 V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}	–	–	V
Input Hysteresis	V_{IHys}		150	300	–	mV
Input Current [1]	I_{IN}		–1	–	1	µA
RESET Pulse Width [2]	t_{wR}		0.2	–	1	µs

Continued on the next page...

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued) at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 12 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
CURRENT CONTROL						
Blank Time	t_{BLANK}	R_{OSC} = 10 kΩ,	1.2	1.5	1.8	µs
Fixed Off-Time	t_{OFF}	R_{OSC} = 10 kΩ, , SR= High	18.12	–	23.16	µs
Reference Input Voltage	V_{REF}		0.8	–	2	V
Internal Reference Voltage	V_{REFInt}	20 kΩ to V_{DD}	1.9	2.0	2.1	V
Current Trip Point Error [3]	E_{ITRIP}	V_{REF} = 2 V	–	–	±5	%
Reference Input Current [1]	I_{REF}		–3	0	3	µA
Oscillator Frequency	f_{OSC}	R_{OSC} = 10 kΩ	3.2	4	4.8	MHz
PROTECTION						
VREG Undervoltage Lockout	V_{REGUV}	Decreasing V_{REG}	7.5	8	8.5	V
VREG Undervoltage Lockout Hysteresis	$V_{REGUVHys}$		100	200	–	mV
VDD Undervoltage Lockout	V_{DDUV}	Decreasing V_{DD}	2.45	2.7	2.95	V
VDD Undervoltage Lockout Hysteresis	$V_{DDUVHys}$		50	100	–	mV
Overtemperature Shut Down	T_{TSD}	Temperature increasing	–	165	–	°C
Overtemperature Shut Down Hysteresis	T_{TSDHys}	Recovery = T_{TSD} – T_{TSDHys}	–	15	–	°C
CONTROL TIMING						
STEP Low Duration	t_{STEPL}		1	–	–	µs
STEP High Duration	t_{STEPH}		1	–	–	µs
Setup Duration	t_{SU}	Input change to STEP pulse; MS1, MS2, DIR	200	–	–	ns
Hold Duration	t_H	Input change from STEP pulse; MS1, MS2, DIR	200	–	–	ns
Wake Time Duration	t_{WAKE}		1	–	–	ms

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] A RESET pulse of this duration will reset the translator to the Home position without entering Sleep mode.
[3] Current Trip Point Error is the difference between actual current trip point and the target current trip point, referred to full scale (100%) current: $E_{ITRIP} = 100 \times (I_{TRIPActual} - I_{TRIPTarget}) / I_{FullScale\ \%}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB, based on JEDEC standard	51	°C/W
		1-layer PCB with copper limited to solder pads	127	°C/W

*Additional thermal information available on Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

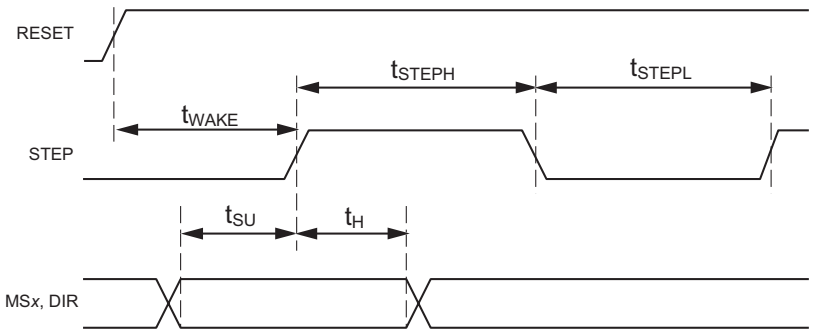


Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS2	MS1	Microstep Resolution
0	0	Full Step
0	1	Half Step
1	0	Quarter Step
1	1	Sixteenth Step

Table 2. Mixed Decay Selection Truth Table

Microstep Setting	Magnitude of Current	PFDx State			
		PFD2 = 0, PFD1 = 0	PFD2 = 0, PFD1 = 1	PFD2 = 1, PFD1 = 0	PFD2 = 1, PFD1 = 1
Full Step (MS2 = 0, MS1 = 0)	Rising	Slow	Slow	Slow	Slow
	Falling	Slow	Slow	Slow	Slow
Half Step (MS2 = 0, MS1 = 1)	Rising	Slow	Slow	Slow	Slow
	Falling	Slow	11%	26%	Fast
1/4 Step (MS2 = 1, MS1 = 0)	Rising	Slow	Step 1: 11%	Step 1: 11%	Step 1: 11%
	Falling	Slow	11%	26%	Fast
1/16 Step (MS2 = 1, MS1 = 1)	Rising	Slow	Steps 1 to 5: 11%	Steps 1 to 5: 11%	Steps 1 to 5: 11%
	Falling	Slow	11%	26%	Fast

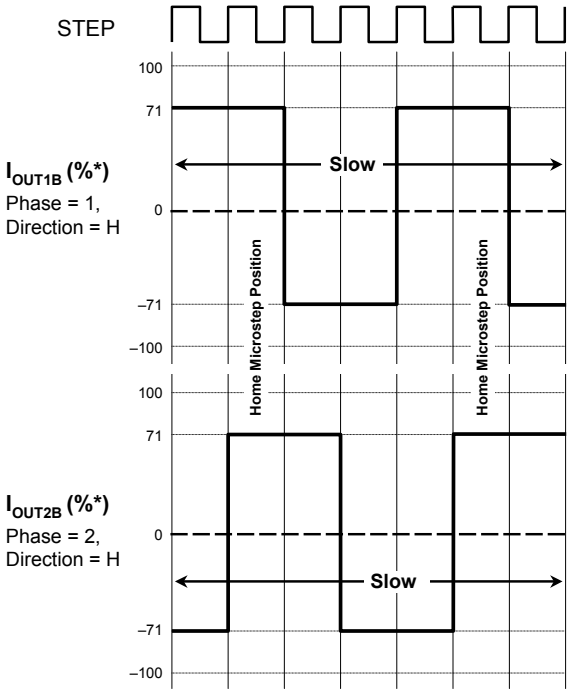
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 3. Step Sequencing Settings

Home microstep position at Step Angle 45°; DIR = H

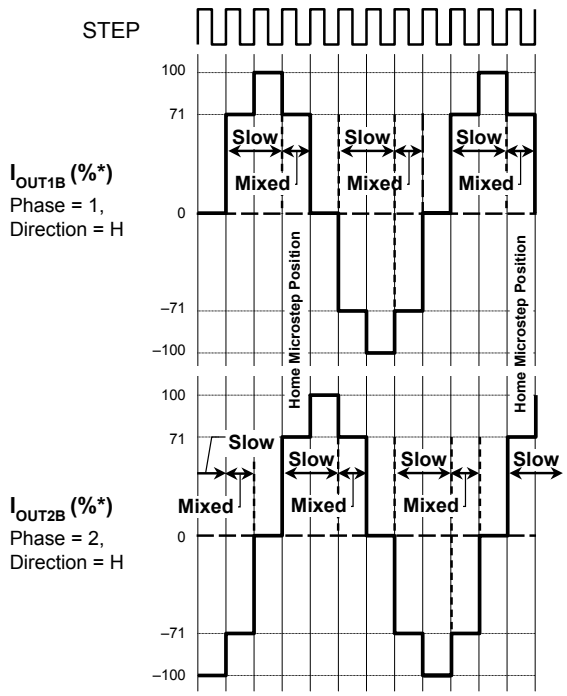
Full Step (#)	Half Step (#)	1/4 Step (#)	1/16 Step (#)	Phase 2 Current (% $I_{TRIP(max)}$)	Phase 1 Current (% $I_{TRIP(max)}$)	Step Angle (°)
	1	1	1	0.00	100.00	0.0
			2	9.38	100.00	5.6
			3	18.75	98.44	11.3
			4	29.69	95.31	16.9
		2	5	37.50	92.19	22.5
			6	46.88	87.50	28.1
			7	56.25	82.81	33.8
			8	64.06	76.56	39.4
1	2	3	9	70.31	70.31	45.0
			10	76.56	64.06	50.6
			11	82.81	56.25	56.3
			12	87.50	46.88	61.9
		4	13	92.19	37.50	67.5
			14	95.31	29.69	73.1
			15	98.44	18.75	78.8
			16	100.00	9.38	84.4
	3	5	17	100.00	0.00	90.0
			18	100.00	–9.38	95.6
			19	98.44	–18.75	101.3
			20	95.31	–29.69	106.9
		6	21	92.19	–37.50	112.5
			22	87.50	–46.88	118.1
			23	82.81	–56.25	123.8
			24	76.56	–64.06	129.4
2	4	7	25	70.31	–70.31	135.0
			26	64.06	–76.56	140.6
			27	56.25	–82.81	146.3
			28	46.88	–87.50	151.9
		8	29	37.50	–92.19	157.5
			30	29.69	–95.31	163.1
			31	18.75	–98.44	168.8
			32	9.38	–100.00	174.4
	5	9	33	0.00	–100.00	180.0
			34	–9.38	–100.00	185.6
			35	–18.75	–98.44	191.3
			36	–29.69	–95.31	196.9
		10	37	–37.50	–92.19	202.5
			38	–46.88	–87.50	208.1
			39	–56.25	–82.81	213.8
			40	–64.06	–76.56	219.4
3	6	11	41	–70.31	–70.31	225.0
			42	–76.56	–64.06	230.6
			43	–82.81	–56.25	236.3
			44	–87.50	–46.88	241.9
		12	45	–92.19	–37.50	247.5
			46	–95.31	–29.69	253.1
			47	–98.44	–18.75	258.8
			48	–100.00	–9.38	264.4
	7	13	49	–100.00	0.00	270.0
			50	–100.00	9.38	275.6
			51	–98.44	18.75	281.3
			52	–95.31	29.69	286.9
		14	53	–92.19	37.50	292.5
			54	–87.50	46.88	298.1
			55	–82.81	56.25	303.8
			56	–76.56	64.06	309.4
4	8	15	57	–70.31	70.31	315.0
			58	–64.06	76.56	320.6
			59	–56.25	82.81	326.3
			60	–46.88	87.50	331.9
		16	61	–37.50	92.19	337.5
			62	–29.69	95.31	343.1
			63	–18.75	98.44	348.8
			64	–9.38	100.00	354.4
	1	1	1	0.00	100.00	360.0

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



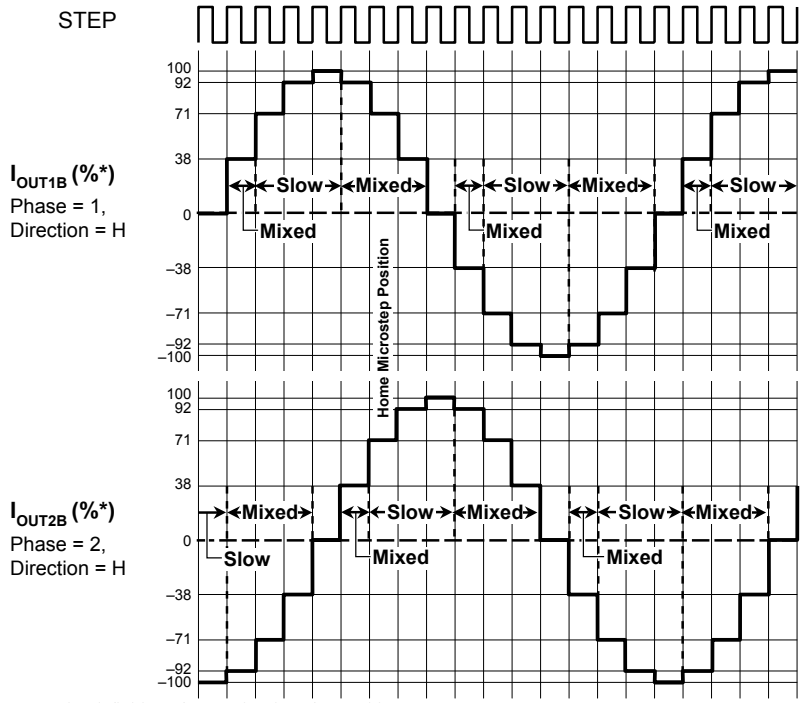
*For precise definition of output levels, refer to table 3

Figure 2. Decay Mode for Full-Step Increments



*For precise definition of output levels, refer to table 3

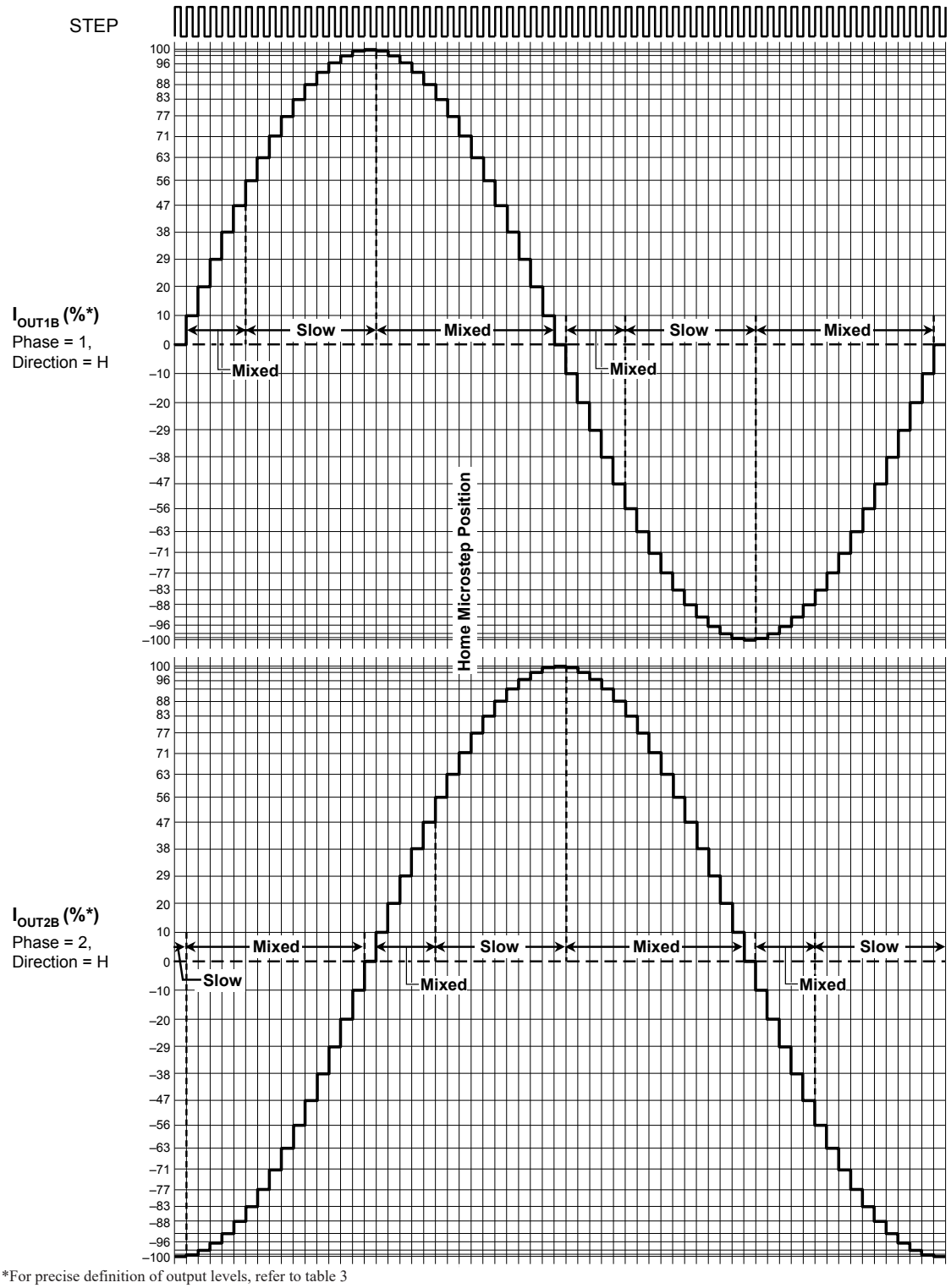
Figure 3. Decay Modes for Half-Step Increments



*For precise definition of output levels, refer to table 3

Figure 4. Decay Modes for Quarter-Step Increments

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



*For precise definition of output levels, refer to table 3

Figure 5. Decay Modes for Sixteenth-Step Increments

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Basic Operation

The A4989 is a complete microstepping FET driver with built-in translator for easy operation with a minimum number of control inputs. It is designed to operate 2-phase bipolar stepper motors in full-, half-, quarter, and sixteenth-step modes. The current in each of the two external power full-bridges, all N-channel MOSFETs, is independently regulated by a fixed off-time PWM control circuit. The full-bridge current at each step is set by the value of an external current sense resistor, R_{SENSEX}, in the ground connection to the bridge, a reference voltage, V_{REF}, and the output of the DAC controlled by the translator.

The use of PWM with N-channel MOSFETs provides the most cost-effective solution for a high efficiency motor drive. The A4989 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are above 10 V, and that there is no cross-conduction (shoot through) in the external bridge.

Specific functions are described more fully in the following sections.

Power Supplies

Two power connections are required. The motor power supply should be connected to VBB to provide the gate drive levels. Power for internal logic is provided by the VDD input. Internal logic is designed to operate from 3 to 5.5 V, allowing the use of 3.3 or 5 V external logic interface circuits.

GND. The ground pin is a reference voltage for internal logic and analog circuits. There is no large current flow through this pin. To avoid any noise from switching circuits, this should have an independent trace to the supply ground star point.

VREG. The voltage at this pin is generated by a low-drop-out linear regulator from the VBB supply. It is used to operate the low-side gate drive outputs, GL*xx*, and to provide the charging current for the bootstrap capacitors, CBOOT*x*. To limit the voltage drop when the charge current is provided, this pin should be decoupled with a ceramic capacitor, CREG, to ground. The value C_{REG} should typically be 40 times the value of the bootstrap capacitor for PWM frequencies up to 14 kHz. Above 14 kHz, the minimum recommended value can be determined from the following formula:

$$C_{REG} > C_{BOOT} \times 3 \times f_{PWM} ,$$

where C_{REG} and C_{BOOT} are in nF, and f_{PWM} is the maximum PWM frequency, in kHz. V_{REG} is monitored, and if the voltage becomes too low, the outputs will be disabled.

REF. The reference voltage, V_{REF}, at this pin sets the maximum (100%) peak current. The REF input is internally limited to 2 V when a 20 kΩ pull-up resistor is connected between VREF and VDD. This allows the maximum reference voltage to be set without the need for an externally generated voltage. An external reference voltage below the maximum can also be input on this pin. The voltage at VREF is divided by 8 to produce the DAC reference voltage level.

OSC. The internal FET control timing is derived from a master clock running at 4 MHz typical. A resistor, ROSC, connected from the OSC pin to GND sets the frequency (in MHz) to approximately:

$$f_{OSC} \approx 100 / (6 + 1.9 \times R_{OSC}) ,$$

where R_{OSC}, in kΩ, is typically between 50 kΩ and 10 kΩ. The master oscillator period is used to derive the PWM off-time, dead time, and blanking time.

Gate Drive

The A4989 is designed to drive external power N-channel MOSFETs. It supplies the transient currents necessary to quickly charge and discharge the external FET gate capacitance in order to reduce dissipation in the external FET during switching. The charge and discharge rate can be controlled using an external resistor , RGx, in series with the connection to the gate of the FET. Cross-conduction is prevented by the gate drive circuits which introduce a dead time, t_{DEAD}, between switching one FET off and the complementary FET on. t_{DEAD} is at least three periods of the master oscillator but can be up to one cycle longer to allow oscillator synchronization.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

C1A, C1B, C2A, and C2B. High-side connections for the bootstrap capacitors, CBOOT*x*, and positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately V_{REG} when the associated output S*xx* terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs. The bootstrap capacitor should be ceramic and have a value of 10 to 20 times the total MOSFET gate capacitance.

GH1A, GH1B, GH2A, and GH2B. High-side gate drive outputs for external N-channel MOSFETs. External series gate resistors can be used to control the slew rate seen at the gate, thereby controlling the *di*/*dt* and *dv*/*dt* at the motor terminals. GH*xx* = 1 (high) means that the upper half of the driver is turned on and will source current to the gate of the high-side MOSFET in the external motor-driving bridge. GH*xx* = 0 (low) means that the lower half of the driver is turned on and will sink current from the external MOSFET's gate circuit to the respective S*xx* pin.

S1A, S1B, S2A, and S2B. Directly connected to the motor, these terminals sense the voltages switched across the load and define the negative supply for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low impedance traces to the MOSFET bridge.

GL1A, GL1B, GL2A, and GL2B. Low-side gate drive outputs for external N-channel MOSFETs. External series gate resistors (as close as possible to the MOSFET gate) can be used to reduce the slew rate seen at the gate, thereby controlling the *di*/*dt* and *dv*/*dt* at the motor terminals. GL*xx* = 1 (high) means that the upper half of the driver is turned on and will source current to the gate of the low-side MOSFET in the external motor-driving bridge. GL*xx* = 0 (low) means that the lower half of the driver is turned on and will sink current from the gate of the external MOSFET to the LSS*x* pin.

LSS1 and LSS2. Low-side return path for discharge of the gate capacitors, connected to the common sources of the low-side external FETs through low-impedance traces.

Motor Control

Motor speed and direction is controlled simply by two logic inputs, and the microstep level is controlled by a further two logic inputs. At power-up or reset, the translator sets the DACs and phase current polarity to the initial Home state (see figures 2 through 5 for home-state conditions) and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level (see table 3 for the current level sequence and current polarity).

The microstep resolution is set by inputs MS1 and MS2 as shown in table 1. If the new DAC level is higher or equal to the previous level, then the decay mode for that full-bridge will normally be slow decay. If the new DAC output level is lower than the previous level, the decay mode for that full bridge will be set by the PFD1 and PFD2 inputs. The full range of settings available is given in table 2. This automatic current-decay selection improves microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

STEP. A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs as well as the direction of current flow in each winding. The size of the increment is determined by the state of the MS*x* inputs.

MS1 and MS2. These Microstep Select inputs are used to select the microstepping format, per table 1. Changes to these inputs do not take effect until the next STEP input rising edge.

DIR. This Direction input determines the direction of rotation of the motor. When low, the direction is "clockwise" and "counterclockwise" when high. A change on this input does not take effect until the next STEP rising edge.

Internal PWM Current Control

Each full-bridge is independently controlled by a fixed off-time PWM current control circuit that limits the load current in the phase to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink MOSFETs are enabled and current flows through the motor winding and the current sense resistor, RSENSE*x*. When the voltage across RSENSE*x* equals the DAC output voltage, the current sense comparator resets the PWM latch, which turns off

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

the source MOSFET (slow decay mode) or the sink and source MOSFETs (fast decay mode). The maximum value of current limiting is set by the selection of R_{SENSE} and the voltage at the REF input, with a transconductance function approximated by:

$$I_{TRIP(max)} = V_{REF}/(8 \times R_{SENSE})$$

The DAC, controlled by the translator, reduces the reference voltage, V_{REF}, in precise steps to produce the required sinusoidal reference levels for the current sense comparator. This limits the phase current trip level, I_{TRIP}, to a portion of the maximum current level, $I_{TRIP(max)}$, defined by:

$$I_{TRIP} = (\%\, I_{TRIP(max)}/100) \times I_{TRIP(max)}$$

See table 3 for $\%\, I_{TRIP(max)}$ at each step.

Fixed Off-Time. The internal PWM current control circuitry uses the master oscillator to control the length of time the power MOSFETs remain off. The off-time, t_{OFF}, is nominally 87 cycles of the master oscillator (21.75 µs at 4 MHz), but may be up to 1 cycle longer to synchronize with the master oscillator.

Blanking. This function blanks the output of the current sense comparator when the outputs are switched by the internal current control. The comparator output is blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes and switching transients related to the capacitance of the load. The blank time, t_{BLANK}, is 6 cycles of the master oscillator (1.5 µs at 4 MHz). Because the t_{BLANK} follows the end of t_{OFF}, no synchronization error occurs.

Dead Time. To prevent cross-conduction (shoot through) in the power full-bridge, a dead time is introduced between switching one MOSFET off and switching the complementary MOSFET on. The dead time, t_{DEAD}, is 3 cycles of the master oscillator (750 ns at 4MHz), but may be up to 1 cycle longer to synchronize with the master oscillator.

ENABLE. This input simply turns off all the power MOSFETs. When set at logic high, the outputs are disabled. When set at logic low, the internal control enables the outputs as required. Inputs to the translator (STEP, DIR, MS1, and MS2) and the internal sequencing logic are all active independent of the ENABLE input state.

RESET. An active-low control input used to minimize power consumption when not in use. This disables much of the internal circuitry, including the output MOSFETs and internal regulator. When set at logic high, allows normal operation and start-up of the device in the home position. When coming out of sleep mode, wait 1 ms before issuing a STEP command, to allow the internal regulator to stabilize. The outputs can also be reset to the home position without entering sleep mode. To do so, pulse the RESET input low, with a pulse width between $t_{wR(min)}$ and $t_{wR(max)}$.

Mixed Decay Operation

Mixed decay is a technique that provides greater control of phase currents while the current is decreasing. When a stepper motor is driven at high speed, the back EMF from the motor will lag behind the driving current. If a passive current decay mode, such as slow decay, is used in the current control scheme, then the motor back EMF can cause the phase current to rise out of control. Mixed decay eliminates this effect by putting the full-bridge initially into fast decay, and then switching to slow decay after some time. Because fast decay is an active (driven) decay mode, this portion of the current decay cycle will ensure that the current remains in control. Using fast decay for the full current decay time (off-time) would result in a large ripple current, but switching to slow decay once the current is in control will reduce the ripple current value. The portion of the off-time that the full-bridge has to remain in fast decay will depend on the characteristics and the speed of the motor.

When the magnitude of the phase current is rising, the motor back EMF will not affect the current control and slow decay may be used to minimize the phase current ripple. The A4989 automatically switches between slow decay, when the current is rising, and mixed decay, when the current magnitude is falling. The portion of the off-time that the full-bridge remains in fast decay is defined by the PFD1 and PFD2 inputs. However, when high VBB voltages are used with motors having low values of DC phase resistance, the minimum current that can be controlled can be higher than the target value required in some microstepping modes. Errors in the average current amplitude delivered to the phases of a motor can lead to positional errors in the holding condition and/or excessive torque ripple and acoustic noise at low speeds.

The conditions for the loss of current control due to this effect are just after a current zero crossing, as the magnitude of the current increases. Introducing mixed decay over the range of steps

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

affected enhances current control. Because the requirements are closely related to the microstep settings used, the relationship between MSx and PFDx is tabulated in table 2 for clarity.

The overall result is an extension of the minimum current control range the 4989 can achieve. The effect can be seen clearly in figures 6 and 7, below.

PFD1 and PFD2. The Percent Fast Decay pins are used to select the portion of fast decay, according to table 2, to be used when mixed decay is enabled. Mixed decay is enabled when a STEP input signal commands an output current that is lower than for the previous step. In mixed decay mode, as the trip point is reached, the A4989 goes into fast decay mode until the specified number of master oscillator cycles has completed. After this fast decay portion, the A4989 switches to slow decay mode for the remainder of the fixed off-time, t_{OFF}.

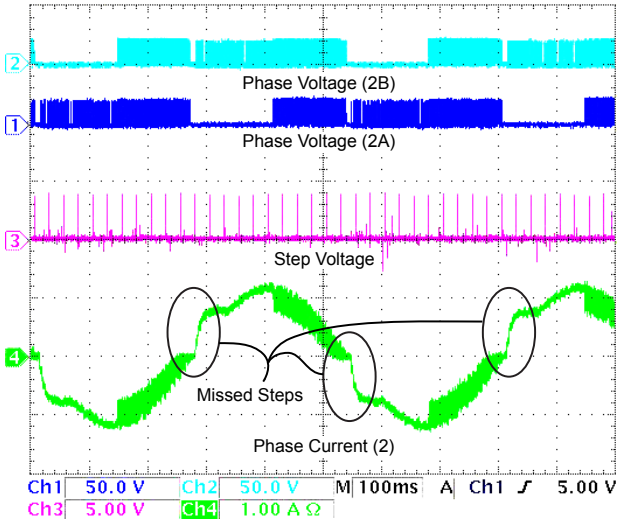


Figure 6. An example of missed steps when $^1/_{16}$ microstepping a motor at low stepping speeds

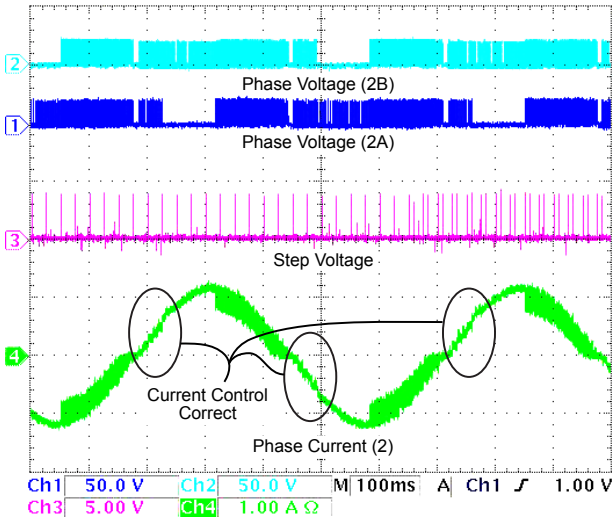


Figure 7. A 4989 driving the same motor as in figure 6, using these settings: MS1=MS2=1, PFD1=PFD2= 1

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Using PFD1 and PFD 2 to select 0% fast decay will effectively maintain the full bridge in slow decay at all times. This option can be used to keep the phase current ripple to a minimum when the motor is stationary or stepping at very low rates.

Selecting 100% fast decay will provide the fastest current control when the current is falling and can help when the motor is being driven at very high step rates.

SR. Input used to set synchronous rectification mode. When a PWM off-cycle is triggered, load current recirculates according to the decay mode selected by the control logic. The synchronous rectification feature turns on the appropriate MOSFETs during the current decay and effectively shorts out the body diodes with the low $R_{DS(ON)}$ of the MOSFET. This lowers power dissipation significantly and eliminates the need for additional Schottky diodes. Synchronous rectification can be set to either active mode or disabled mode.

- **Active Mode** When the SR pin input is logic low, active mode is enabled and synchronous rectification will occur. This mode prevents reversal of the load current by turning off synchronous rectification when a zero current level is detected. This prevents the motor winding from conducting in the reverse direction.
- **Disabled Mode** When the SR pin input is logic high, synchronous rectification is disabled. This mode is typically used when external diodes are required to transfer power dissipation from the power MOSFETs to external, usually Schottky, diodes.

Shutdown Operation. In the event of an overtemperature fault, or an undervoltage fault on VREG, the MOSFETs are disabled until the fault condition is removed. At power-up, and in the event of low voltage at VDD, the undervoltage lockout (UVLO) circuit disables the MOSFETs until the voltage at VDD reaches the minimum level. Once V_{DD} is above the minimum level, the translator is reset to the home state, and the MOSFETs are reenabled.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Current Sensing

To minimize inaccuracies in sensing the I_{PEAK} current level caused by ground-trace IR drops, the sense resistor, RSENSE*x*, should have an independent return to the supply ground star point. For low-value sense resistors, the IR drops in the sense resistor PCB traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_{SENSEx} due to their contact resistance.

Thermal Protection

All drivers are turned off when the junction temperature reaches 165°C typical. This is intended only to protect the A4989 from failures due to excessive junction temperatures. Thermal protection will not protect the A4989 from continuous short circuits. Thermal shutdown has a hysteresis of approximately 15°C.

Circuit Layout

Because this is a switch-mode application, where rapid current changes are present, care must be taken during layout of the application PCB. The following points are provided as guidance for layout. Following all guidelines will not always be possible. However, each point should be carefully considered as part of any layout procedure.

Ground connection layout recommendations:

1. Decoupling capacitors for the supply pins VBB, VREG, and VDD should be connected independently close to the GND pin and not to any ground plane. The decoupling capacitors should also be connected as close as possible to the corresponding supply pin.

2. The oscillator timing resistor ROSC should be connected to the GND pin. It should not be connected to any ground plane, supply common, or the power ground.

3. The GND pin should be connected by an independent low impedance trace to the supply common at a single point.

4. Check the peak voltage excursion of the transients on the LSS pin with reference to the GND pin using a close grounded (tip and barrel) probe. If the voltage at LSS exceeds the absolute maximum specified in this datasheet, add additional clamping, capacitance, or both between the LSS pin and the AGND pin.

Other layout recommendations:

1. Gate charge drive paths and gate discharge return paths may carry transient current pulses. Therefore, the traces from GH*xx*, GL*xx*, S*xx*, and LSS*x* should be as short as possible to reduce the inductance of the circuit trace.

2. Provide an independent connection from each LSS pin to the common point of each power bridge. It is not recommended to connect LSS directly to the GND pin. The LSS connection should not be used for the SENSE connection.

3. Minimize stray inductance by using short, wide copper runs at the drain and source terminals of all power FETs. This includes motor lead connections, the input power bus, and the common source of the low-side power FETs. This will minimize voltages induced by fast switching of large load currents.

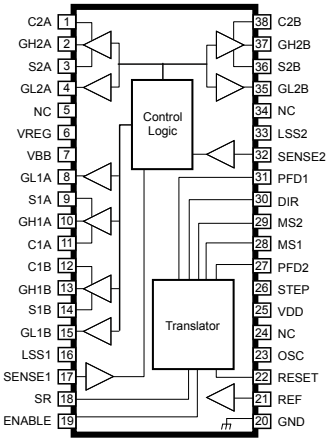
4. Consider the use of small (100 nF) ceramic decoupling capacitors across the source and drain of the power FETs to limit fast transient voltage spikes caused by trace inductance.

The above are only recommendations. Each application is different and may encounter different sensitivities. Each design should be tested at the maximum current, to ensure any parasitic effects are eliminated.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pinout Diagram



Terminal List Table

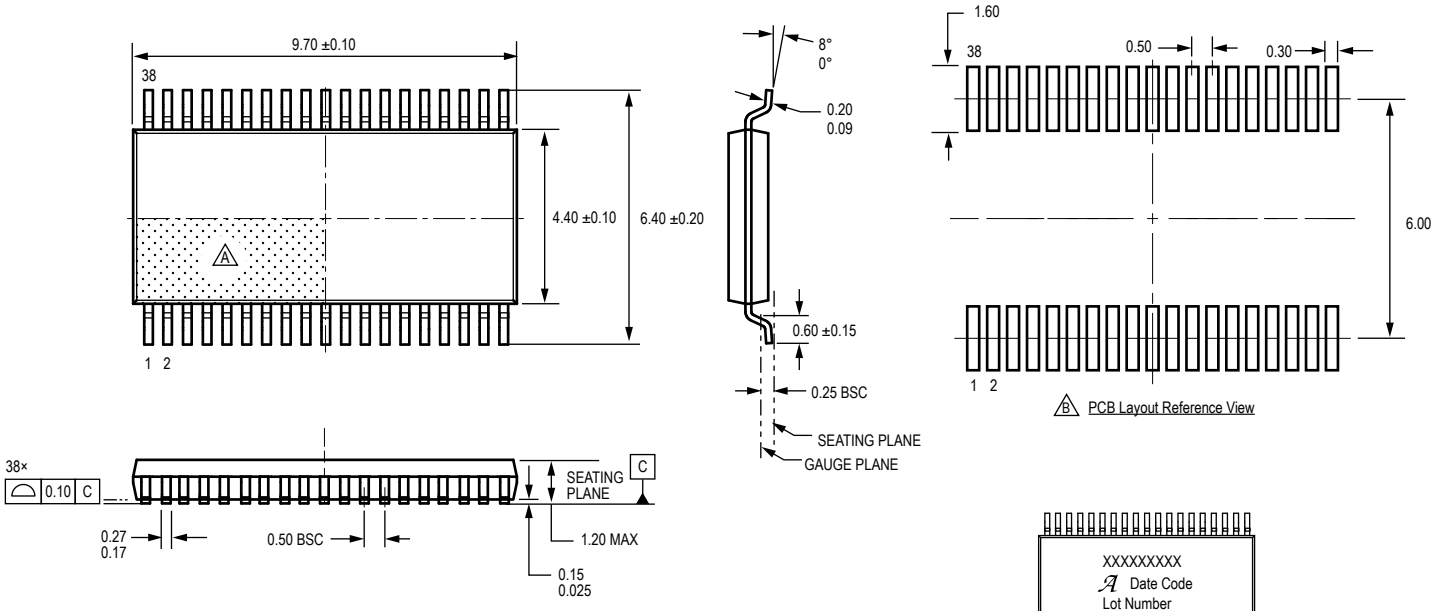
Number	Name	Description
1	C2A	Phase 2 bootstrap capacitor drive A connection
2	GH2A	Phase 2 high-side gate drive A
3	S2A	Phase 2 motor connection A
4	GL2A	Phase 2 low-side gate drive A
5	NC	No internal connection
6	VREG	Regulator decoupling capacitor connection
7	VBB	Motor supply voltage
8	GL1A	Phase 1 low-side gate drive A
9	S1A	Phase 1 motor connection A
10	GH1A	Phase 1 high-side gate drive A
11	C1A	Phase 1 bootstrap capacitor drive A connection
12	C1B	Phase 1 bootstrap capacitor drive B connection
13	GH1B	Phase 1 high-side gate drive B
14	S1B	Phase 1 motor connection B
15	GL1B	Phase 1 low-side gate drive B
16	LSS1	Phase 1 low-side source connection
17	SENSE1	Phase 1 bridge current sense input
18	SR	Synchronous rectification enable
19	ENABLE	Output enable
20	GND	Ground
21	REF	Reference voltage
22	RESET	Reset input
23	OSC	Oscillator input, ROSC resistor connection
24	NC	No internal connection
25	VDD	Logic supply voltage
26	STEP	Step input
27	PFD2	Percent Fast Decay input 2
28	MS1	Microstep Select input 1
29	MS2	Microstep Select input 2
30	DIR	Direction input
31	PFD1	Percent Fast Decay input 1
32	SENSE2	Phase 2 bridge current sense input
33	LSS2	Phase 2 low-side source connection
34	NC	No internal connection
35	GL2B	Phase 2 low-side gate drive B
36	S2B	Phase 2 motor connection B
37	GH2B	Phase 2 high-side gate drive B
38	C2B	Phase 2 bootstrap capacitor drive B connection

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LD Package, 38-Pin TSSOP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 BD-1)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference pad layout (reference IPC SOP50P640X110-38M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

C Standard Branding Reference

Lines 1, 2, 3 = 13 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: First 8 characters of Assembly Lot Number

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
2	April 10, 2020	Minor editorial updates
3	April 5, 2022	Updated package drawing (page 17)
4	April 3, 2023	Minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com