Mobile Phone Xenon Photoflash Capacitor Charger With IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Mobile Phone Xenon Photoflash Capacitor Charger With IGBT Driver

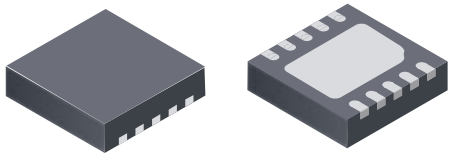
Features and Benefits

- Low quiescent current draw (0.01 µA in shutdown mode)
- Primary-side output voltage sensing; no resistor divider required
- User-adjustable current limit from 0.6 to 1.8 A
- 1.1 V logic (V_{HI}(min)) compatibility
- Integrated IGBT driver
- System enable input
- Optimized for mobile phone, 1-cell Li+ battery applications
- Zero-voltage switching for lower loss
- >75% efficiency
- Regulation feature to maintain the output voltage
- Charge complete indication
- Integrated 40 V DMOS switch

Applications

- Mobile phone flash
- Digital and film camera flash

Package: 10-contact DFN with exposed thermal pad (package EJ)



Approximate Scale 1:1

Description

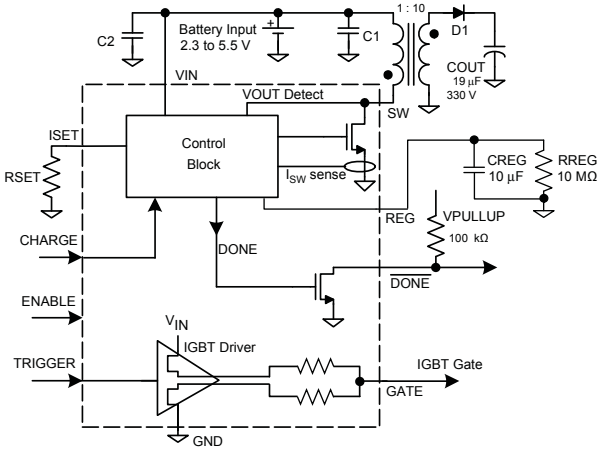
The Allegro® A8733 Xenon photoflash charger IC is designed to meet the needs of ultra-low power, small form factor cameras, particularly camera-phones.

The charge time is adjustable by setting the charge current limit from 0.6 to 1.8 A maximum. By using primary-side voltage sensing, the need for a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. To extend battery life, the A8733 features very low supply current draw—typically 0.01 µA in shutdown mode.

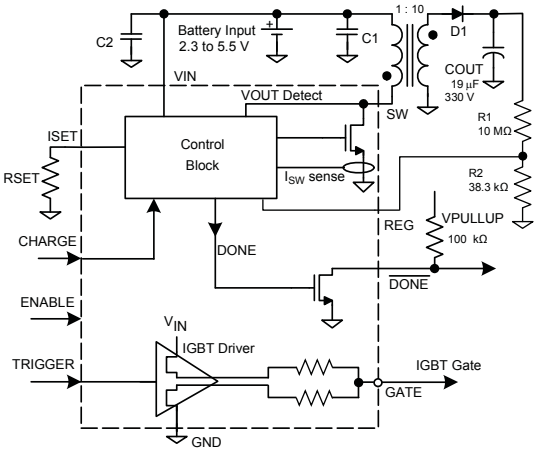
The A8733 has a system enable pin to prevent accidental activation of CHARGE or TRIGGER signals The charge and trigger voltage logic thresholds are set at 1.1 V_{HI}(min) to support applications implementing low voltage control logic.

The A8733 is available in a 10-contact 3 mm × 3 mm DFN package with a 0.75 nominal overall package height, and an exposed pad for enhanced thermal performance.

Typical Applications



Application 1. Maintaining output voltage by predicting the output voltage droop (REG pin connected to primary -side RC network).



Application 2. Maintaining output target voltage by directly monitoring the output voltage (REG pin connected to a secondary-side resistor divider).

Selection Guide

Part Number	Package	Packing
A8733EEJTR-T	10-contact DFN	Tape and reel, 1500 pieces per reel

*Contact Allegro for additional ordering information.

Absolute Maximum Ratings

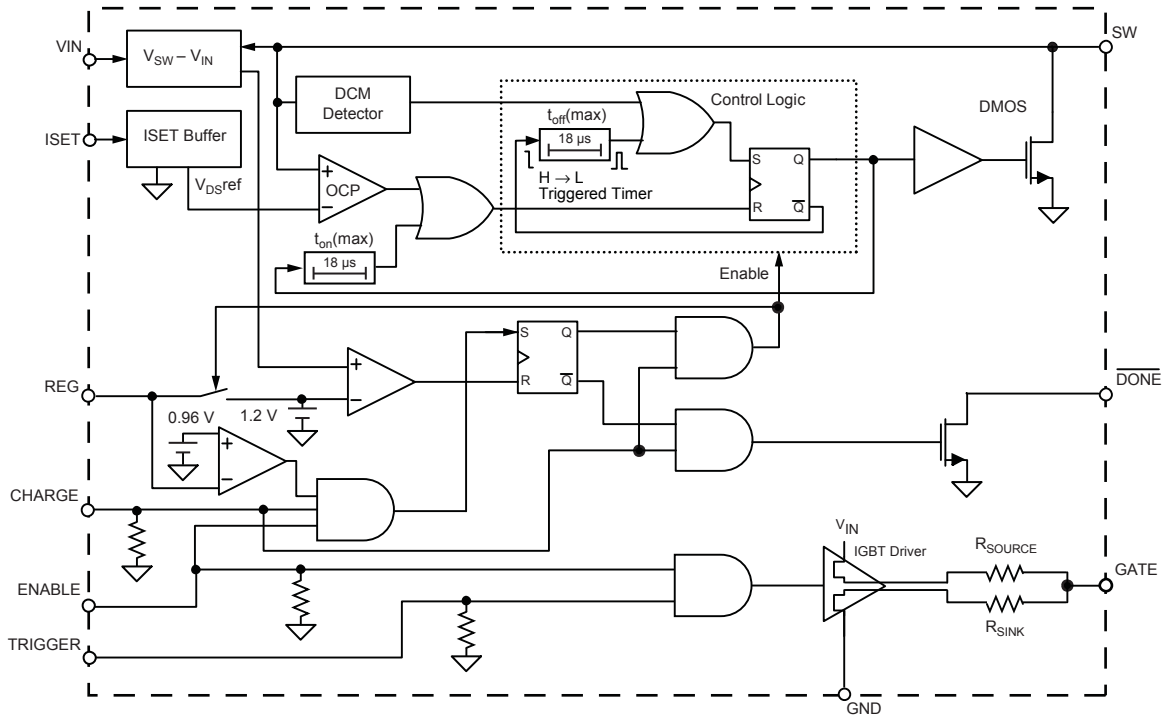
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 40	V
VIN Pin	V_{IN}		–0.3 to 6.0	V
$\overline{\text{ENABLE}}$, CHARGE, TRIGGER, $\overline{\text{DONE}}$ Pins		Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

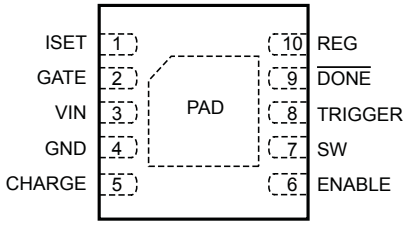
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer PCB with 0.88 in.^{2} area of 2 oz. copper each side, based on JEDEC standard	65	ºC/W
		On 4-layer PCB based on JEDEC standard	45	ºC/W

*Additional thermal information available on Allegro website.

Functional Block Diagram



Pin-out Diagram



(Contacts-Down View)

Terminal List Table

Number	Name	Function
1	ISET	Sets the maximum switch current; connect an external resistor to GND to set the desired peak current
2	GATE	IGBT gate drive (sink and source)
3	VIN	Input voltage; connect to a 2.3 to 5.5 V battery supply; use same battery supply connected to transformer.
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging
6	ENABLE	System enable input; when ENABLE = low, both CHARGE and TRIGGER are disabled
7	SW	Drain connection of internal power MOSFET switch; connect to transformer primary winding
8	TRIGGER	IGBT input trigger
9	$\overline{\text{DONE}}$	Pulls low when output reaches target value and CHARGE pin is high; goes high during charging or whenever CHARGE pin is low
10	REG	Output voltage regulation pin; connect to external resistor and capacitor to regulate output voltage (see Output Regulation section for details)
–	PAD	Exposed pad for enhanced thermal dissipation; connect to ground plane

ELECTRICAL CHARACTERISTICS valid at V_{IN} = 3.6 V, ENABLE = V_{IN}, R_{SET} = 26.7 kΩ, I_{SWlim} = 1.2 A, and T_A=25°C, except ● indicates specifications guaranteed from −40°C to 85°C unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VIN Voltage Range	V_{IN}		●	2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising		–	2.05	2.2	V
UVLO Hysteresis	$V_{INUVhys}$			–	150	–	mV
VIN Supply Current	I_{IN}	Shutdown (ENABLE = low, CHARGE = low, and TRIGGER = low)		–	0.01	0.5	µA
		Standby current (ENABLE = high, CHARGE = high, $\overline{DONE}$ = low)		–	0.7	–	mA
		Charging (ENABLE = high and CHARGE = high)		–	2	–	mA
Current Limits							
Switch Current Limit[1]	$I_{SWlimMAX}$	R_{SET} = 18 kΩ		1.62	1.8	1.98	A
	$I_{SWlimMIN}$	R_{SET} = 55 kΩ		–	0.6	–	A
SW / ISET Current Ratio	I_{SW}/I_{SET}	CHARGE = high		–	28	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	CHARGE = high		–	1.2	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$			–	1000	–	Ω
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 1.2 A		–	0.25	–	Ω
Switch Leakage Current[2]	I_{SWlk}	V_{SW} = V_{IN}(max)	●	–	–	2	µA
		Combined V_{IN} and SW leakage current at T_A=25°C V_{IN}= 5.5 V in Shutdown		–	–	0.5	µA
ENABLE Input Current	I_{ENABLE}	V_{ENABLE} = V_{IN}		–	36	–	µA
ENABLE Logic Input[2]	V_{ENABLE}	High, over input supply range	●	1.1	–	–	V
		Low, over input supply range	●	–	–	0.4	V
ENABLE Pull-Down Resistor Value	R_{ENPD}			–	100	–	kΩ
CHARGE Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}		–	36	–	µA
CHARGE Logic Input[2]	V_{CHARGE}	High, over input supply range	●	1.1	–	–	V
		Low, over input supply range	●	–	–	0.4	V
CHARGE Pull-Down Resistor Value	R_{CHPD}			–	100	–	kΩ
CHARGE ON/OFF Delay	t_{CH}	Time between CHARGE = 1 and charging enabled		–	20	–	us
Maximum Switch-Off Timeout	t_{offMAX}			–	18	–	µs
Maximum Switch-On Timeout	t_{onMAX}			–	18	–	µs
$\overline{DONE}$ Output Leakage Current[2]	I_{DONElk}			–	–	1	µA
$\overline{DONE}$ Output Low Voltage[2]	V_{DONEL}	32 µA into $\overline{DONE}$ pin		–	–	100	mV
Output Comparator Trip Voltage[2]	$V_{OUTTRIP}$	Measured as V_{SW} – V_{IN}	●	31	31.5	32	V
Output Comparator Overdrive	V_{OUTOV}	Pulse width = 200 ns (90% to 90%)		–	200	400	mV
dV/dt Threshold of ZVS Comparator	dV/dt	Measured at SW pin		–	20	–	V/µs
Regulation							
REG Voltage When Charging Completes	$V_{REG(H)}$	CHARGE = high, at $\overline{DONE}$ → low transition		1.15	1.2	1.25	V
REG Voltage Threshold for Regulation	$V_{REG(L)}$	CHARGE = high, at $\overline{DONE}$ = low		–	0.96	–	V
REG Output Current Drive Capability	I_{REG}	CHARGE = high, at $\overline{DONE}$ = high, V_{SW} – V_{IN} = 30 V, V_{REG} = 1.0 V		–	50	–	µA

Continued on the next page…

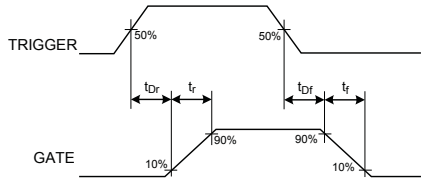
ELECTRICAL CHARACTERISTICS (continued) valid at V_{IN} = 3.6 V, ENABLE = V_{IN}, R_{SET} = 26.7 kΩ, I_{SWlim} = 1.2 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
IGBT Driver							
TRIGGER Logic Input[2]	$V_{TRIG(H)}$	Input = logic high, over input supply range	●	1.1	–	–	V
	$V_{TRIG(L)}$	Input = logic low, over input supply range	●	–	–	0.4	V
TRIGGER Pull-Down Resistor	R_{TRIGPD}			–	100	–	kΩ
GATE Resistance to VIN	$R_{SrcDS(on)}$	V_{IN} = 3.6 V, V_{GATE} =1.8 V, $V_{TRIGGER}$ = Logic high		–	10	–	Ω
GATE Resistance to GND	$R_{SnkDS(on)}$	V_{IN} = 3.6 V, V_{GATE} = 1.8 V, $V_{TRIGGER}$ = Logic low		–	30	–	Ω
Propagation Delay (Rising)	t_{Dr}	Measurement taken at pin, C_L= 6500 pF, V_{IN}= 3.6 V		–	110	–	ns
Propagation Delay (Falling)	t_{Df}			–	140	–	ns
Output Rise Time	t_r			–	125	–	ns
Output Fall Time	t_f			–	360	–	ns

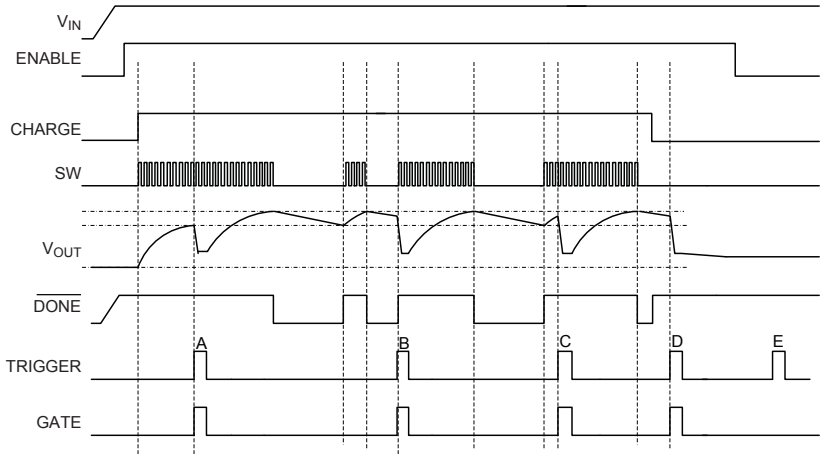
[1]Current limit guaranteed by design and correlation to static test. Refer to application section for peak current in actual circuits.

[2]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.

IGBT Drive Timing Definition



Operation Timing Diagram



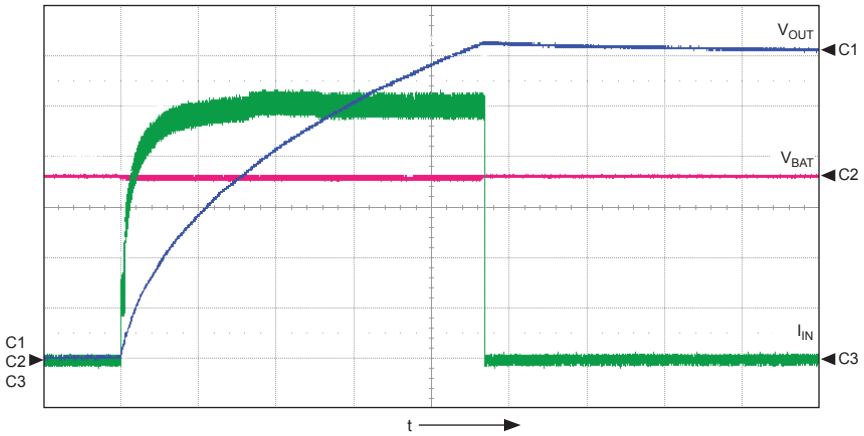
Trigger 'A' arrives during charging process. GATE is enabled.
Trigger 'B' arrives during regulation mode while not refreshing. GATE is enabled.
Charging resumes once $\overline{\text{DONE}}$ pins goes high.
Trigger 'C' arrives during regulation mode while refreshing. GATE is enabled.
Trigger 'D' arrives when ENABLE is high but CHARGE pin is low. GATE is enabled.
Trigger 'E' arrives when ENABLE is low. GATE is disabled.

Performance Characteristics

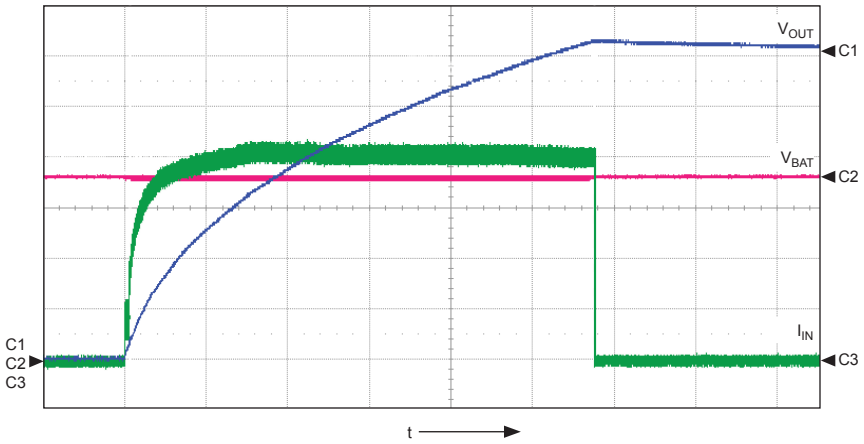
Charging Time at Various Peak Current Levels

Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{BAT}	1 V
C3	I_{IN}	100 mA
t	time	200 ms
Conditions	**Parameter**	**Value**
	V_{BAT}	3.6 V
	C_{OUT}	20 µF

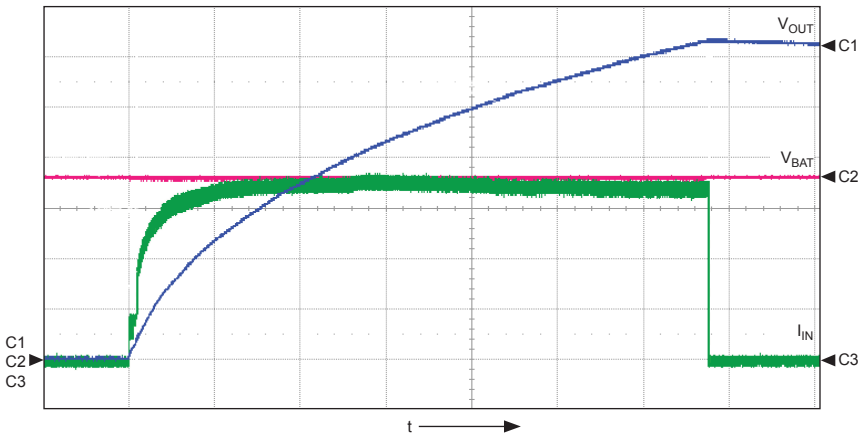
Conditions	Parameter	Value
	R_{SET}	26.7 kΩ
	I_{SWlim}	≈1.2 A

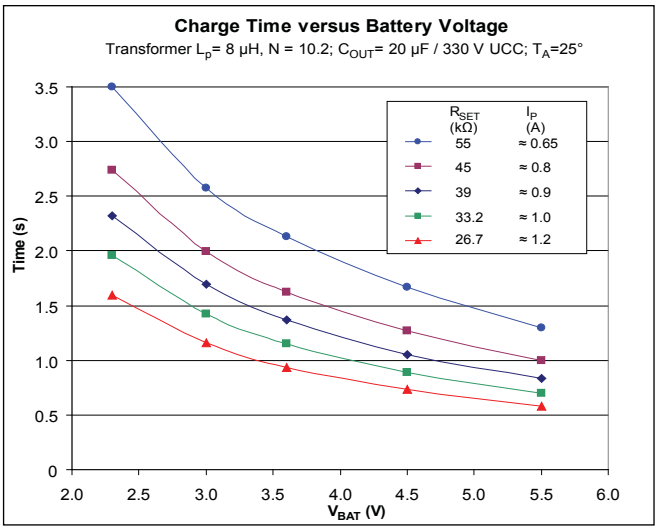


Conditions	Parameter	Value
	R_{SET}	33.2 kΩ
	I_{SWlim}	≈1.0 A

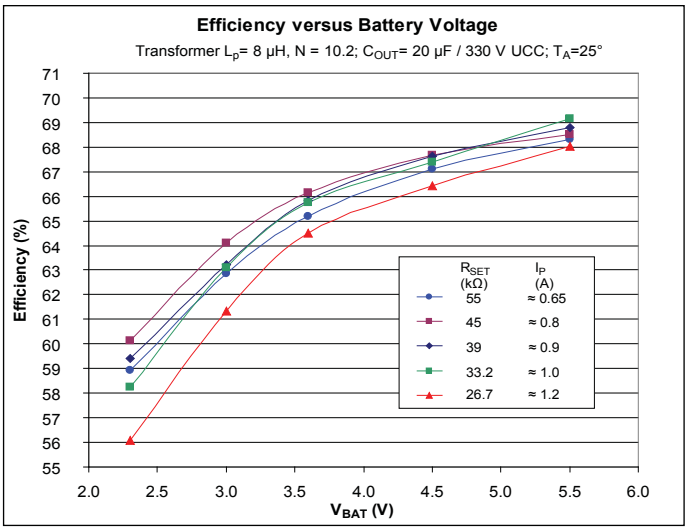


Conditions	Parameter	Value
	R_{SET}	39 kΩ
	I_{SWlim}	≈0.9 A

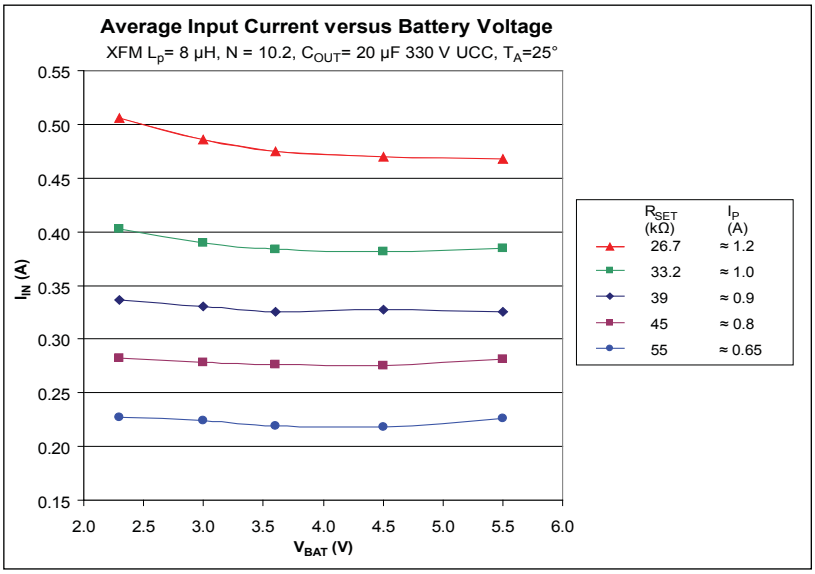




C_{OUT}= 20 µF. For larger or smaller capacitances, charging time scales proportionally.



Special low-profile transformer with relatively low inductance (Lp= 8 µH) and high winding resistance (Rp = 0.37 Ω). Higher efficiency can be achieved by using transformers with higher Lp, which reduces switching frequency and therefore switching loses, and lower resistance, which reduces conduction losses.



An increase in I_{SWlim} with respect to V_{BAT} actually keeps the average input current roughly constant throughout the battery voltage range. Normally, if I_{SWlim} is kept constant, the average current will drop as V_{BAT} goes higher.

Application Information

General Operation Overview

The charging operation is started by a low-to-high signal on the ENABLE pin, provided that V_{IN} is above the V_{UVLO} level. It is strongly recommended to keep the ENABLE pin at logic low during power-up.

- When ENABLE input is low, the device will be completely shut down and will not respond to any input at CHARGE or TRIGGER pin.
- When ENABLE is high and CHARGE is low, the device will remain in low-power standby mode. However, the IGBT gate driver will now respond to TRIGGER input signal.
- When ENABLE is high and CHARGE is high, the device will start switching to charge-up the output capacitor. Charging will stop after the output target voltage is reached.

Pulling either the CHARGE pin or the ENABLE pin low during a charging process stops the charging immediatey.

The $\overline{\text{DONE}}$ open-drain indicator is pulled low when CHARGE is high and target output voltage is reached. The primary peak current is set by RSET connected across ISET. When a charging cycle is initiated, the transformer primary side current, $I_{Primary}$, ramps up linearly at a rate determined by the combined effect of the battery voltage, V_{BAT}, and the primary side inductance, $L_{Primary}$. When $I_{Primary}$ reaches the current limit, I_{SWLIM}, the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, COUT, from the secondary winding. The secondary side current drops linearly as COUT charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period, t_{offMAX} (18 µs), whichever occurs first.

The A8733 senses output voltage indirectly on the primary side. This eliminates need for high voltage feedback resistors required for secondary sensing. Flyback converter stops switching when output voltage reaches:

$$V_{OUT} = K \times N - V_D , \quad (1)$$

where K = 31.5 typically, N is the transformer turns ratio, and V_D is the forward drop of the output diode (approximately 1 to 2 V).

Output Voltage Regulation

The A8733 can also be used to regulate output voltage within a predetermined window. In this mode, connect a capacitor, CREG, and resistor, RREG, from the REG pin to GND (refer to the figure Application 1). When CHARGE is held high, the voltage monitoring circuit of the A8733 is always active, irrespective of the REG pin voltage level.

Voltage Regulation Using Predicitive Droop The A8733 uses a technique called *Predictive Droop* for regulating the output capacitor voltage after the completion of a charging cycle. When the target output voltage is reached, the converter stops charging and output capacitor voltage droops due to leakage current. An external resistor and capacitor connected from the REG pin to ground will provide an RC discharge time constant. This time constant can be selected to mirror the droop rate of the output capacitor. When voltage at the REG pin drops to 80% of the reference value, the converter starts charging again and brings the output capacitor back to target voltage again.

The time required for an R_{REG}-C_{REG} network to discharge from V_0 to V_T is given by:

$$T = R_{REG} \times C_{REG} \times \ln(V_0 / V_T) . \quad (2)$$

For example, if C_{REG} = 10 µF, R_{REG} = 10 MΩ and V_0/V_T = 1.25, then T = 22 seconds. Assuming that the RC-discharge characteristic of the output capacitor

matches that at the REG pin, we can predict that the output voltage has drooped 20%, and therefore it is time to recharge the output capacitor.

By implementing a Predictive Droop technique, no additional leakage paths are introduced on the secondary side, which helps to keep power losses to a minimum. By intentionally making the RC discharge time constant of the REG pin shorter than that of the output capacitor, we can regulate the output voltage to a window tighter than the default 20% hysteresis.

Voltage Regulation Using Direct Sensing If direct sensing from the secondary side is desired, connect the REG pin to a resistor divider network across the output capacitor to enable output regulation. In this case, the charging cut-off is still controlled by primary side sensing (charging stops when reflected voltage across transformer primary winding reaches 31.5 V), but the regulation threshold is controlled by the secondary side sensing. When the CHARGE pin is high, and the sensed output voltage falls below the lower V_{REG} threshold, the flyback converter charges the output capacitor again until the primary side sensing stops further charging. This cycle repeats till the CHARGE pin is pulled low.

The benefit of this method is that a lower output voltage can be selected independently, simply by changing the resistor divider ratio. For example, given R_1=10 MΩ, R_2= 33.2 kΩ, and $V_{REG(L)}$= 0.96 V, then:

$$V_{OUT}(\text{Low}) = V_{REG(L)} \times (R_1/R_2 + 1) = 290 \text{ V} . \quad (3)$$

Selection of Switching Current Limit

The A8733 features continuously adjustable peak switching current between 0.6 and 1.8 A. This is done by selecting the value of an external resistor RSET, connected from the ISET pin to GND, which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} according to the following equations:

$$I_{SWlim} = I_{SET} \times K = V_{SET} / R_{SET} \times K , \quad (4)$$

where K = 28000 when battery voltage is 3.6 V.

In real applications, the actual switching current limit is affected by input battery voltage, and also the transformer primary inductance, Lp. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{GND(INT)}), \quad (5)$$

where:

$R_{SET(INT)}$ is the internal resistance of the I_{SET} pin (1 kΩ typical),

$R_{GND(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and

$K = (K' + V_{IN} \times K'')$, with $K' = 24350$ and $K'' \approx 1040$ at $T_A = 25°C$. Then,

$$I_{SWlim} = I_{SET} \times K + V_{BAT} / L_P \times t_D , \quad (6)$$

where t_D is the delay in SW turn-off (0.1 µs typical).

Figure 2 can be used to determine the relationship between R_{SET} and I_{SWlim} at various battery voltages.

Smart Current Limit (Optional)

With the help of some simple external logic, the user can change the charging current according to the battery voltage. For example, assume that I_{SET} is normally 36 µA (for I_{SWlim} = 1.0 A). Referring to figure 3, when the battery voltage drops below 2.5 V, the signal at BL (battery-low) goes high. The resistor RBL, connecting BL to the ISET pin, then injects 10 µA into RSET. This effectively reduces ISET current to 26 µA (for I_{SWLIM} = 0.73 A). A disadvantage of the above method is that the 10 µA current is always flowing whenever the BL signal goes high.

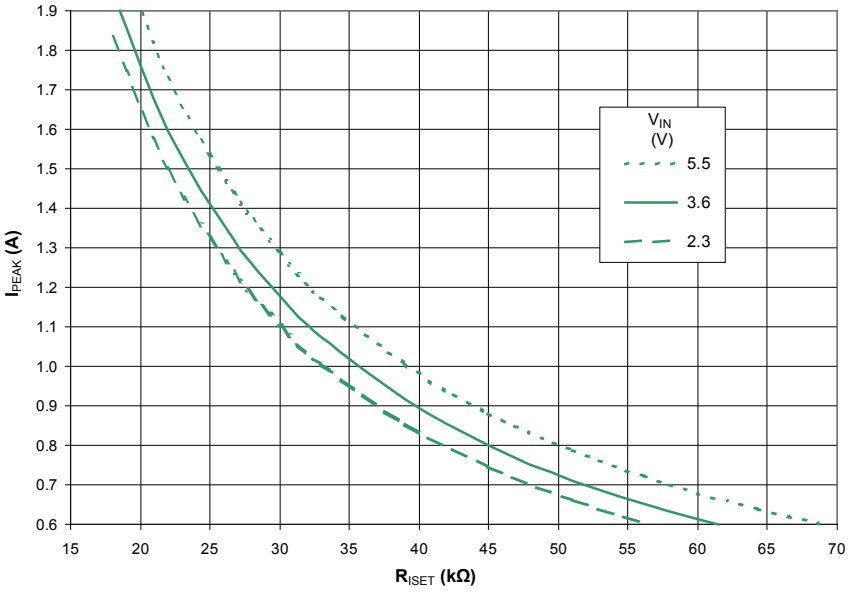


Figure 2. Peak Current versus ISET resistance at various input voltages. $T_A \approx 22°C$, transformer L_P = 8.2 µH.

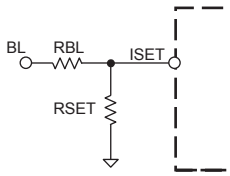


Figure 3. Smart Current Limit reference circuit

Timer Mode and Fast Charging Mode

The A8733 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process The relationship of Timer Mode and Fast Charging Mode is shown in figure 4.

The IC operates in Timer Mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 15 to 20 V. Timer Mode is a fixed period, 18 µs, off-time control. One advantage of having Timer Mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer Mode interval is shown in figure 5.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging Mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to

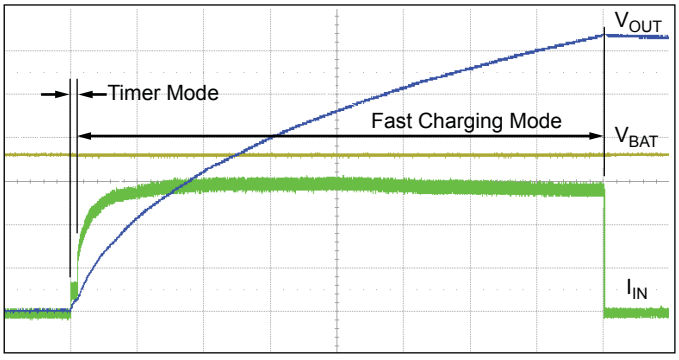


Figure 4. Timer Mode and Fast Charging Mode. t =200 ms/div, V_{OUT} =50 V/div, V_{BAT} =1 V/div., I_{IN} =100 mA/div., V_{BAT} =3.6 V, C_{OUT} =20 µF/330 V, R_{SET}=46 kΩ (I_{SWlim}≈0.75 A).

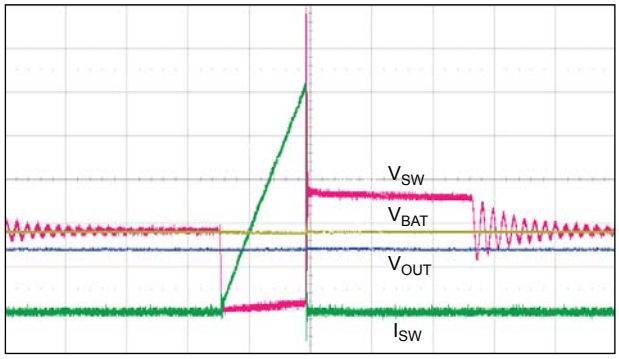


Figure 5. Timer Mode expanded view. V_{OUT} ≤ 14 V, t = 2 µs / div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

0 V. This enables Fast-Charging Mode to start earlier than previously possible, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 6.

During Fast-Charging Mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 7.

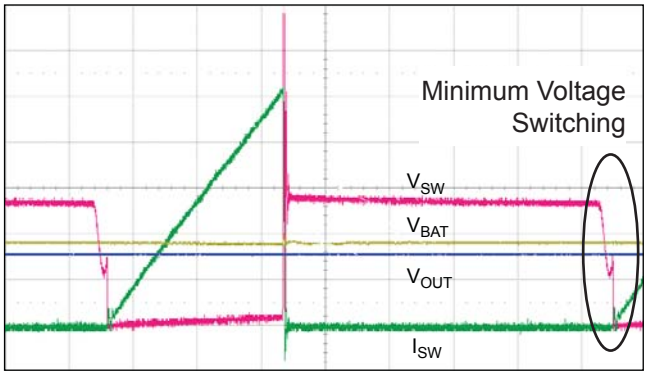


Figure 6. Minimum voltage switching. $V_{OUT} \geq 15$ V; t =1 µs/div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

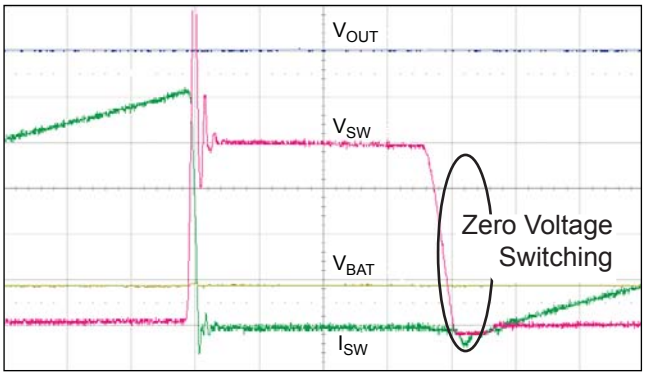


Figure 7. Zero voltage switching. V_{OUT} = 120 V. t = 0.2 µs/div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

Transformer Selection

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P \quad , \tag{7}$$

$$V_{OUT} = 31.5 \times N - V_d \quad , \tag{8}$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, L_P, determines the on-time of the switch:

$$t_{on} = (-L_P / R) \times \ln(1 - I_{SWlim} \times R / V_{IN}) \quad , \tag{9}$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{IN} \quad . \tag{10}$$

3. The secondary inductance, L_S, determines the off-time of the switch. Given:

$$L_S / L_P = N \times N \text{ , then}$$

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} \tag{11}$$

$$= (I_{SWlim} \times L_P \times N) / V_{OUT} \quad . \tag{12}$$

The minimum pulse width for t_{off} determines what is the minimum L_P required for the transformer. For

example, if I_{SWlim} = 0.7 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 9 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in figure 8.

In general, choosing a transformer with a larger L_P results in higher efficiency (because a larger L_P means lower switch frequency and hence lower switching loss). But transformers with a larger L_P also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Component Selection

Selection of the flyback transformer should be based on the peak current, according to the following table:

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)
0.6 to 1.2	TDK	LDT565630T-003	10.5
0.9 to 1.6	TDK	LDT565630T-001	6
0.6 to 1.6	Tokyo Coil	T-16-024A	12.8
0.6 to 1.8	Tokyo Coil	T-15-154M	14.2

Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the absolute maximum specification on the SW pin (refer to the Absolute Maximum Ratings table). An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, CIN. During initial timer mode the device operates with 18 µs off-time. The resonant period caused by the input filter inductor and capacitor should be at least 2 times greater or smaller than the 18 µs timer period, to reduce input ripple current during this period.

The resonant period is given by:

$$T_{RES} = 2\,\pi\,(L_{IN} \times C_{IN})^{1/2}\,. \qquad (13)$$

It is recommended to use at least 4.7 µF / 6.3 V to decouple the battery input, V_{BAT}, at the primary of the transformer. Decouple the VIN pin using

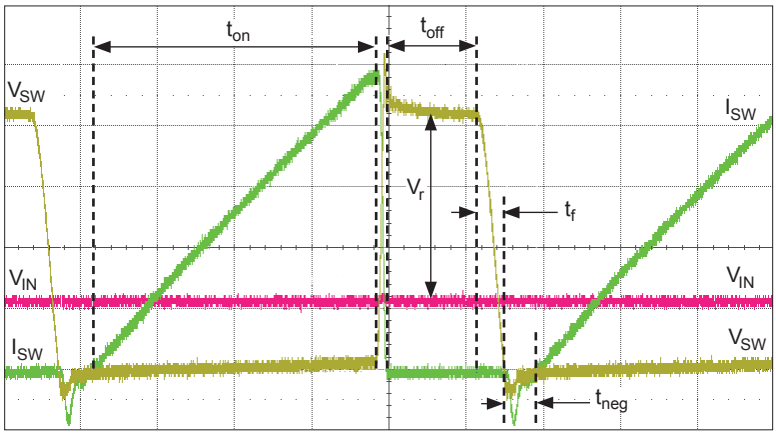


Figure 8. Pulse width relationship definitions.

0.1 µF / 6.3 V bypass capacitor. This configuration is illustrated in figure 9.

Output Diode Selection

Choose the rectifying diodes, D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diode, V_{RDPeak} , occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{RDPeak} = V_{OUT} + N \times V_{BAT} . \quad (14)$$

The peak current of the rectifying diode, I_{DPeak}, is calculated as:

$$I_{DPeak} = I_{Primary\_Peak} / N . \quad (15)$$

Layout Guidelines

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side).

- Use short, thick traces for connections to the transformer primary and the SW pin.
- It is important that the $\overline{\text{DONE}}$ signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup.
- High voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.
- Avoid ground plane underneath transformer secondary and diode to minimize parasitic capacitance.
- For low threshold logic (<1.2 V), add 1 nF capacitors across the CHARGE and TRIGGER pins to GND to avoid malfunction due to noise.

Refer to the figures on the following page for a recommended layout.

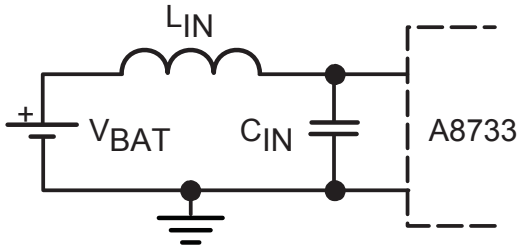
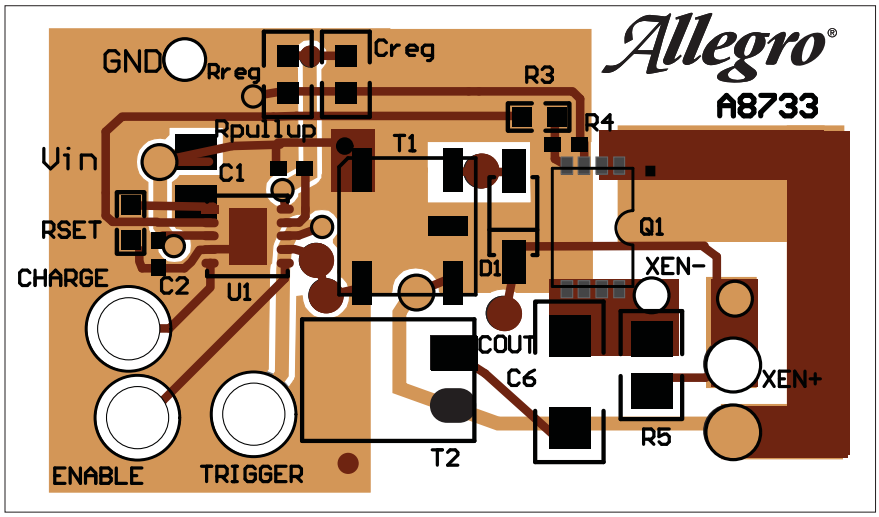
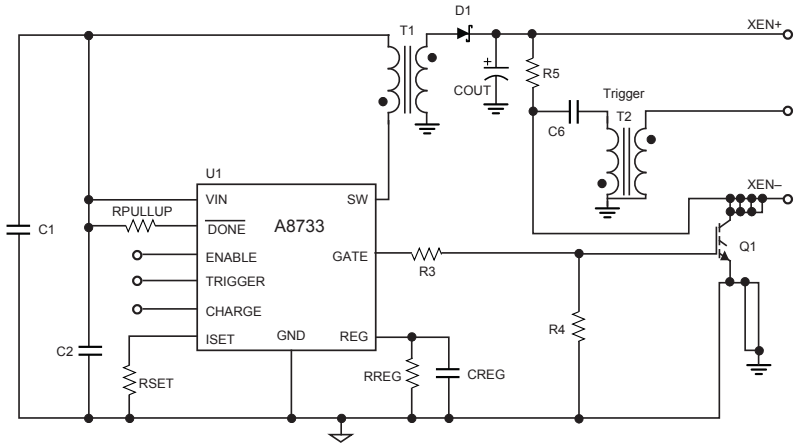


Figure 9. Typical input selection with input inductance. Inductance, L_{IN}, may ba an input filter inductor or inductance due to long wires in the test setup.

Application 1

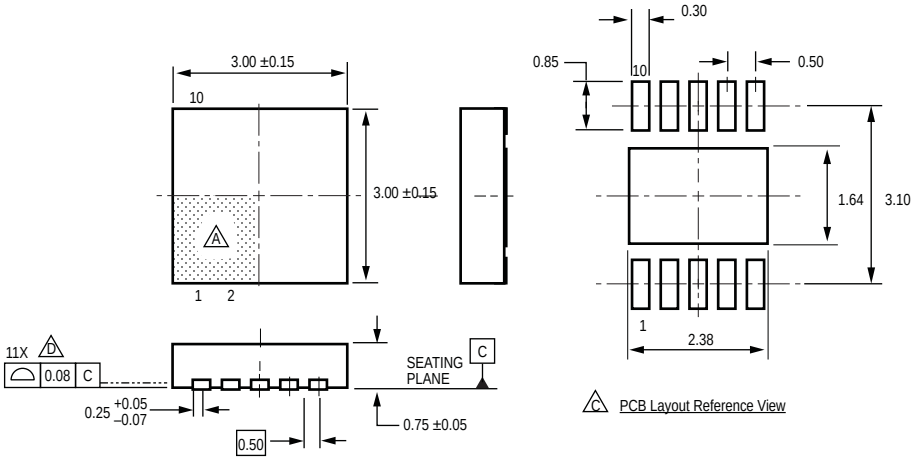


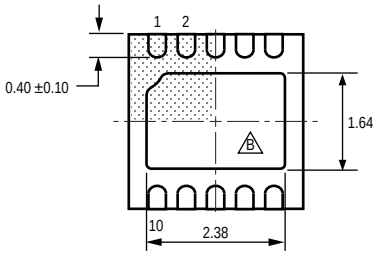


Component Table for Application Circuits on Page 1

Component	Rating	Part Number	Source
C1, Input Capacitor	4.7 µF, ±10%, 6.3 V, X5R ceramic capacitor (0805)	JMK212BJ475K	Taiyo Yuden
C2, Bypass capacitor	0.1 µF, ±10%, 6.3 V X7R ceramic capacitor (0603)		
COUT, Photoflash Capacitor	80 µF / 330 V	EPH-331E--800A030S	Chemi-Con
D1, Output Diode	800 V	FV02R80	Origin
	2 × 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
RSET	36 kΩ, 1%		
RPULLUP	100 kΩ		
CREG (application 1 only)	10 µF / 6.3 V		
RREG (application 1 only)	10 MΩ		
R1 (application 2 only)	10 MΩ, high voltage		
R2 (application 2 only)	38.3 kΩ (0603)		
T1, Transformer	Refer to Component Selection section		

Package EJ, 3 mm x 3 mm 10-Contact DFN
with Exposed Thermal Pad





For Reference Only
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Miscellaneous format changes

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