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## ***Fixed Gate Drive Xenon Photoflash Charger***

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### **Discontinued Product**

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

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**NOTE:** For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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## Fixed Gate Drive Xenon Photoflash Charger

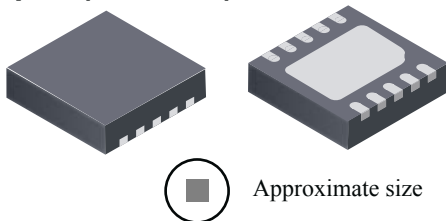
### Features and Benefits

- Low quiescent current draw (0.5  $\mu$ A max in shutdown mode)
- Primary-side output voltage sensing; no resistive divider required
- User-adjustable current limit from 0.4 to 0.9 A
- 1.1 V logic ( $V_{IH(min)}$ ) compatibility
- Integrated constant voltage IGBT driver with separate sink and source
- Optimized for mobile phone, 1-cell Li+ battery applications
- Zero-voltage switching for lower loss
- >75% efficiency
- Charge Complete indication
- Independent charge/trigger control
- Integrated 40 V DMOS switch

### Applications

- Mobile phone flash
- Digital and film camera flash

**Package: 10-contact TDFN with exposed thermal pad (suffix EJ)**



### Description

The Allegro® A8738 Xenon photoflash charger IC is designed to meet the needs of ultra-low power, small form factor cameras, particularly camera-phones.

This device integrates a fixed regulator to precisely control the IGBT flash current across a wide range of battery voltages, providing a 3 V, gate drive. The IGBT driver also has separate source and sink connections, for flexibility in controlling IGBT rise and fall times.

The charge current time is adjustable by setting the charge current limit from 0.4 to 0.9 A maximum. By using primary-side voltage sensing, the a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. To extend battery life, the A8738 features very low supply current draw, typically 0.5  $\mu$ A maximum in shutdown mode.

The charge and trigger voltage logic thresholds are set at 1.1 V ( $V_{IH(min)}$ ) to support applications implementing low voltage control logic.

The device is available in a 10-contact, 3 mm  $\times$  3 mm TDFN package with exposed pad for enhanced thermal performance. It is lead (Pb) free, with 100% matte-tin leadframe plating.

### Typical Application

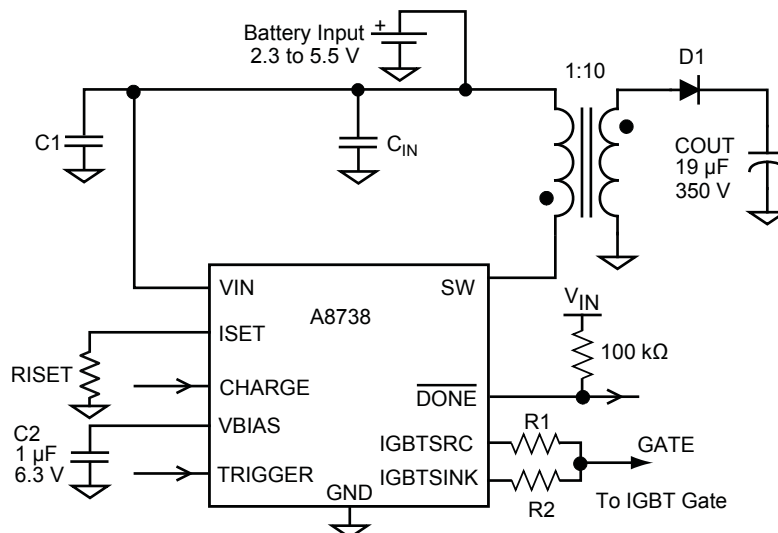


Figure 1. Typical application circuit

**Selection Guide**

Part Number	IGBT Drive Voltage $V_{IGBT}(V)$	Packing	Package
A8738EEJTR-T	3	1500 pieces per 7-in. reel	10-contact TDFN

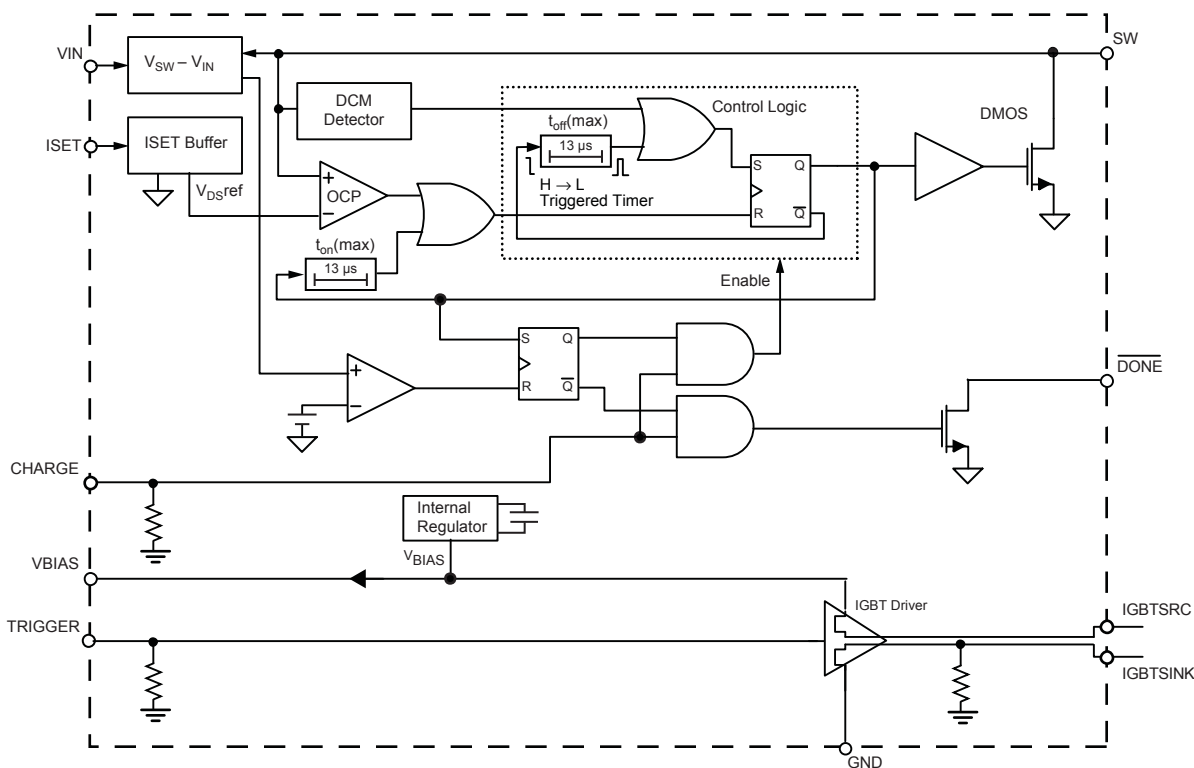
**Absolute Maximum Ratings**

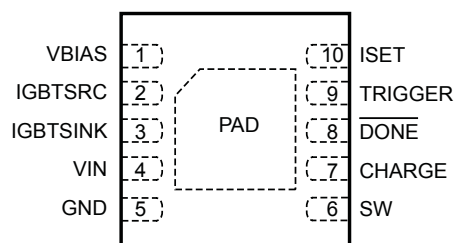
Characteristic	Symbol	Notes	Rating	Units
SW Pin	$V_{SW}$	DC voltage ( $V_{SW}$ is self-clamped by an internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 $\mu J$ at frequency = 400 kHz.)	–0.3 to 40	V
VIN Pin	$V_{IN}$		–0.3 to 6.0	V
Logic and Input Pins	$V_I$	Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to $V_{IN} + 0.3$	V
VBIAS Pin	$V_{BIAS}$		–0.3 to 6.0	V
IGBT SRC and IGBT SINK Pins	$V_{IGBT}$		–0.3 to $V_{BIAS} + 0.3$	V
Operating Ambient Temperature	$T_A$	Range E	–40 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	$T_{stg}$		–55 to 150	°C

**Thermal Characteristics**

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC standard	45	°C/W
		On 2-layer PCB with 0.88 in. <sup>2</sup> 2-oz. copper each side, based on JEDEC standard	65	°C/W

\*Additional thermal information available on the Allegro website

**Functional Block Diagram**

**Pin-out Diagram**

(Top View)

**Terminal List Table**

Name	Number	Function
CHARGE	7	Pull high to initiate charging; pull low to enter low-power standby mode.
$\overline{\text{DONE}}$	8	Pulls low when output reaches target value and CHARGE pin is high; goes high during charging or whenever CHARGE pin is low. Connect an external pull-up resistor to VIN.
GND	5	Ground connection.
IGBTSINK	3	IGBT driver gate drive sink output.
IGBTSRC	2	IGBT driver gate drive source output.
ISET	10	Set the maximum switch current. Connect an external resistor to GND to program the desired peak switch current.
PAD	–	Exposed pad for enhanced thermal dissipation. Connect to GND plane.
SW	6	Drain connection of internal power MOSFET switch; connect to transformer primary winding.
TRIGGER	9	IGBT input trigger.
VIN	4	Input voltage; connect to a 2.3 to 5.5 V input supply. Decouple this pin with 0.1 $\mu\text{F}$ capacitor.
VBIAS	1	Output of internal 3 V regulated supply. Connect a 1 $\mu\text{F}$ / 6.3 V capacitor from this pin to GND.

**ELECTRICAL CHARACTERISTICS** Valid at  $V_{IN} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$  except • indicates specifications guaranteed from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  ambient unless otherwise specified

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
V <sub>IN</sub> Voltage Range <sup>1</sup>	V <sub>IN</sub>		•	2.3	–	5.5	V
UVLO Enable Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> rising		–	2.05	2.2	V
UVLO Hysteresis	V <sub>UVLOhys</sub>			–	150	–	mV
VIN Supply Current	I <sub>IN</sub>	Shutdown, CHARGE = TRIGGER = 0		–	0.01	0.5	μA
		Charging completed (regulating V <sub>BIAS</sub> )		–	0.8	–	mA
		During charging (CHARGE = VIN)		–	2.8	–	mA
Current Limit							
Switch Current Limit <sup>2</sup>	I <sub>SWLIMmax</sub>	R <sub>SET</sub> = 37.4 kΩ		0.8	0.9	1.0	A
	I <sub>SWLIMmin</sub>	R <sub>SET</sub> = 85 kΩ		–	0.4	–	A
SW/ISET Ratio	I <sub>SW</sub> /I <sub>SET</sub>	R <sub>SET</sub> = 37.4 kΩ; CHARGE = 1		–	28	–	kA/A
ISET Charging Pin Voltage	V <sub>SET</sub>	R <sub>SET</sub> = 37.4 kΩ; CHARGE = 1, I <sub>SW</sub> = 0 A (SW disconnected)		–	1.2	–	V
ISET Pin Internal Resistance	R <sub>SET(INT)</sub>			–	1000	–	Ω
Switch Resistance	R <sub>DS(on)</sub>			–	0.25	–	Ω
Switch Leakage Current <sup>1</sup>	I <sub>SWLEAK</sub>	V <sub>SW</sub> = V <sub>IN(max)</sub>	•	–	–	2	μA
		Combined V <sub>IN</sub> and SW leakage current at T <sub>A</sub> = 25°C, V <sub>IN</sub> = 5.5 V in Shutdown		–	–	0.5	μA
TRIGGER/CHARGE Input Current	I <sub>INPUT</sub>	V <sub>CHARGE</sub> = V <sub>TRIGGER</sub> = V <sub>IN</sub>		–	36	–	μA
Logic Input High <sup>1</sup>	V <sub>IH</sub>	CHARGE and TRIGGER pins; High over full V <sub>IN</sub> range	•	1.1	–	–	V
Logic Input Low <sup>1</sup>	V <sub>IL</sub>	CHARGE and TRIGGER pins; Low over full V <sub>IN</sub> range	•	–	–	0.4	V
TRIGGER/CHARGE Pull-down	R <sub>PULLDOWN</sub>	Internal pull-down resistor		–	100	–	kΩ
CHARGE On/Off Delay	t <sub>CH</sub>	Time between CHARGE = 1 and charging enabled		–	20	–	μs
Switch Off Timeout	t <sub>OFFMAX</sub>			–	13	–	μs
Switch On Timeout	t <sub>ONMIN</sub>			–	13	–	μs
$\overline{\text{DONE}}$ Output Leakage Current	I <sub>DONEIK</sub>			–	–	1	μA
$\overline{\text{DONE}}$ Output Low Voltage	V <sub>DONEL</sub>	32 μA into $\overline{\text{DONE}}$ pin		–	–	100	mV
Output Comparator Trip Voltage <sup>1</sup>	V <sub>OUTTRIP</sub>	Measured as V <sub>SW</sub> – V <sub>IN</sub>	•	31	31.5	32	V
Output Comparator Overdrive	V <sub>OUTOV</sub>	140 ns pulse width (90% to 90%)		–	200	400	mV
dV/dt Threshold for ZVS Comparator	dV/dt	Measured at SW pin		–	20	–	V/μs
IGBT Driver							
IGBT Drive Voltage	V <sub>IGBT</sub>			–	3	–	V
IGBT Source Resistance	R <sub>SOURCE</sub>	V <sub>BIAS</sub> = 3 V, I <sub>GBTSINK</sub> = 1.5 V		–	5	–	Ω
IGBT Sink Resistance	R <sub>SINK</sub>	I <sub>GBTSINK</sub> = 1.5 V		–	6	–	Ω
IGBT Sink Pull-Down Resistor	R <sub>Gsink</sub>	Internal pull-down resistor on IGBTSINK		–	500	–	kΩ

Continued on the next page...

**ELECTRICAL CHARACTERISTICS (continued)** Valid at  $V_{IN} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$  except • indicates specifications guaranteed from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  ambient unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
TRIGGER Propagation Delay, Rising	$t_{Dr}$	IGBTSRC and IGBTSINK tied together, measurement taken at pin; $R_{GATE} = 12\ \Omega$ , $C_L = 6500\text{ pF}$	–	30	–	ns
TRIGGER Propagation Delay, Falling	$t_{Df}$		–	30	–	ns
Output Rise Time	$t_r$		–	70	–	ns
Output Fall Time	$t_f$		–	70	–	ns

<sup>1</sup>Specifications over the range  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  guaranteed by design and characterization.

<sup>2</sup>Current limit guaranteed by design and correlation to static test. Refer to Applications Information section for peak current in actual circuits.

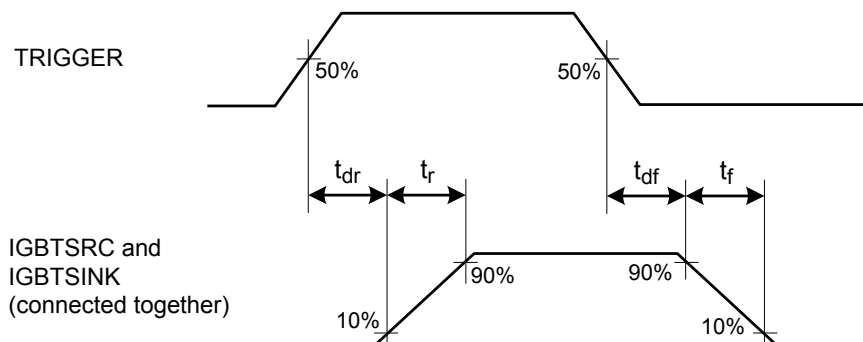
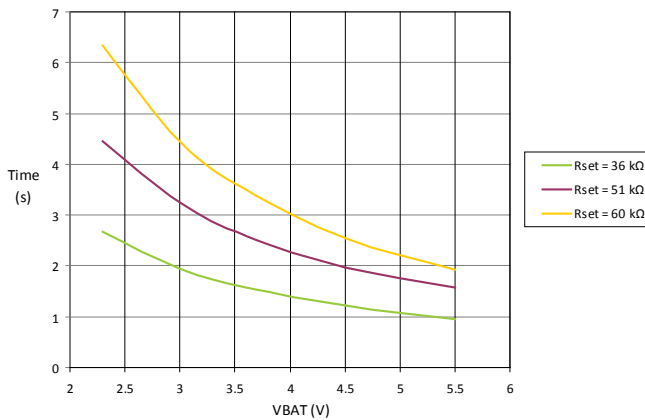


Figure 2. IGBT Drive Timing Definition

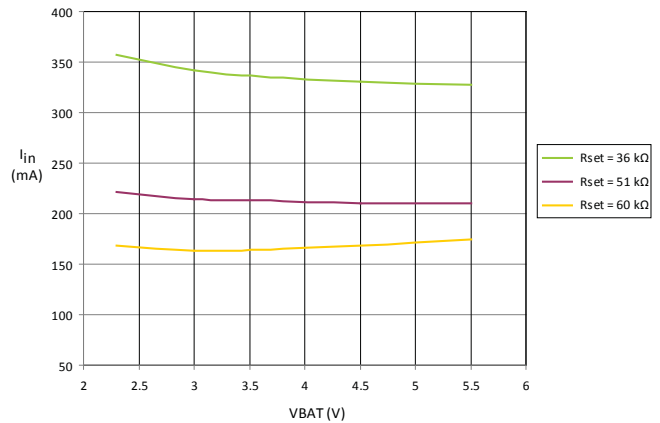
## Characteristic Performance

Test conditions:  $L_P = 6.5 \mu\text{H}$ ,  $N = 10.2$ ,  $C_{OUT} = 21 \mu\text{F}$ ,  $V_{OUT} = 330 \text{ V}$

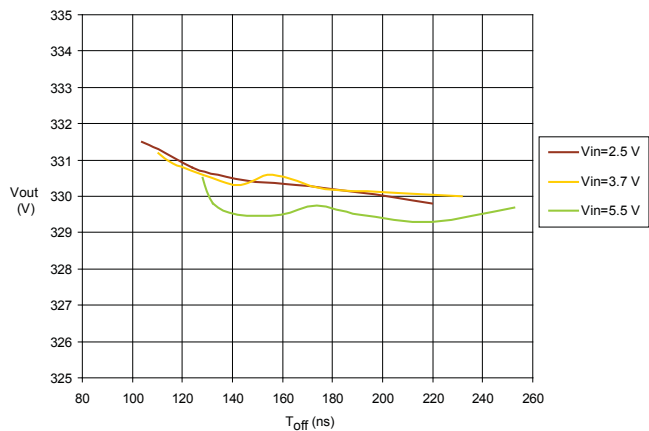
Charge Time vs. Battery Voltage



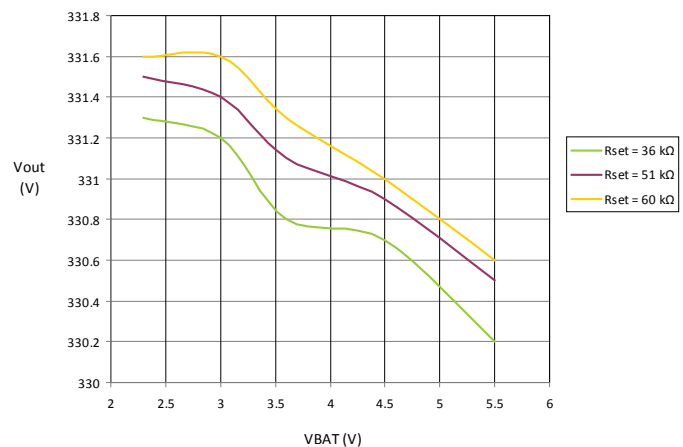
Average Input Current vs. Battery voltage



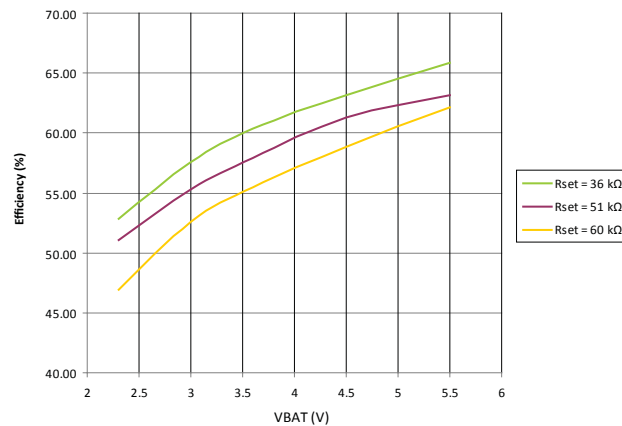
Final Output Voltage vs. Switch Off-Time



Final Output Voltage vs. Battery Voltage



Efficiency vs. Battery Voltage



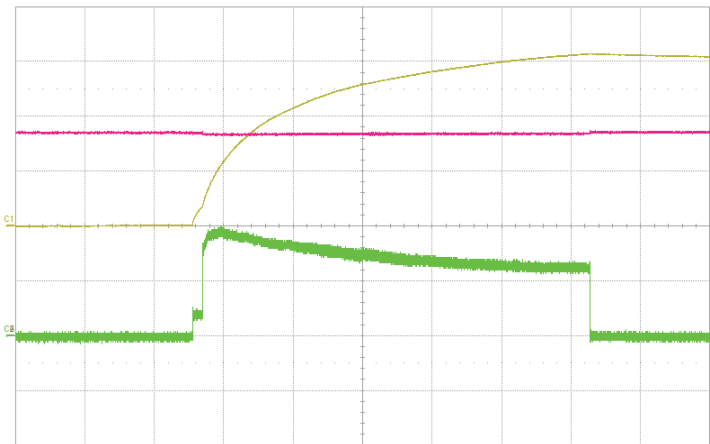


Characteristic Performance

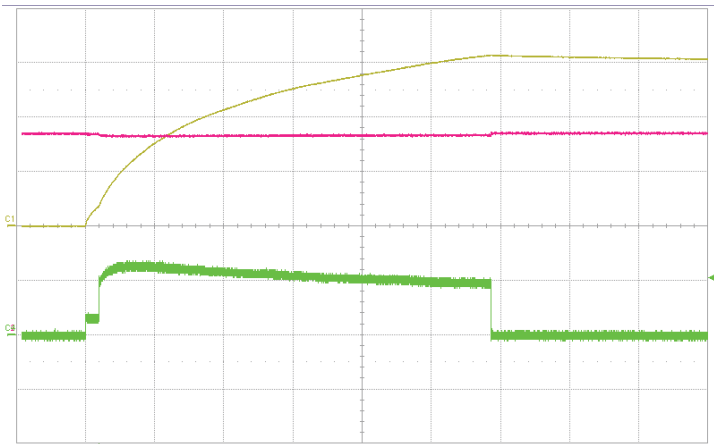
Charging Time at Various  $R_{\text{ISET}}$  Values

Common Parameters		
Symbol	Parameter	Units/Division
C1	$V_{\text{OUT}}$	50 V
C2	$V_{\text{BAT}}$	1 V

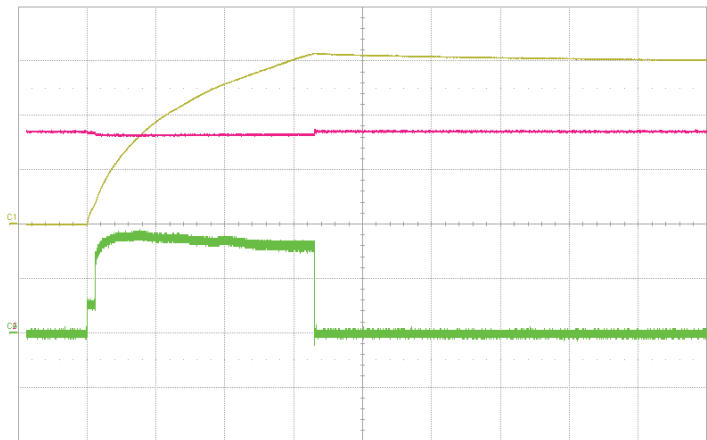
Common Conditions	
Parameter	Value
$V_{\text{BAT}}$	3.6 V
$C_{\text{OUT}}$	21 $\mu\text{F}$
$L_{\text{PRI}}$	8 $\mu\text{H}$



$R_{\text{SET}} = 61\text{ k}\Omega$ , CH4:  $I_{\text{IN}} = 100\text{ mA/div}$ , Time = 1s/div

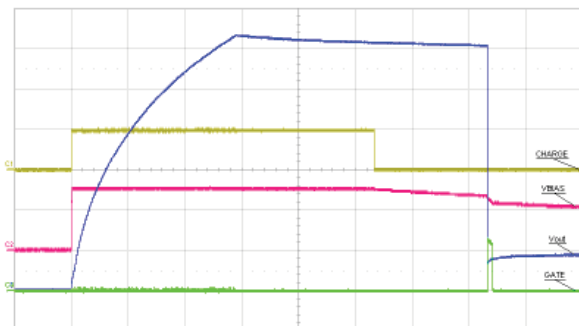


$R_{\text{SET}} = 49\text{ k}\Omega$ , CH4:  $I_{\text{IN}} 200\text{ mA/div}$ , Time = 0.5 s/div



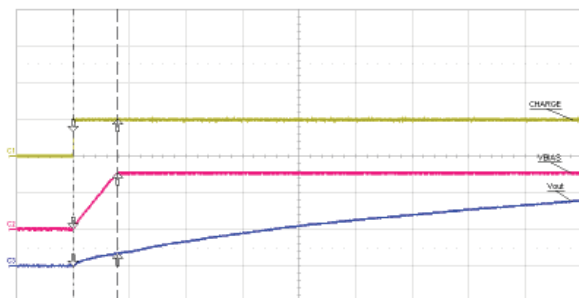
$R_{\text{SET}} = 36\text{ k}\Omega$ , CH4:  $I_{\text{IN}} = 200\text{ mA/div}$ , Time = 0.5 s/div

Complete  $C_{BIAS}$  Charge Cycle versus Time  
See Charge Pump Operation section for timing diagram details

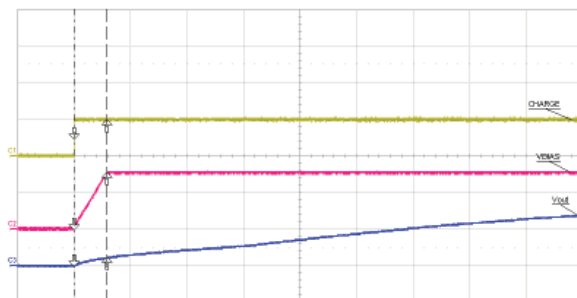


$V_{IN} = 3.6\text{ V}$ ,  $C_{OUT} = 21\text{ }\mu\text{F}$ ,  $C_{BIAS} = 1\text{ }\mu\text{F}$ , Trigger pulse width = 50 ms,  
C1: Charge = 2 V/div, C2:  $V_{BIAS} = 2\text{ V/div}$ , C3:  $V_{OUT} = 50\text{ V/div}$ ,  
C4:  $V_{GATE} = 2\text{ V/div}$ , Time = 500 ms/div

$V_{BIAS}$  Charging versus  $V_{IN}$

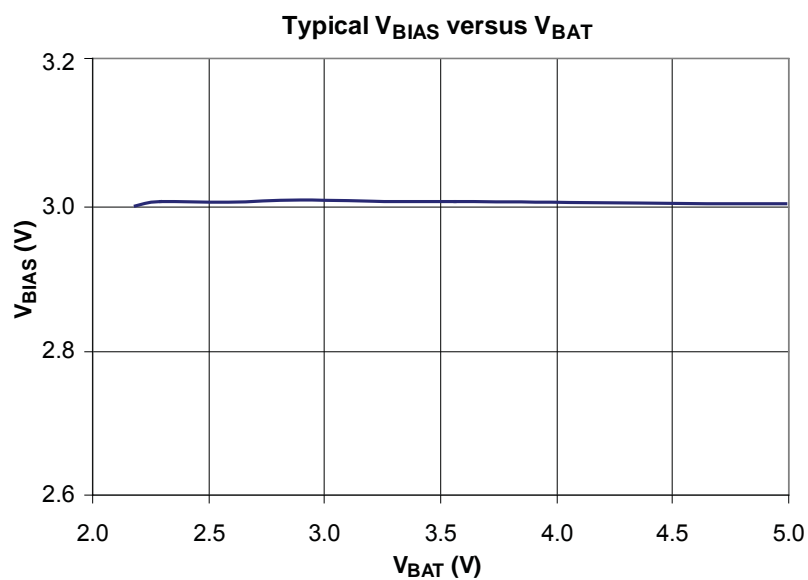


$V_{IN} = 2.3\text{ V}$ .  
 $C_{BIAS} = 1\text{ }\mu\text{F}$ , Charge Time = 8 ms, C1: Charge = 2 V/div,  
C2:  $V_{BIAS} = 2\text{ V/div}$ , C3:  $V_{OUT} = 50\text{ V/div}$ , Time = 10 ms/div



$V_{IN} = 3.6$ .  
 $C_{BIAS} = 1\text{ }\mu\text{F}$ , Charge Time = 6 ms, C1: Charge = 2 V/div,  
C2:  $V_{BIAS} = 2\text{ V/div}$ , C3:  $V_{OUT} = 50\text{ V/div}$ , Time = 10 ms/div

$V_{BIAS}$  charges to required 3 V level in 8 ms, at 2.3 V input, and in 6 ms at 3.6 V input. This is much faster than  $V_{OUT}$  charging.



## Functional Description

### General Operation Overview

The charging operation is started by a low-to-high signal on the CHARGE pin, provided that  $V_{IN}$  is above the  $V_{UVLO}$  level. It is strongly recommended to keep the CHARGE pin at logic low during power-up. After  $V_{IN}$  exceeds the UVLO level, a low-to-high transition on the CHARGE pin is required to start the charging.

The  $\overline{DONE}$  open-drain indicator is pulled low when CHARGE is high and target output voltage is reached. The primary peak current is set by RSET connected across  $I_{SET}$ . When a charging cycle is initiated, the transformer primary side current,  $I_{Primary}$ , ramps up linearly at a rate determined by the combined effect of the battery voltage,  $V_{BAT}$ , and the primary side inductance,  $L_{Primary}$ . When  $I_{Primary}$  reaches the current limit,  $I_{SWLIM}$ , the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor,  $C_{OUT}$ , from the secondary winding. The secondary side current drops linearly as  $C_{OUT}$  charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period,  $t_{OFF(max)}$  (13  $\mu s$ ), whichever occurs first.

The A8738 senses output voltage indirectly on the primary side. This eliminates the requirement for high voltage feedback resistors required for secondary sensing. Flyback converter stops switching when output voltage reaches:

$$V_{OUT} = K \times N \cdot V_d,$$

where:

$K = 31.5$  typically,

$V_d$  is the forward drop of the output diode (around 2 V), and

$N$  is transformer turns ratio.

toggling the CHARGE pin reinitiates charging operation.

### Switch On-Time and Off-Time Control

The A8738 implements an adaptive on-time/off-time control. On-time duration,  $t_{on}$ , is equal to  $t_{on} = I_{SWLIM} \times L_P / V_{BAT}$ . Off-time duration,  $t_{off}$ , depends on the operating conditions during switch off-time. The A8738 applies two charging modes, Fast Charging mode and Timer mode, according to those conditions.

### Timer Mode and Fast Charging Mode

The A8738 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer mode and Fast Charging mode is shown in figure 3.

The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage,  $V_{OUT}$ , is less than approximately 15 to 20 V. Timer mode is a fixed period, 13  $\mu s$ , off-time control. One advantage of having Timer mode is that it limits the initial battery current surge

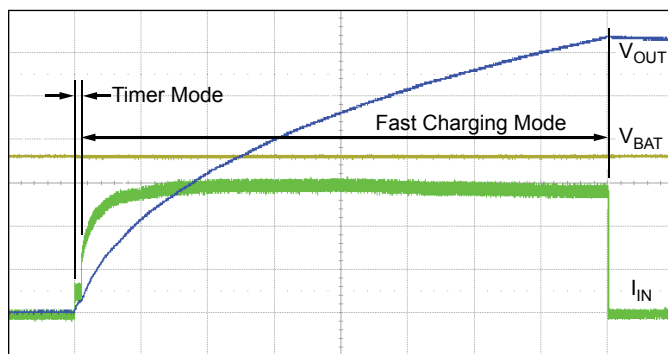


Figure 3. Timer mode and Fast Charging mode:  $t = 200 \text{ ms/div}$ ;  $V_{OUT} = 50 \text{ V/div}$ ;  $V_{BAT} = 1 \text{ V/div}$ ;  $I_{IN} = 100 \text{ mA/div}$ ;  $V_{BAT} = 3.6 \text{ V}$ ;  $C_{OUT} = 20 \mu F / 330 \text{ V}$ ; and  $I_{SWLIM} \approx 0.75 \text{ A}$ .

and thus acts as a “soft-start.” A time-expanded view of a Timer mode interval is shown in figure 4.

As soon as a sufficient voltage has built-up at the output capacitor, the IC enters Fast-Charging mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging mode to start earlier, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 5.

During Fast-Charging mode, when  $V_{OUT}$  is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 6.

## Switch Current Setting

The A8738 features continuously adjustable peak switching current between 0.4 and 0.9 A. This is done by selecting the value of an external resistor,  $R_{SET}$ , connected from the ISET pin to GND, which determines the ISET bias current, and therefore the switching current limit,  $I_{SWlim}$ .

To the first order approximation,  $I_{SWlim}$  is related to ISET and  $R_{SET}$  according to the following equations:

$$I_{SWlim} = I_{SET} \times K = V_{SET} / R_{SET} \times K, \quad (3)$$

where  $K = 28000$  when battery voltage is 3.6 V.

In real applications, the actual switching current limit is affected by input battery voltage, and also the transformer primary inductance,  $L_{Primary}$ . If necessary, the following expressions can be used to determine  $I_{SWlim}$  more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{GND(INT)}), \quad (4)$$

where:

$R_{SET(INT)}$  is the internal resistance of the ISET pin (1 k $\Omega$  typical),

$R_{GND(INT)}$  is the internal resistance of the bonding wire for the GND pin (27 m $\Omega$  typical), and

$K = (K' + V_{IN} \times K'')$ , with  $K' = 24350$  and  $K'' \approx 1040$  at  $T_A = 25^\circ\text{C}$ .

Then,

$$I_{SWlim} = I_{SET} \times K + V_{BAT} / L_{Primary} \times t_D,$$

where  $t_D$  is the delay in SW turn-off (0.1  $\mu\text{s}$  typical).

The chart in figure 7 can be used to determine the relationship between  $R_{SET}$  and  $I_{SWlim}$  at various battery voltages.

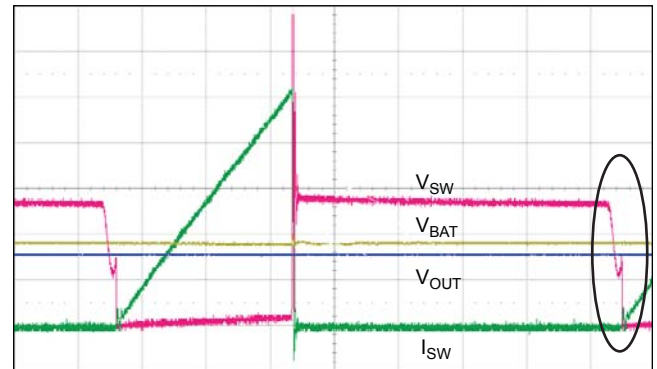


Figure 5. Minimum-voltage switching:  $V_{OUT} \geq 15\text{ V}$ ;  $t = 1\text{ }\mu\text{s/div}$ ;  $V_{BAT} = 3.6\text{ V}$ .

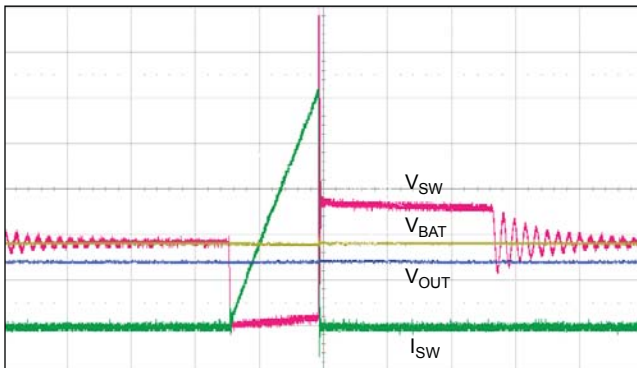


Figure 4. Expanded view of Timer mode:  $V_{OUT} \leq 14\text{ V}$ ;  $t = 2\text{ }\mu\text{s/div}$ ;  $V_{BAT} = 3.6\text{ V}$ .

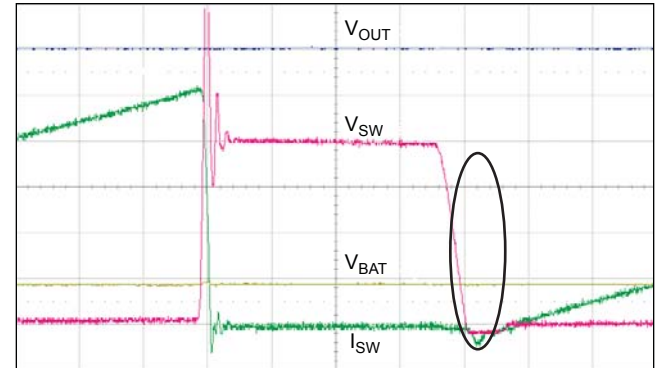


Figure 6. True zero-voltage switching (ZVS):  $V_{OUT} = 120\text{ V}$ ;  $t = 0.2\text{ }\mu\text{s/div}$ ;  $V_{BAT} = 3.6\text{ V}$ .

### Smart Current Limit (Optional)

With the help of some simple external logic, charging current can be varied according to the battery voltage. For example, let's say ISET current is normally 33  $\mu\text{A}$  (for  $I_{\text{LIM}} = 0.9 \text{ A}$ ). When the battery voltage drops below 2.5 V, a BL (battery-low) signal from external controller goes high. A resistor connecting from BL to ISET pin then injects 15  $\mu\text{A}$  into RSET. This effectively reduces ISET current to 18  $\mu\text{A}$  (for  $I_{\text{LIM}} = 0.5 \text{ A}$ ) (see figure 8).

### Charge Pump Operation

The A8738 integrates a regulated 2 $\times$  charge pump to regulate gate voltage across a wide range of supply voltages. It can regulate output voltage to 3 V over the entire range of  $V_{\text{IN}}$ . The charge pump is enabled as long as the CHARGE pin is high. Figure 9 shows a timing diagram for output capacitor charging and  $V_{\text{BIAS}}$ .

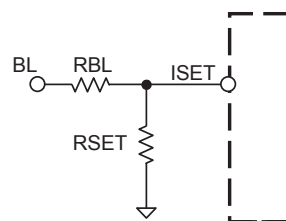


Figure 8. Smart current limiting option

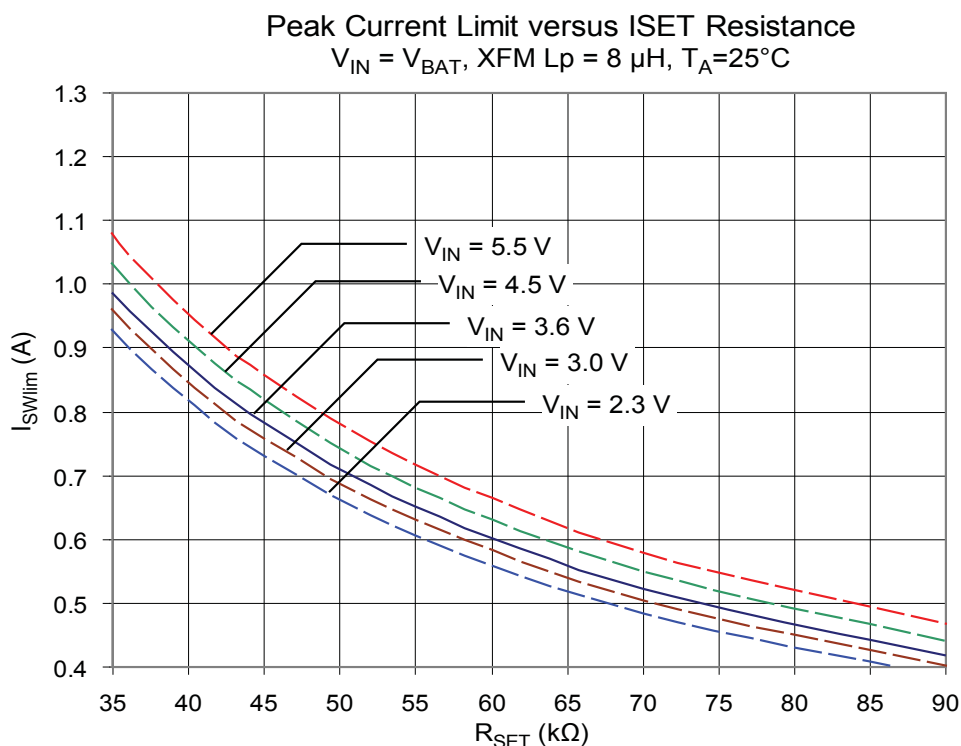


Figure 7. Determination of value for current limiting

In figure 9, at time A, the output capacitor is completely discharged and the CHARGE pin is pulled high. The flyback converter charges the output capacitor to the target output level at time C, and the DONE pin goes low, indicating Charge Complete. The charge pump output voltage reaches 3 V during time interval A–B. The charge pump stops regulating voltage after time D, as the CHARGE pin is pulled low.

Voltage across CBIAS (C2) may drop after this time due to leakage. The voltage drop is:

$$\Delta V_{\text{BIAS}} = 0.2 \mu\text{A} \times \text{time} / C_{\text{BIAS}} ,$$

where  $0.2 \mu\text{A}$  is the internal leakage current via the VBIAS pin.

To minimize VBIAS voltage droop, apply the TRIGGER pulse within a few milliseconds ( $<100 \text{ ms}$ ) after the CHARGE pin is pulled low.

A short pre-flash trigger pulse is applied at time E. The typical IGBT gate charge is  $40 \text{ nC}$ . This charge is supplied by CBIAS, and VBIAS drops by  $40 \text{ nC} / C_{\text{BIAS}}$ . The main trigger pulse is applied at time G. Voltage VBIAS drops further in this period. IGBT gate voltage drops due to charge transfer to the IGBT gate.

The IGBT trigger pulse can be applied at any time, as shown at time instance I.

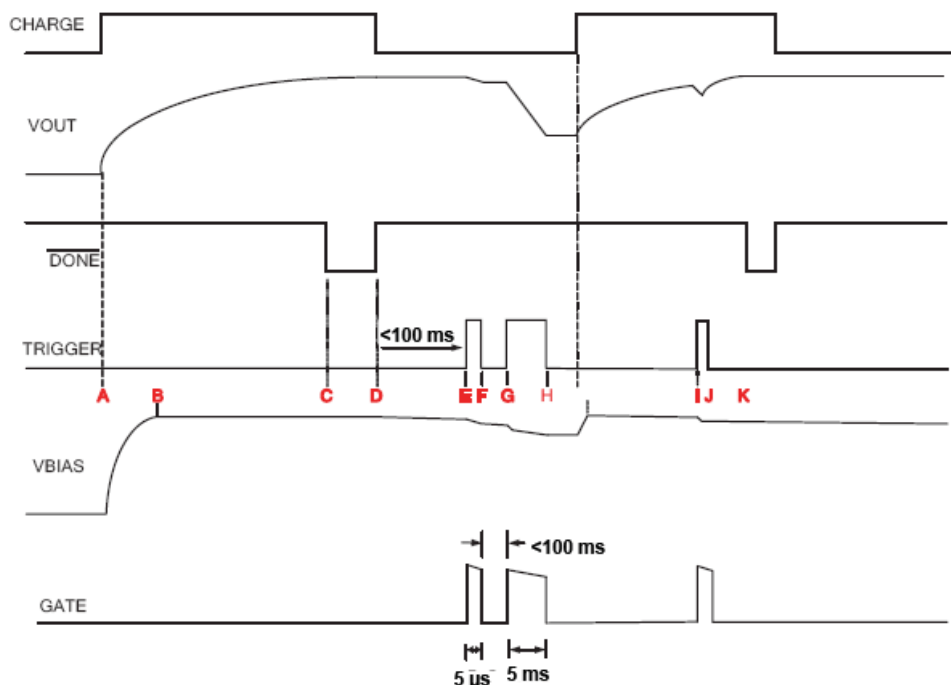


Figure 9. Timing diagram for output capacitor charging and charge pump output (Not to Scale)

## Applications Information

## Transformer Design

1. The transformer turns ratio,  $N$ , determines the output voltage:

$$N = N_S / N_P$$

$$V_{OUT} = 31.5 \times N - V_d ,$$

where 31.5 is the typical value of  $V_{OUTTRIP}$ , and  $V_d$  is the forward drop of the output diode.

2. The primary inductance,  $L_P$ , determines the on-time of the switch:

$$t_{on} = (-L_P / R) \times \ln(1 - I_{SWlim} \times R / V_{IN}) ,$$

where  $R$  is the total resistance in the primary current path (including  $R_{SWDS(on)}$  and the DC resistance of the transformer).

If  $V_{IN}$  is much larger than  $I_{SWlim} \times R$ , then  $t_{on}$  can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{IN} .$$

3. The secondary inductance,  $L_S$ , determines the off-time of the switch. Given:

$$L_S / L_P = N \times N , \text{ then}$$

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} \\ = (I_{SWlim} \times L_P \times N) / V_{OUT} .$$

The minimum pulse width for  $t_{off}$  determines what is the minimum  $L_{Primary}$  required for the transformer. For example, if  $I_{SWlim} = 0.7 \text{ A}$ ,  $N = 10$ , and  $V_{OUT} = 315 \text{ V}$ , then  $L_{Primary}$  must be at least  $6.3 \mu\text{H}$  in order to keep  $t_{off}$  at 140 ns or longer. These relationships are illustrated in figure 10.

In general, choosing a transformer with a larger  $L_{Primary}$  results in higher efficiency (because a larger  $L_{Primary}$  corresponds to a lower switch frequency and hence lower switching loss). But transformers with a larger  $L_{Primary}$  also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

## Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the absolute maximum specification on the SW pin (refer to the Absolute Maximum Ratings table). An achievable minimum leakage inductance for this application, however, is

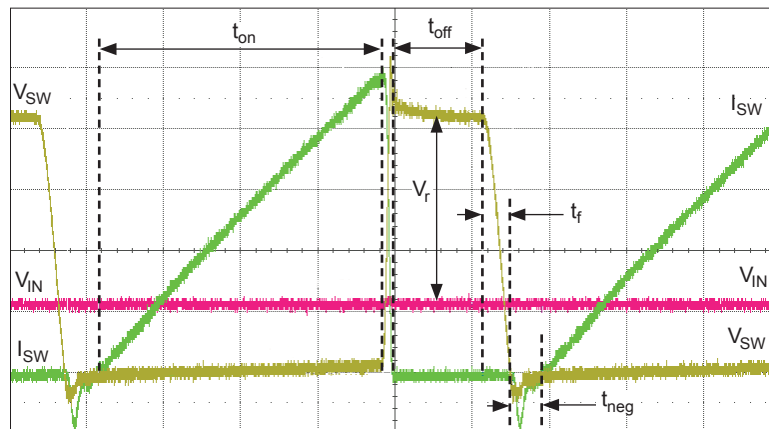


Figure 10. Transformer Selection Relationships



usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by  $N^2$  when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

### Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor,  $C_{IN}$ . During initial timer mode the device operates with 13  $\mu$ s off time. Resonant period caused by input filter inductor and capacitor should be at least 2 times greater or smaller than the 13  $\mu$ s timer period, to reduce input ripple current during this period. The typical input LC filter is shown in figure 11.

The resonant period is given by:

$$T_{res} = 2\pi (L \times C_{IN})^{1/2}.$$

Effect of input filter components is shown in figures 12, 13, and 14. It is recommended to use at least 4.7  $\mu$ F / 6.3 V to decouple the battery input,  $V_{BAT}$ , at the primary of the transformer. Decouple VIN pin using 0.1  $\mu$ F / 6.3 V bypass capacitor.

### Output Diode Selection

Choose the rectifying diode(s), D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diode,  $V_{DPeak}$ , occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{DPeak} = V_{OUT} + N \times V_{BAT}.$$

The peak current of the rectifying diode,  $I_{DPeak}$ , is calculated as:

$$I_{DPeak} = I_{Primary\_Peak} / N.$$

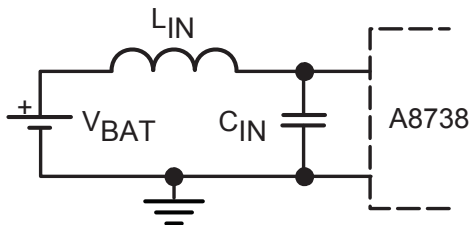


Figure 11. Typical input section with input inductance (inductance,  $L_{IN}$ , may be an input filter inductor or inductance due to long wires in test setup)

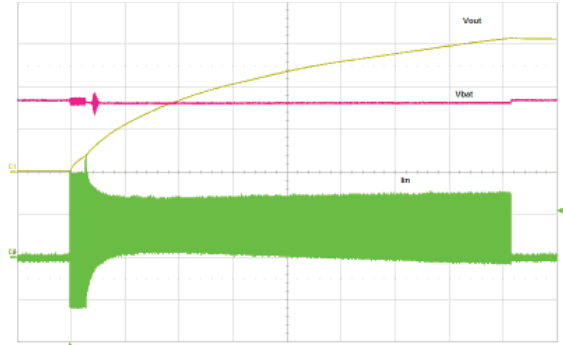


Figure 12. Input current waveforms with Li+ battery connected by 5-in. wire and decoupled by 4.7  $\mu$ F capacitor. CH1:  $V_{OUT} = 100$  V/div, CH2:  $V_{BAT} = 2$  V/div, CH4:  $I_{IN(av)} = 500$  mA/div, Time = 200 ms/div,  $C_{OUT} = 21$   $\mu$ F,  $R_{ISET} = 36$  k $\Omega$

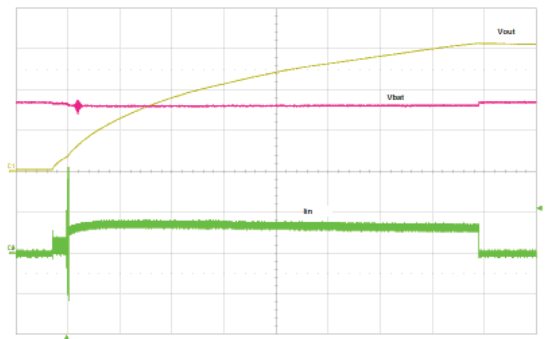


Figure 13. Input current waveforms with Li+ battery connected through 10  $\mu$ H inductor and 4.7  $\mu$ F capacitor. CH1:  $V_{OUT} = 100$  V/div, CH2:  $V_{BAT} = 2$  V/div, CH4:  $I_{IN(av)} = 500$  mA/div, Time = 200 ms/div,  $C_{OUT} = 21$   $\mu$ F,  $R_{ISET} = 36$  k $\Omega$

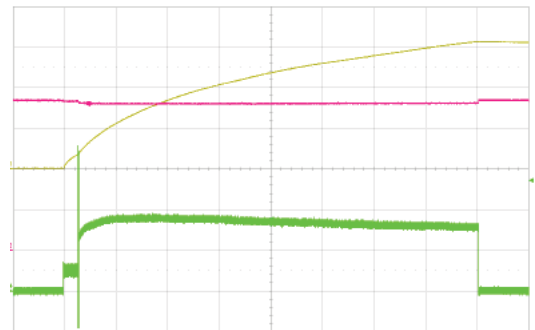


Figure 14. Input current waveforms with Li+ battery connected through 10  $\mu$ H inductor and 10  $\mu$ F capacitor. CH1:  $V_{OUT} = 100$  V/div, CH2:  $V_{BAT} = 2$  V/div, CH4:  $I_{IN(av)} = 200$  mA/div, Time = 200 ms/div,  $C_{OUT} = 21$   $\mu$ F,  $R_{ISET} = 36$  k $\Omega$

**Bias Capacitor Selection**

Select bias capacitor sufficiently large to hold the voltage during Charging done and trigger applied. Also this capacitor provides charge to IGBT gate capacitance during every flash period. It is recommended to use a 1  $\mu\text{F}$  / 6.3 V capacitor for this application. If the voltage droop is more than requirement, increase capacitor accordingly. The MLCC (multi-layer ceramic capacitor) specify capacitance at zero-bias voltage. When a DC bias is applied, the capacitance may be reduced by as much as 70%. For example, when a ceramic capacitor rated as 0.47  $\mu\text{F}$  / 6.3 V biased at 5 VDC could have capacitance equal to 0.15  $\mu\text{F}$ . A larger package (such as a 0603) is preferred over a smaller one (such as a 0402), because the capacitance derating is worse for capacitors with smaller package and lower operating voltage. See the table Recommended Components for more information.

**Layout Guidelines**

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop

(transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin. It is important that the  $\overline{\text{DONE}}$  signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

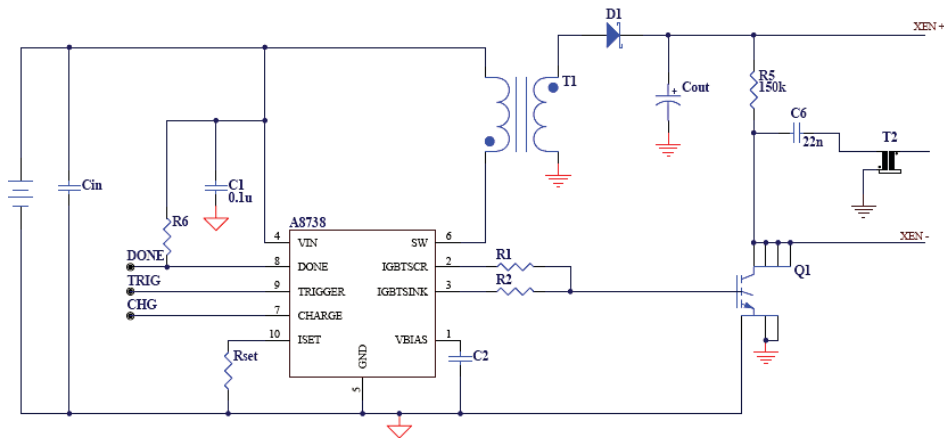
Avoid ground plane underneath transformer secondary and diode to minimize parasitic capacitance.

For low threshold logic (<1.2 V) add 1 nF capacitors across the CHARGE and TRIGGER pins to GND to avoid malfunction due to noise.

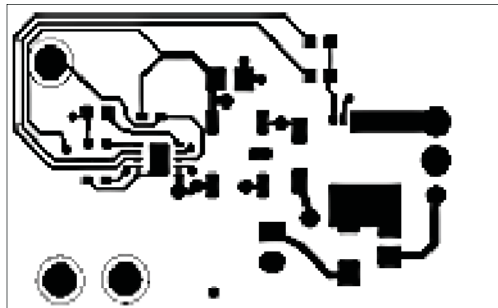
Connect EJ package PAD, or CG package GND pins to ground pad for better thermal performance. Use ground planes on both the top and bottom layers below the IC, and connect through multiple thermal vias. Refer to the figures on the next page for recommended layout.

## Recommended layout:

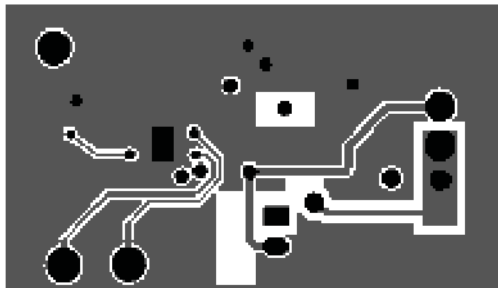
Schematic



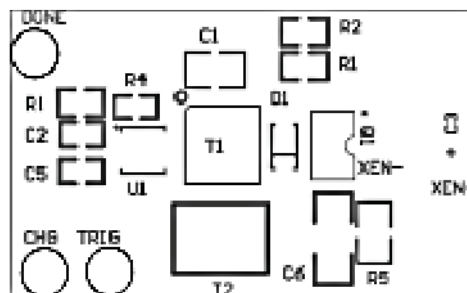
Top side



Bottom side



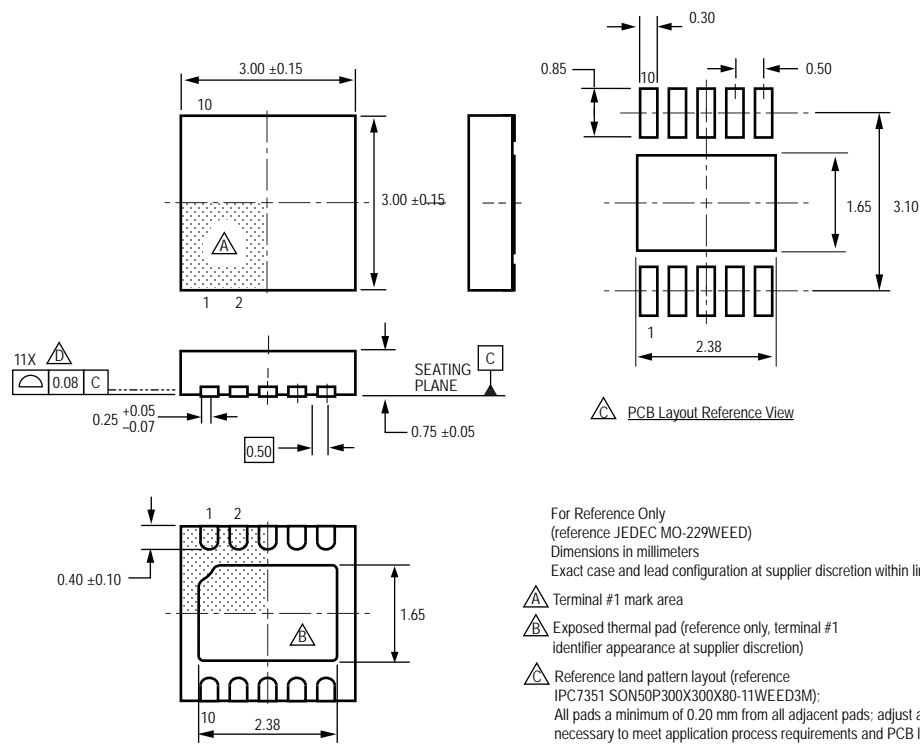
Top components



**Recommended Components**

Component	Rating	Part Number	Source
C1	0.1 $\mu$ F, 6.3 V, X5R ceramic capacitor		
C2, Bias Capacitor	1 $\mu$ F, $\pm 10\%$ , 6.3 V, X7R ceramic capacitor (0603)	GRM188R60J105	Murata
C <sub>IN</sub> , Input Capacitor	4.7 $\mu$ F, $\pm 10\%$ , 6.3 V, X5R ceramic capacitor (0805)	JMK212BJ475K	Taiyo Yuden
C <sub>OUT</sub> , Photoflash Capacitor	80 $\mu$ F / 330 V	EPH-331E--800A030S	Chemi-Con
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
Rset	36 k $\Omega$ , 1%		
R1	23 $\Omega$ , 0603		
R2	30 $\Omega$ 0603		
T1, Transformer	L <sub>primary</sub> = 8 $\mu$ H, N = 9.9, 5 mm x 5 mm x 2.2 mm	C5-KT2.2L	Mitsumi Electric Co.
	L <sub>primary</sub> = 6.6 $\mu$ H, N = 10.2, 5 mm x 5 mm x 2 mm	T-19-243	Tokyo Coil Electric

**Package EJ 10-Contact TDFN  
with Exposed Thermal Pad**



For Reference Only  
(reference JEDEC MO-229WEED)  
Dimensions in millimeters  
Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- △ Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

**Revision History**

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	A8738 only, miscellaneous format changes

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