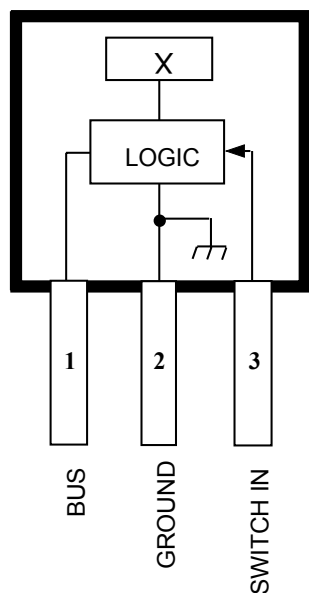


DISCONTINUED PRODUCT
Shown for Reference Only

MULTIPLEXED TWO-WIRE HALL-EFFECT SENSOR ICs



Dwg. PH-005

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25^\circ\text{C}$

| | |
|---|--|
| Supply Voltage, V_{BUS} | 24 V |
| Magnetic Flux Density, B | Unlimited |
| Operating Temperature Range, T_A | -20°C to $+85^\circ\text{C}$ |
| Storage Temperature Range, T_S | -55°C to $+150^\circ\text{C}$ |
| Package Power Dissipation, P_D | 750 mW |

The UGN3055U Hall-effect sensor IC is a digital magnetic sensing IC capable of communicating over a two-wire power/signal bus. Using a sequential addressing scheme, the device responds to a signal on the bus and returns the diagnostic status of the IC, as well as the status of each monitored external magnetic field. As many as 30 devices can function on the same two-wire bus. This IC is ideal for multiple device applications where minimizing the wiring harness size is desirable or essential.

The device consists of high-resolution bipolar Hall-effect switching circuitry, the output of which drives high-density CMOS logic stages. These logic stages decode the address pulse and enable a response at the appropriate address. The combination of magnetic-field or switch-status sensing, low-noise amplification of the Hall-transducer output, and high-density decoding and control logic is made possible by the development of a new device BiMOS fabrication technology.

This unique magnetic sensing IC operates within specifications between -20°C and $+85^\circ\text{C}$. Alternate magnetic and temperature specifications are available upon request. It is supplied in a 60 mil (1.54 mm) thick, three-pin plastic SIP. Each package is clearly marked with a two-digit decimal device address (xx).

FEATURES

- Complete Multiplexed Hall-Effect IC with Simple Sequential Addressing Protocol
- Allows Power and Communication Over a Two-Wire Bus (Supply/Signal and Ground)
- Up to 30 Hall-Effect Devices Can Share a Bus
- Diagnostic Capabilities
- Magnetic-Field or Switch-Status Sensing
- Low Power of BiMOS Technology Favors Battery-Powered and Mobile Applications
- Ideal for Automotive, Consumer, and Industrial Applications

Always order by complete part number: **UGN3055U** .

3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

OPERATIONAL CHARACTERISTIC over operating temperature range.

| Electrical Characteristics | | Symbol | Limits | | | |
|----------------------------|---|------------|-----------|------|-----------|---------------|
| | | | Min. | Typ. | Max. | Units |
| Power Supply Voltage | | V_{BUS} | — | — | 15 | V |
| Signal Current | | I_S | 12 | 15 | 20 | mA |
| Quiescent Current | $V_{BUS} = 6\text{ V}$ | I_{QH} | — | — | 2.5 | mA |
| | $V_{BUS} = 9\text{ V}$ | I_{QL} | — | — | 2.5 | mA |
| | $I_{QH} - I_{QL}$ | I_Q | — | — | 300 | μA |
| Address Range | | Addr | 1 | — | 30 | — |
| Clock Thresholds | LOW to HIGH | V_{CLH} | — | — | 8.5 | V |
| | HIGH to LOW | V_{CHL} | 6.5 | — | — | V |
| | Hysteresis | V_{CHYS} | — | 0.8 | — | V |
| Clock Period | | t_{CLK} | 0.1 | 1.0 | — | ms |
| Address LOW Voltage | | V_L | V_{RST} | 6 | V_{CHL} | V |
| Address HIGH Voltage | | V_H | V_{CLH} | 9 | V_{BUS} | V |
| Power-On Reset Voltage | | V_{RST} | 2.5 | 3.5 | 5.5 | V |
| Settling Time | $V_{BUS} = 9\text{ V}$ | t_h | 100 | — | — | μs |
| | $V_{BUS} = 6\text{ V}$ | t_l | 100 | — | — | μs |
| Propagation Delay | LOW to HIGH | t_{plh} | 10 | — | — | μs |
| | HIGH to LOW | t_{phi} | — | — | 10 | μs |
| Pin 3 Input Resistance | No Magnetic Field ($V_{OUT} = \text{HIGH}$) | R_{OUTH} | 40 | — | 75 | $k\Omega$ |
| | Mag. Field Present ($V_{OUT} = \text{LOW}$) | R_{OUTL} | — | — | 50 | Ω |

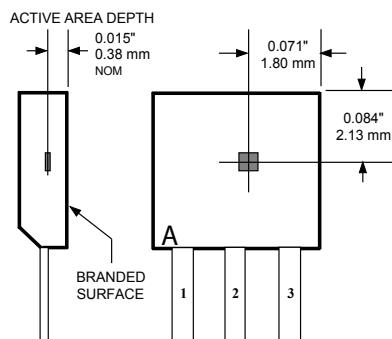
Magnetic Characteristics

| | | | | | | |
|----------------------------------|----------|-----------|-----|-----|-----|---|
| Magnetic Thresholds | *Turn-On | B_{OP} | 50 | 150 | 300 | G |
| | Turn-Off | B_{RP} | -25 | 100 | 300 | G |
| Hysteresis ($B_{OP} - B_{RP}$) | | B_{HYS} | 0 | 50 | 75 | G |

*Alternate magnetic switch point specifications are available on request. Please contact the factory.

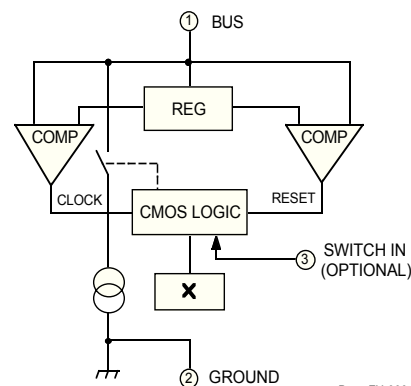
3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

ELEMENT LOCATION ($\pm 0.005"$ [0.13 mm] die placement)



Dwg. MH-002A

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-009

DEFINITION OF TERMS

Device Address

Each bus device has a factory-specified predefined address. At present, allowable device addresses are integers from 1 to 30.

LOW-to-HIGH Clock Threshold (V_{CLH})

Minimum voltage required during the positive-going transition to increment the bus address and trigger a diagnostic response from the bus devices. This is also the maximum threshold of the on-chip comparator, which monitors the supply voltage, V_{BUS} .

HIGH-to-LOW Threshold (V_{HL})

Maximum voltage required during the negative-going transition to trigger a *signal* current response from the bus devices. This is also the maximum threshold of the on-chip comparator, which monitors the supply voltage, V_{BUS} .

Bus HIGH Voltage (V_H)

Bus HIGH voltage required for addressing. Voltage should be greater than V_{CLH} .

Address LOW Voltage (V_L)

Bus LOW Voltage required for addressing. Voltage should be greater than V_{RST} and less than V_{CHL} .

Bus Reset Voltage (V_{RST})

Voltage level required to reset individual devices.

Device Quiescent Current Drain (I_Q)

The current drain of bus devices when active but not addressed. I_{QH} is the maximum quiescent current drain when the device is not addressed and is at V_H . I_{QL} is the maximum quiescent current drain when the device is not addressed and is at V_L .

Diagnostic Phase

Period on the bus when the address voltage is at V_H . During this period, a correctly addressed device responds by increasing its current drain on the bus. This response from the device is called the **diagnostic response** and the bus current *increase* is called the **diagnostic current**.

Signal Phase

Period on the bus when the address voltage is at V_L . During this period, a correctly addressed device that detects a magnetic field greater than magnetic Operate Point, B_{OP} , responds by maintaining a current drain of I_S on the bus. This response from the device is called the **signal response** and the bus current *increase* is called the **signal current**.

Device Address Response Current (I_S)

Current returned by the bus devices during the *diagnostic* and the *signal* responses of the bus devices. This is accomplished by enabling the constant current source (CCS).

Magnetic Operate Point (B_{OP})

Minimum magnetic field required to switch ON the Hall amplifier and switching circuitry of the addressed device. This circuitry is only active when the device is addressed.

Magnetic Release Point (B_{RP})

Magnetic field required to switch OFF the Hall amplifier and switching circuitry after the output has switched ON. This is due to magnetic memory in the switching circuitry. However, when a device is deactivated by changing the current bus address, all magnetic memory is lost.

Magnetic Hysteresis (B_{HYS})

Difference between the B_{OP} and B_{RP} magnetic field thresholds.

3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

ADDRESSING PROTOCOL

The device may be addressed by modulating the supply voltage as shown in Figure 1. A preferred addressing protocol is as follows: the bus supply voltage is brought down to 0V so that all devices on the bus may be reset. The voltage is then raised to the address LOW voltage (V_L) and the bus quiescent current is measured. The bus is then toggled between V_L and V_H (address HIGH voltage), with each positive transition representing an increment in the bus address. After each voltage transition, the bus current is monitored to check for diagnostic and signal responses from sensor ICs.

Device Addressing

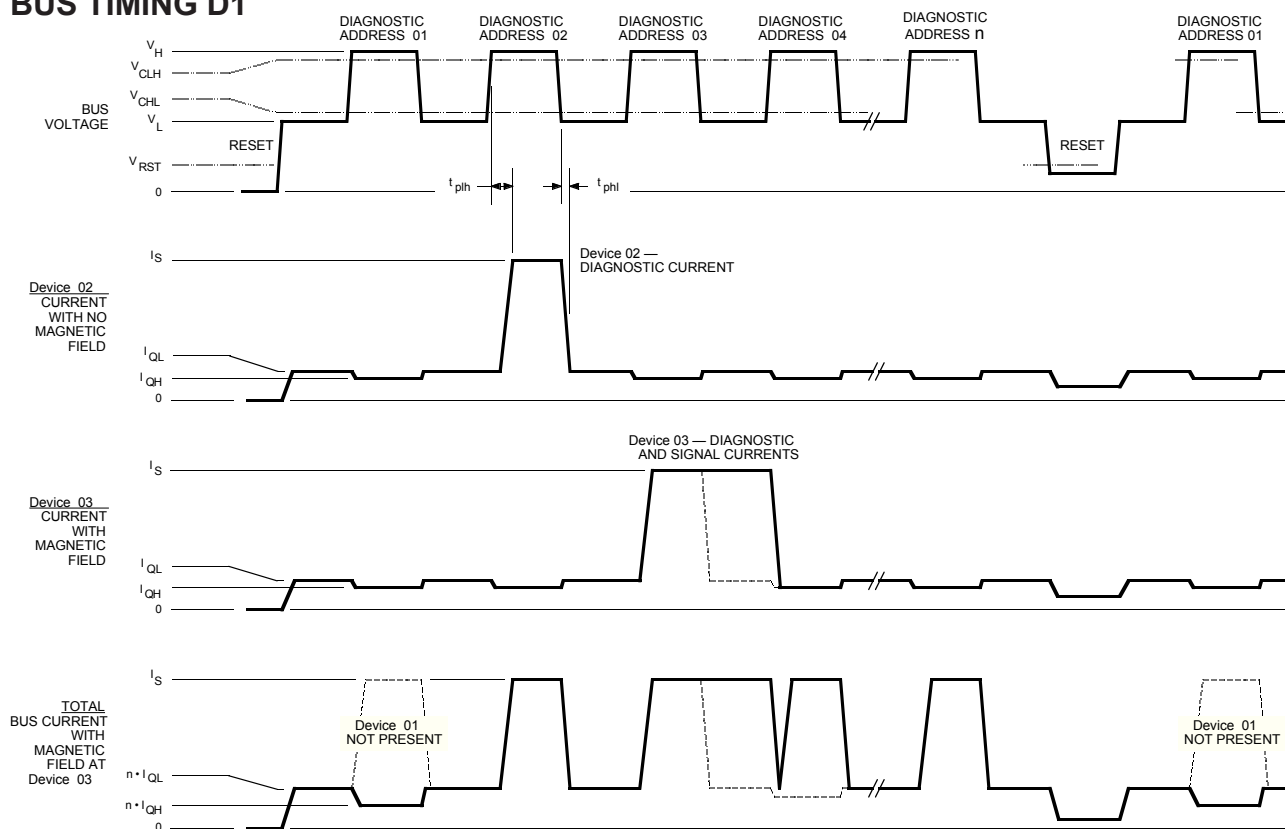
When a device detects a bus address equal to its factory programmed address, it re-

sponds with an increase in its supply current drain (called I_S during the HIGH portion of the address cycle). This response may be used as an indication that the device is alive and well on the bus and is also called the *diagnostic* response. If the device detects an ambient magnetic field, it also responds with I_S during the low portion of the address cycle. This response from the device is called the *signal* response. When the next positive transition is detected, the device becomes disabled, and its contribution to the bus signal current returns to I_Q .

Bus Current

Figure 1 displays the above described addressing protocol. The top trace represents the bus voltage transitions as controlled by the bus driver (see applications note for an optimal bus driver schematic). The second trace represents the bus current contribution of device (address 02). The *diagnostic* response from the device indicates that it detected its address on the bus; however, no *signal* response current is returned, which indicates that sufficient magnetic field is not detected at the chip surface. The third trace represents the current drain of device 03 when a magnetic field is detected. Note both the *diagnostic* and *signal* response from the device. The last trace represents

**FIGURE 1
BUS TIMING D1**



Dwg. WH-005

3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

the overall bus current drain. When no devices are addressed, the net bus current drain is the sum of quiescent currents of all devices on the bus (for 'n' devices, the bus quiescent current drain is $n \cdot I_Q$).

Bus Issues

At present, a maximum of 30 active devices can coexist on the same bus, each with a different address. Address 0 is reserved for bus current calibration in software. This feature allows for fail-safe detection of signal current and eliminates detection problems caused by low signal current (I_S), the operation of devices at various ambient temperatures, lot-to-lot variation of quiescent current, and the addition and replacement of devices to the bus while in the field. Address 31 is designed to be inactive to allow for further address expansion of the bus (to 62 maximum addresses). In order to repeat the address cycle, the bus must be reset as shown in Figure 1 by bringing the supply voltage to below V_{RST} . Devices have been designed not to 'wrap-around'.

Magnetic Sensing

The device IC has been designed to respond to an external magnetic field whose magnetic strength is greater than B_{OP} . It accomplishes this by amplifying the output of an on-chip Hall transducer and feeding it into a threshold detector. In order that bus current is kept to a minimum, the transducer and amplification circuitry is kept powered down until the device is addressed. Hence, the magnetic status is evaluated only when the device is addressed.

External Switch Sensing

The third pin of the IC (pin 3) may be used to detect the status of an external switch when magnetic field sensing is not desired (and in the absence of a magnetic field). The allowable states for the switch are 'open' and 'closed' (shorted to device ground).

APPLICATIONS NOTES

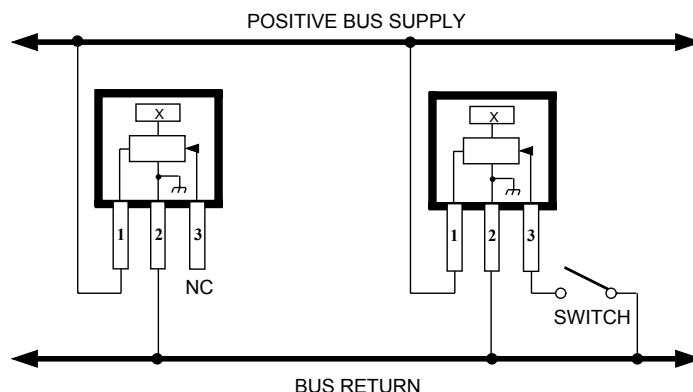
Magnetic Actuation

The left side of Figure 2 shows the wiring of the UGN3055U when used as a magnetic threshold detector. Pin 1 of the device is wired to the positive terminal of the bus, pin 2 is connected to the bus negative terminal, and *pin 3 has no connection*.

Mechanical Actuation

The right side of Figure 2 shows the wiring of the UGN3055U when used to detect the status of a mechanical switch. In this case, pin 3 is connected to the positive terminal of the switch. The negative side of the switch is connected to the negative terminal of the bus. When the mechanical switch is closed (shorted to ground) and the correct bus address is detected by the IC, the device responds with a signal current. If the switch is open, only a diagnostic current is returned.

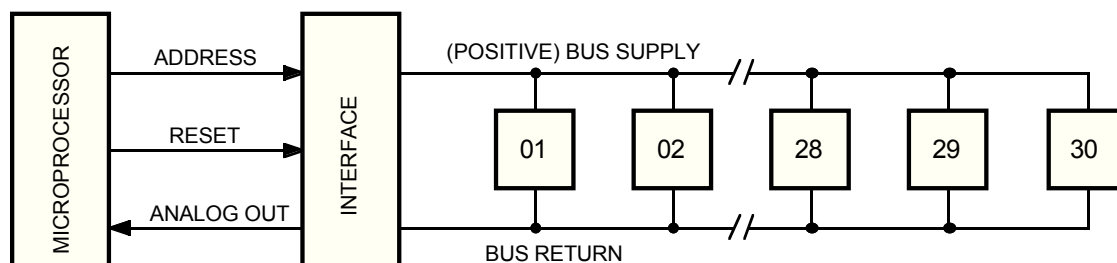
**FIGURE 2
DEVICE CONNECTIONS**



Dwg. EH-004

3055 MULTIPLEXED TWO-WIRE HALL EFFECT DEVICE IC

**FIGURE 3
BUS INTERCONNECTION**



Dwg. EH-005

Bus Configuration

A maximum of 30 devices may be connected across the same two wire bus as shown in Figure 3. It is recommended that the devices use a dedicated digital ground wire to minimize the effects of changing ground potential (as in the case of chassis ground in the automotive industry).

The bus was not designed to require two-wire twisted-pair wiring to the devices; however, in areas of extreme EMI (electro-magnetic interference), it may be advisable to install a small bypass capacitor (0.01 μ F for example) between the supply and ground terminals of each device instead of using the more expensive wiring.

Bus Driver

It is recommended that the bus be controlled by microprocessor-based hardware for the following reasons:

- Device address information may be stored in ROM in the form of a look up table.
- Bus faults can be pinpointed by the microprocessor by comparing the diagnostic response to the expected response in the ROM look up table.
- The microprocessor, along with an A/D converter, can also be used to self calibrate the quiescent currents in the bus and hence be able to easily detect a signal response.

- The microprocessor can also be used to filter out random line noise by digitally filtering the bus responses.
- The microprocessor can easily keep track of the signal responses, initiate the appropriate action; e.g., light a lamp, sound an alarm, and also pinpoint the location of the signal.

Optimally, the microprocessor is used to control bus-driving circuitry that will accept TTL level inputs to drive the bus and will return an analog voltage representation of the bus current.

Interface Schematic

The bus driver is easily designed using a few operational amplifiers, resistors, and transistors. Figure 4 shows a schematic of a recommended bus driver circuit that is capable of providing 6 V to 9 V transitions, resetting the bus, and providing an analog measurement of the current for use by the A/D input of the microprocessor.

In Figure 4, the Address pin provides a TTL-compatible input that is used to control the Bus supply. A HIGH (5 V) input switches Q1 ON and sets the bus voltage to 6 V through the resistor divider R4, R5, and the Zener Z1. A LOW input switches OFF Q2 and sets the bus voltage to 9 V. This voltage is fed into the positive input of the operational amplifier OP1 and is buffered and made available at Bus Supply (or device supply). Bus reset control is also available in the form of a TTL-compatible input. When this input, which is marked Reset, is HIGH, Q2 is switched ON and the positive input of the op amp is set to the saturation voltage of the transistor (approximately 0 V). This resets the bus.

A linear reading of the bus current is made possible by amplifying the voltage generated across R6 (which is $I_{BUS} * R6$). The amplifier, OP2, is a standard differential amplifier of gain $R9/R7$ (provided that $R7 = R8$, $R9 = R10$). The gain of the total transimpedance amplifier is given by:

$$V_{OUT} = I_{BUS} * R6 * R9/R7$$

This voltage is available at the terminal marked Analog Out.

3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

Bus Control Software

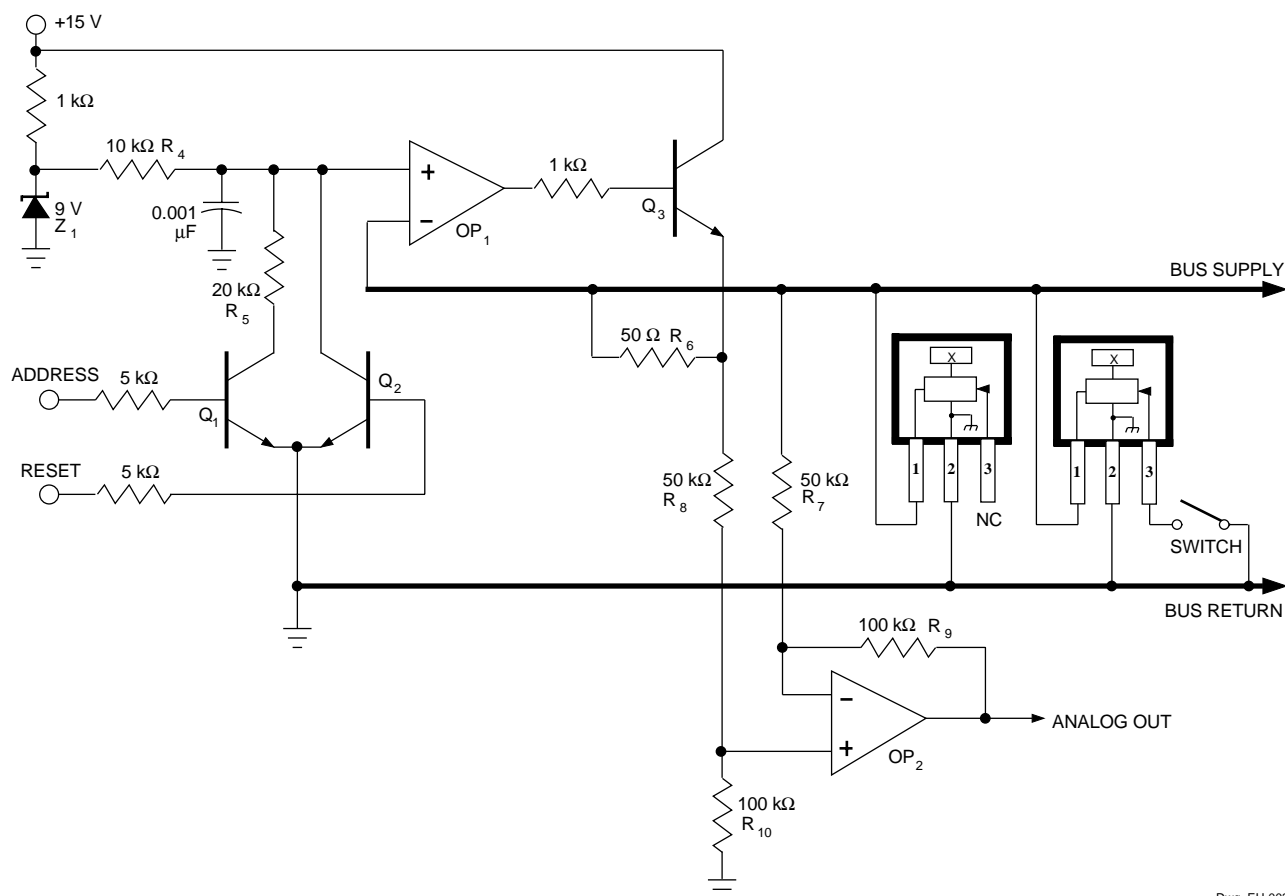
The processing of the bus current (available at Analog Out) is best done by feeding it into the A/D input of a microprocessor. If the flexibility provided by a microprocessor is not desired, this signal could be fed into threshold detection circuitry; e.g., comparator, and the output used to drive a display.

Related References

1. G. AVERY, "Two Terminal Hall. Sensor," *ASSIGNEE: Sprague Electric Company, North Adams, MA, United States. Patent number 4,374,333; Feb. 1983.*

2. T. WROBLEWSKI and F. MEISTERFIELD, "Switch Status Monitoring System, Single Wire Bus, Smart Sensor Arrangement There Of," *ASSIGNEE: Chrysler Motor Corporation, Highland Park, MI, United States. Patent number 4,677,308; June 1987.*

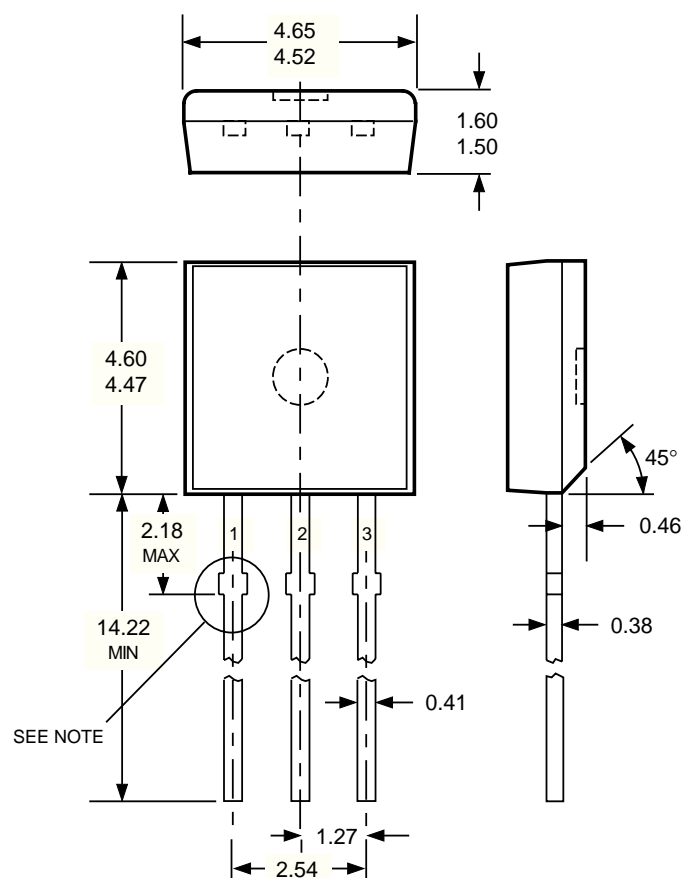
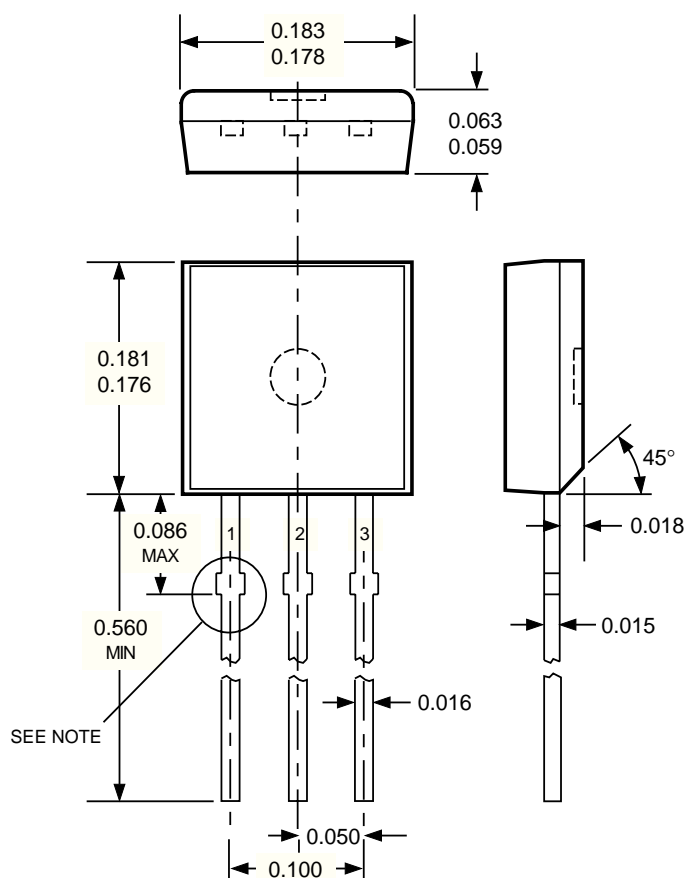
FIGURE 4
BUS INTERFACE SCHEMATIC



3055 MULTIPLEXED TWO-WIRE HALL EFFECT SENSOR IC

**Dimensions in Inches
(controlling dimensions)**

**Dimensions in Millimeters
(for reference only)**



- NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.
6. Minimum lead length was 0.500" (12.70 mm). If existing product to the original specifications is not acceptable, contact sales office before ordering.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.