PRODUCT DESCRIPTION

Technical Paper
STP 98-9

A NEW, LOW-COST DUAL H-BRIDGE MOTOR-DRIVER IC

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ABSTRACT

A new dual H-bridge motor driver IC has been developed to address the universal need to reduce the cost of driving a bipolar stepper motor. This paper will present this new dual H-bridge motor driver, which includes several unique circuit design features. These features, including a new bipolar power output structure, will be explained in detail. This paper will also discuss the decisions behind the various design and system trade-offs that were necessary to minimize cost.

INTRODUCTION

It is well known that driving a stepper motor in a bipolar mode (i.e., the motor is stepped by reversing current in a motor winding) is more efficient than driving in a unipolar mode. In fact, for the same motor power dissipation, the bipolar mode provides 40% higher torque compared to the unipolar mode.

However, driving a stepper motor in bipolar mode requires more complex circuitry than unipolar mode. Typically, two H-bridges and current-control circuitry are needed to drive a bipolar stepper motor. Fortunately, today there are numerous motor-driver ICs that provide the necessary power H-bridge drivers. Many of these motor-driver ICs feature two H-bridges, and many also provide current-control circuitry.

Stepper motor users still have to make a cost/benefit analysis of the improved torque with the bipolar drive mode verses the increased cost of the drive electronics. Therefore, there is a constant market need to reduce the cost of bipolar stepper motor-driver ICs. The A3966 dual H-bridge motor-driver IC was developed specifically to provide a very low cost solution for driving bipolar stepper motors.

MINIMIZING COSTS

The principal objective of this development project was to produce a power IC that would meet the majority of bipolar stepper driver applications with the lowest possible cost. Reducing cost was the key theme for each decision made throughout both the product definition and actual design phases of the A3966.

To satisfy the basic needs of driving a bipolar stepper motor with the most cost-effective solution, the following basic development goals were established for the A3966:
— provide two full H-bridges,
— integrate current-control circuitry,
— utilize cost effective package, and
— minimize external components.

Providing both power H-bridges in one IC would maximize the well-known advantages of integration. However, because the A3966 would have to dissipate the power of *two* H-bridges, the power outputs would have to be optimized for low saturation voltages to reduce the on-chip power dissipation.

The output drivers would need to be rated for at least ±500 mA and 30 V. The 30 V rating would allow the use of the cost-effective DABiC4 process (described later). By not having to increase the chip size for a higher voltage rating, the principle goal of minimizing cost while satisfying the maximum number of bipolar stepper motor applications would still be met. Internal ground-clamp and flyback diodes would be provided to eliminate the need for external diodes.

This low-cost motor-driver IC would also feature an internal current-control circuit. To minimize both the number of external components and the package pin count, a fixed-frequency, pulse-width modulated (PWM) topology would be implemented. With a fixed-frequency topology, only one external RC network is needed to set up the PWM frequency. Additional external filtering

components would not be needed, as the A3966 would incorporate a patented circuit that uses the capacitor in the RC timing network to also set a user-selectable blanking window that prevents false triggering of the PWM current-control circuitry during switching transients.

Generally, in the IC industry, the cost of an IC package is proportional to its size (i.e., the higher the number of pins, the more expensive). To minimize cost, the smallest possible package would be used for the A3966. The bare minimum of functional pins needed for A dual H-bridge motor driver IC with PWM current control is:

	Pins Needed
two outputs per bridge	4
phase & enable logic inputs for each bridge	4
sense connection for each bridge	2
logic supply	1
motor supply	1
reference input	1
RC timing pin	1
ground	1
Minimum Pins Needed	15

The 16-lead SOIC package and 16-pin dual in-line package (DIP) were targeted. Both of these packages are produced in very high volumes and are reasonably low cost. In order to keep the pin count at sixteen, several desirable, but not necessary, features were eliminated. Limiting the number of features also kept the cost of the silicon to a minimum. Because the A3966 is a *power IC*, the power dissipation capabilities of the package also had to be considered. For the surface-mount package version, a reasonable compromise was reached by using a modified 16-lead SOIC package with two leads used as heat sink tabs (thus using all 16 available pins). For the through hole package version, the standard 16-pin DIP with a copper lead frame was used as it has a reasonable thermal capability for the lowest cost.

FUNCTIONAL DESCRIPTION

Logic Inputs

For each bridge of the IC, a PHASE input controls the load-current polarity by selecting the appropriate source-driver and sink-driver pair. An ENABLE input, when held high, disables all the power outputs for that bridge. A logic low on the ENABLE input turns on the selected source and sink driver pair of that H-bridge (see figure 1).

H-bridge Power Outputs

As noted above, the H-bridge power outputs are rated for operating voltages up to 30 V. To reduce the on-chip power dissipation, the sink driver outputs in particular have been optimized for low saturation voltages. The A3966 PWM topology only chops the source drivers, and therefore the sink drivers are always on during the PWM chop cycle (see figure 2). Optimizing the sink drivers for low saturation voltages gave the biggest return for die size utilization.

The sink drivers feature a patented Satlington™ output structure. The Satlington outputs combine the low voltage drop of a *sat*urated transistor and the high peak current capability of a Dar*lington*. Figure 3 shows a representative circuit of the Satlington.

To achieve a low output-voltage drop, a comparatively large current source I1 (~17 mA) is used to drive the base of Q1. This produces the low output-voltage drop that is typical of a saturated transistor for low-to-moderate current levels.

To achieve a higher output-current capability, a comparatively small current source I2 (~1 mA) is used to drive the base of Q2. When Q1 starts to come out of saturation at high load current levels, I2 and Q2 provide an increase in base drive current to Q1 (Q1 and Q2 operate as a Darlington). This allows Q1 to achieve a much higher output-current capability at a somewhat increased output voltage drop (essentially an additional V_{BE}).

When Q1 is saturated, the anti-inverse conduction clamp circuit diverts the I2 current source. This prevents Q2 from inversely conducting, which would divert base drive current from Q1.

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The Satlington driver thus achieves the low voltage drop typical of a saturated npn power transistor at low-to-moderate current levels, while maintaining the high peak-current capability of a Darlington driver. Such an arrangement is ideal for driving motors, as motors often require high peak currents at startup but have lower run currents. It is the lower run current that predominantly determines the power dissipation requirements of the motor driver.

The source drivers of the H-bridges are conventional npn Darlingtons driven by a pnp.

Although the original design specification for the power outputs was ±500 mA, the actual outputs are in fact capable of delivering well over 1 A (the latest version of the A3966 is rated at ±650 mA, continuous; ±750 mA, peak). Figure 4 shows the $V_{CE(SAT)}$ curves of the source outputs and the Satlington sink outputs.

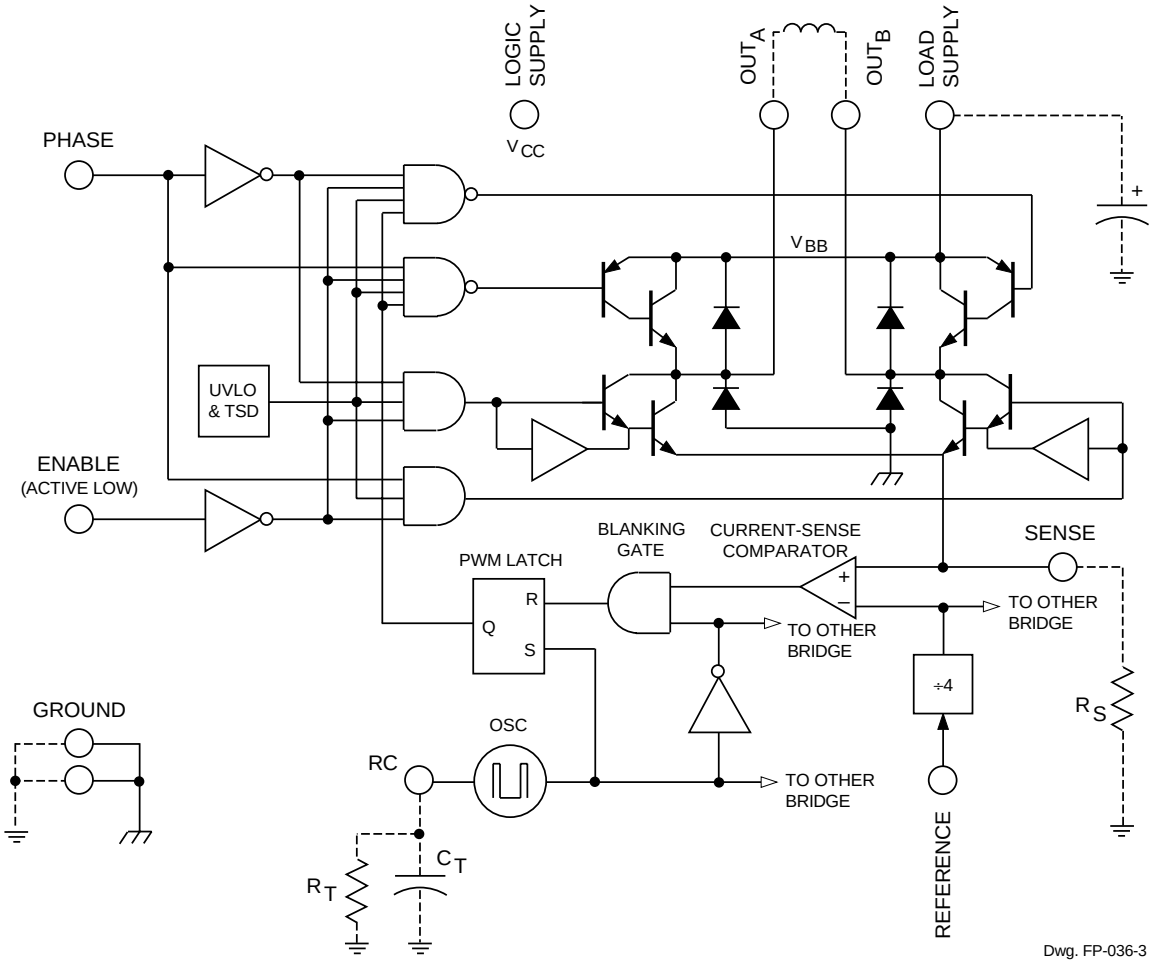

Figure 1: Functional block diagram

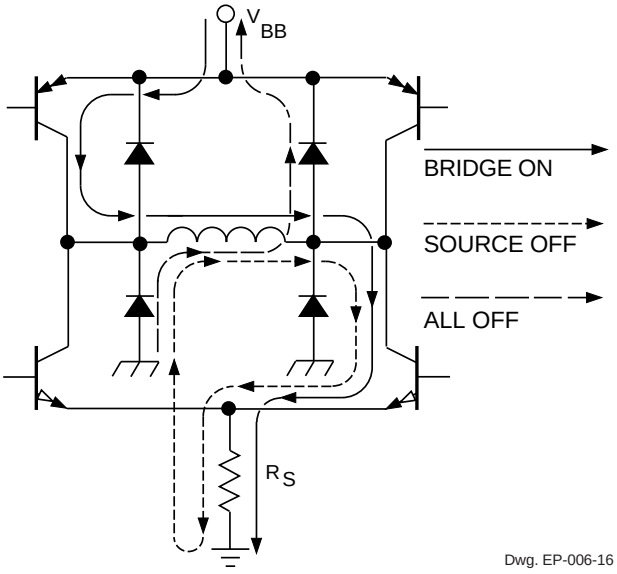

Figure 2: Current paths during PWM chopping

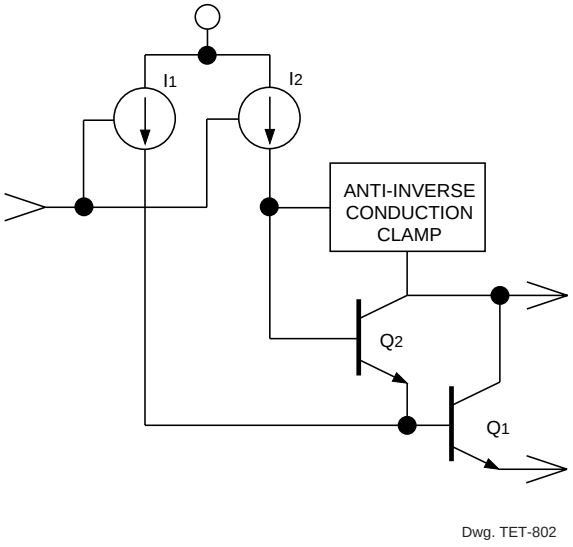

Figure 3: Satlington structure

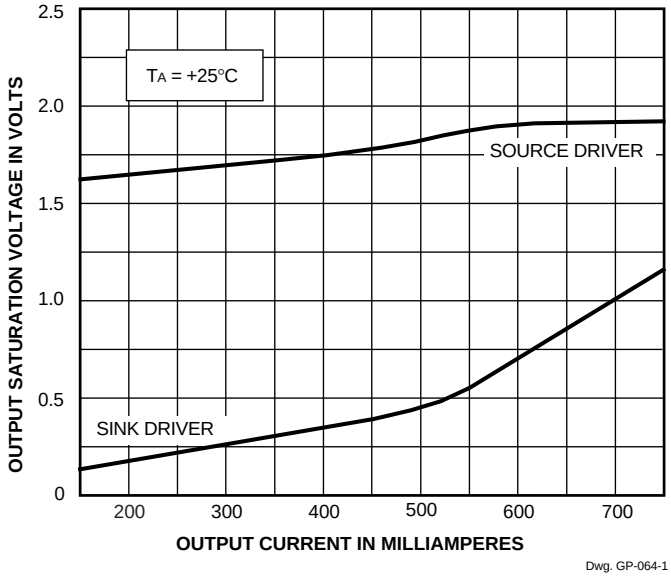

Figure 4: Output saturation voltages

A substrate-isolated diode structure is used for both the ground-clamp and flyback diodes. These diodes protect the source and sink outputs from the potentially destructive transients that are produced by the inductive nature of a stepper motor. Compared to a conventional collector-base diode, this substrate-isolated diode has a much lower parasitic current when conducting.

This results in significantly lower power dissipation when the outputs are switching, and improved output current-handling capability.

Current Control

The fixed-frequency PWM circuit in the motor-driver IC is a commonly used method to control the load current in each motor winding. The current-control circuit works as follows. When the outputs of an H-bridge are turned on, current increases in the motor winding and is sensed by the current-control comparator via an external sense resistor (R_S). Load current continues to increase until it reaches a predetermined value, which is set by selection of the external current-sensing resistor and reference input voltage (V_{REF}) according to the equation:

$$I_{TRIP} = V_{REF}/4R_S$$

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Due to the base-drive current of the sink driver transistor (typically 18 mA), the actual *load* current will be slightly lower:

$$I_{OUT} = I_{TRIP} - 18\ mA$$

At the trip point, the comparator resets the source-enable latch and turns off the source driver for that H-bridge. The source turn off of one H-bridge is independent of the other H-bridge. The inductance of the stepper motor causes the current to recirculate through the ground clamp diode and the sink driver (see figure 2). During this recirculation, the current decreases until the internal clock oscillator sets the source-enable latches of *both* H-bridges, thereby enabling the source drivers of both bridges. The motor winding current again increases, and the cycle is repeated.

External R_T and C_T timing components set the frequency of an internal free-running oscillator, which in turn determines the PWM latch reset frequency and comparator blanking time of the internal PWM current control loop. At the beginning of an oscillator cycle, a 1 mA current source is enabled to charge timing capacitor C_T from a voltage of $0.22V_{CC}$ to $0.6V_{CC}$ (nominally 1.1 V to 3 V). The charging time determines the duration of the PWM set/blanking signal for the PWM current control circuitry (described below).

When voltage on the R_TC_T network reaches $0.6V_{CC}$, the internal 1 mA charging current source is disabled. The voltage on the R_TC_T network decays in one RC time constant to $0.22V_{CC}$, at which point in time the charging current source is re-enabled and the oscillator cycle repeats. This RC time constant and the blank pulse set the frequency of the oscillator (See figure 5):

$$f_{OSC} = 1/(R_TC_T + t_{blank})$$

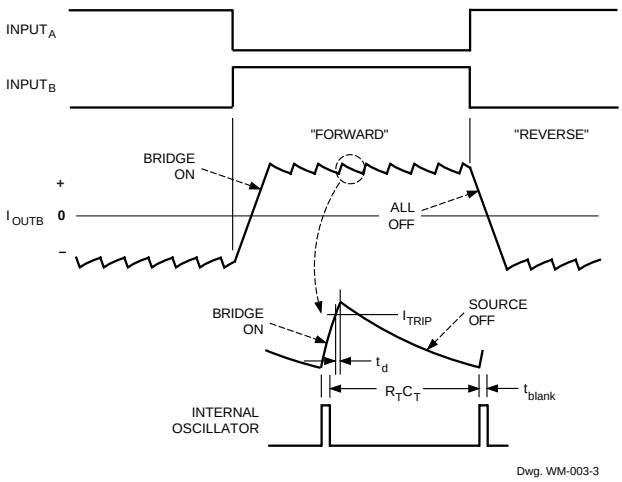

Figure 5: Timing waveforms

Comparator Blanking

When the source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and the distributed capacitance of the stepper motor. This current spike needs to be filtered to prevent false resetting of the source-enable latch. For many motor-driver ICs, an external low-pass RC filter is used to "blank" this current spike. To eliminate the expense of these additional external components, the A3966 employs a patented circuit technique that uses timing capacitor C_T to set a "blanking pulse." This pulse blanks the output of the current-control comparator for a short period of time when the source driver is turned on.

As noted above, the time required for the 1 mA current source to charge timing capacitor C_T from a voltage of $0.22V_{CC}$ to $0.6V_{CC}$ determines the blanking pulse width. Because the 1 mA current source is much larger than the current through R_T in the R_TC_T network, the time it takes to charge C_T, and therefore the blanking time, can be approximated as:

$$t_{blank} = 1900\ C_T$$

A nominal C_T value of 680 pF will give a blanking time of 1.3 µs.

To prevent similar problems due to current spikes generated when the H-bridge outputs are switched by the PHASE or ENABLE inputs, the current-control comparator is blanked by an internally generated blank time of approximately 1 µs. This blanking time for PHASE or ENABLE switching had to be internally generated because the single R_TC_T could only be used for blanking during chopping with the internal current-control circuitry.

Protection Circuitry

An under-voltage lockout circuit protects the A3966 from potential shoot-through currents if the motor-supply voltage is applied before the logic-supply voltage. All outputs are disabled until the logic supply voltage is above 4.1 V, at which time the control logic is able to correctly control the state of the outputs.

Thermal protection circuitry turns off all the power outputs if the junction temperature exceeds 165°C. As with most integrated thermal shutdown circuitry, this is intended only to protect the A3966 for failures due to excessive junction temperature and does not imply that output short circuits are permitted. Normal operation is resumed when the junction temperature has decreased by about 15°C.

Miscellaneous Circuitry

The V_{REF} input is buffered by a unity-gain amplifier to avoid impedance-matching problems between the external and internal resistor dividers. This buffered voltage is divided by four in the control circuitry and then compared by the current-sense comparators as described above.

Most of the control blocks have bias currents that are set up by a trimmed V_{BE}/R current-reference circuit. This optimizes the base drive current requirements for the Satlington sink drivers and the R_TC_T charging current.

APPLICATIONS

For typical applications, the A3966 met its development goal of requiring a minimum number of external components to drive a bipolar stepper motor. The external components needed are:

— two current-sense resistors (R_S) for the current-sense comparators,
— R_T & C_T to set the timing for the internal oscillator and blanking,
— V_{REF} resistor divider to set the reference input voltage (V_{REF}), and
— decoupling capacitors for the logic and load supplies.

Figure 6 shows a typical application with the A3966 (SOIC package) driving a bipolar stepper motor. In this application, the current trip threshold is set for 500 mA, the frequency of the oscillator is approximately 25 kHz, and the blanking time is 1.3 µs.

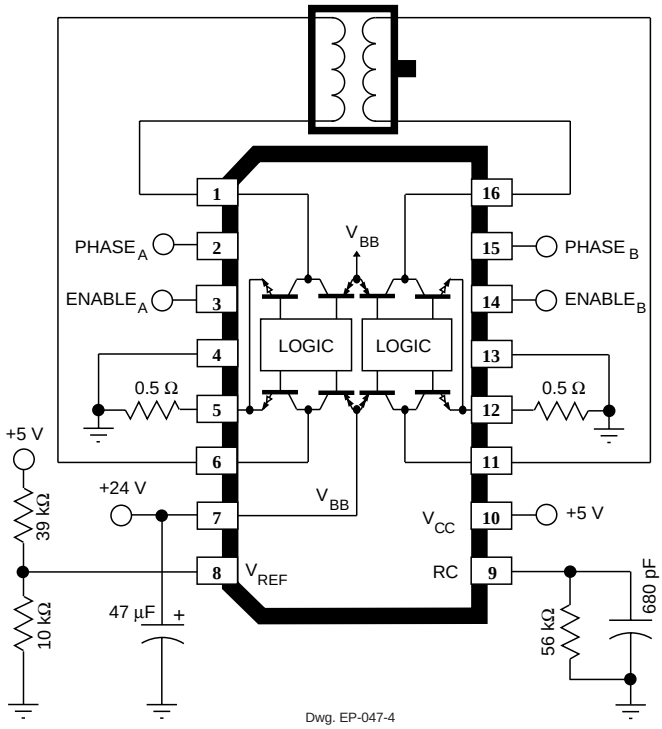

Figure 6: Typical application

The A3966 can drive a bipolar stepper motor in full-step, half-step, or modified half-step modes. Figure 7 shows the logic input sequences for full-step, half-step, and modified half-step operation.

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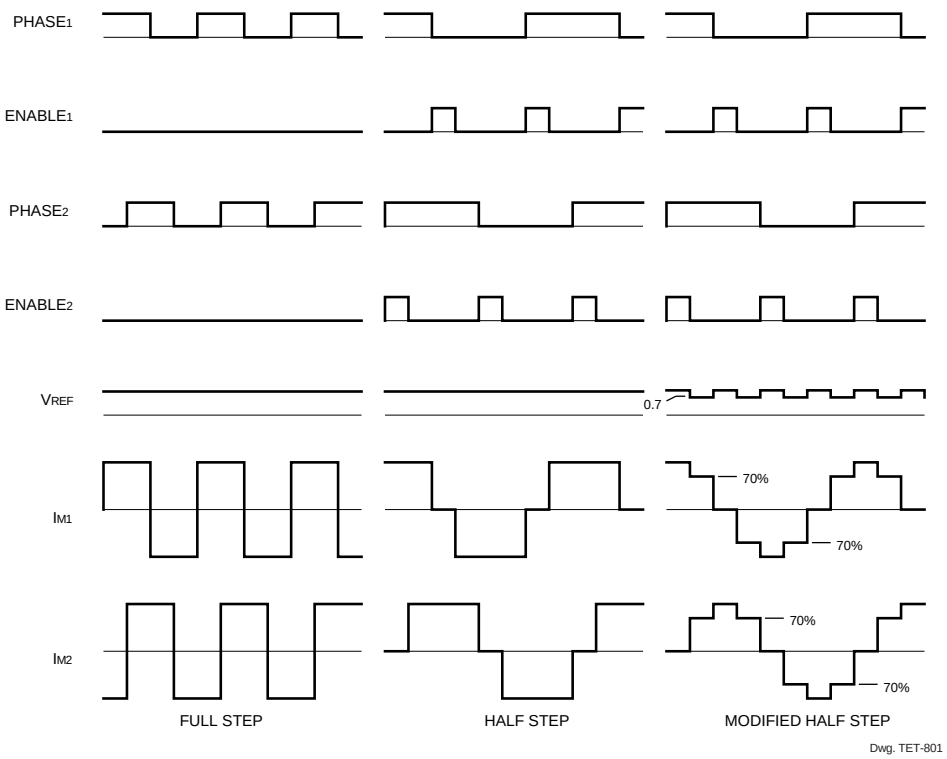

Figure 7: Step waveforms

In full-step operation, both motor windings are energized at the same time with the same current value. For the motor to take one step, the current (and the magnetic field) is reversed in one winding. The motor will advance another step when the current in the other winding is reversed. This sequence is repeated, resulting in four distinct states. Figure 8 shows an oscilloscope trace of current in the motor windings for the A3966 in full-step operation.

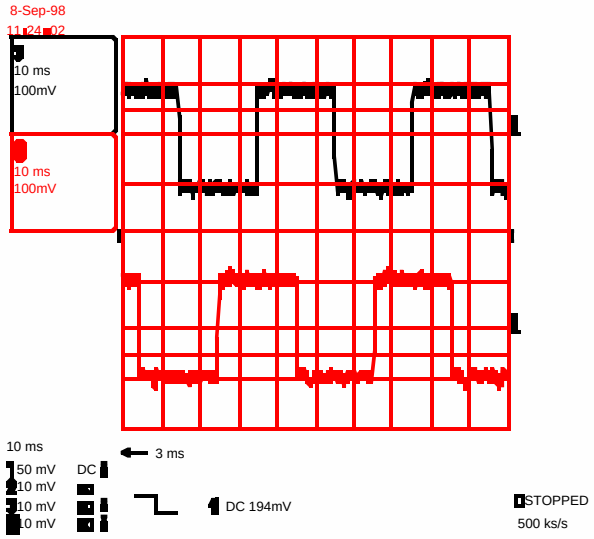

Figure 8: Motor winding currents in full-step mode

There are eight distinct states in half-step operation. In half-step mode, the current in a motor winding is brought to zero before a complete current reversal takes place. This action results in the stepper motor taking two "half-steps," which equates to one full step of motor rotation. Figure 9 shows a scope trace of the current in the motor windings for the A3966 in half-step operation.

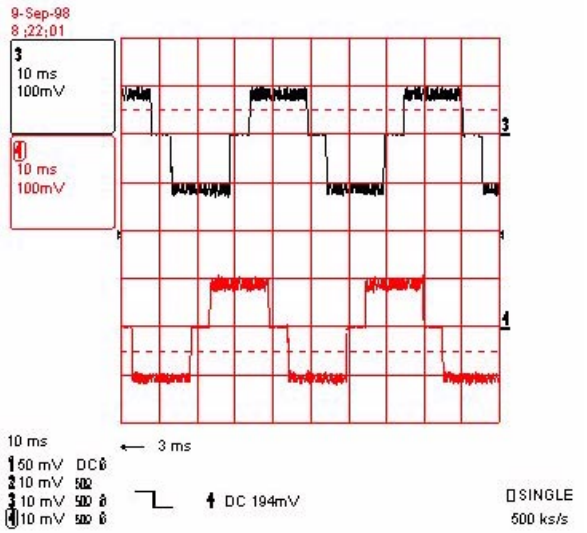

Figure 9: Motor winding currents in half-step mode

Because current is flowing in only one motor winding during the half-step position, the torque in this half-step position is 70% of the full-step position (when current in flowing in both motor windings). Using a modified half-step mode can alleviate the torque variations between the half-step and full-step positions. In this modified (constant-torque) half-step mode, the current in the motor winding is increased 1.4 times during the half-step position. Figure 10 shows a scope trace of the current in the motor windings for the A3966 in modified half-step operation.

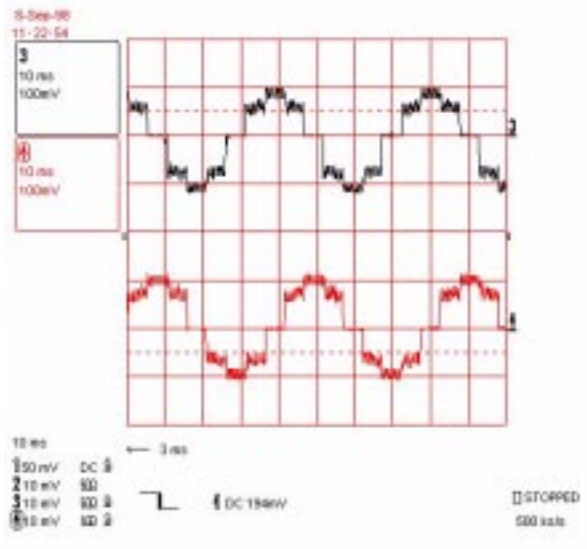

Figure 10: Motor winding currents in modified half-step mode

Figure 11 shows the oscilloscope trace of the RC terminal and the current in both windings of a bipolar stepper motor. Note that the PWM waveform of the recently enabled bridge becomes repetitive after only a few chopping cycles.

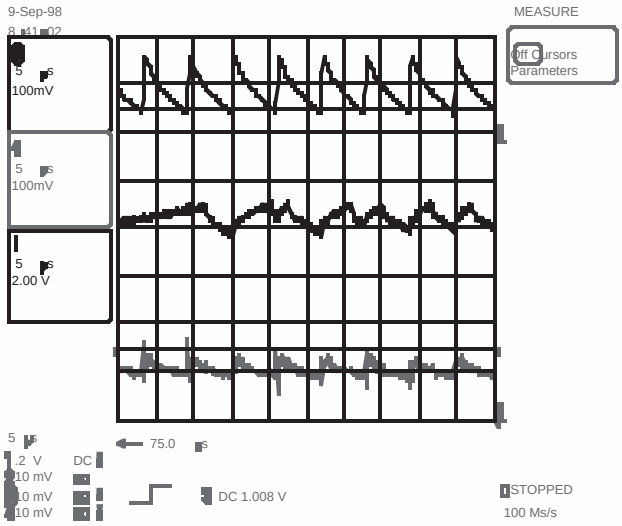

Figure 11: Winding current PWM waveforms

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The frequency of the oscillator will determine the amount of ripple current in the motor windings. A lower frequency will result in higher current ripple, but reduced heating in the motor and the A3966 due to a corresponding decrease in hysteretic core losses and switching losses respectively. A higher frequency will reduce ripple current, but will increase the switching losses and EMI.

DABiC4

The A3966 is fabricated on Allegro Microsystems' DABiC4 (*D*igital *A*nalog *Bi*polar *C*MOS, version *4*) process. DABiC4 is a two-level metal, high-voltage BiCMOS process, combining 2 micron CMOS with 30 V power bipolar transistors. The thick second-level metal facilitates the design of efficient power transistors. The ability to use CMOS instead of bipolar transistors for much of the control functions significantly reduced the area (and cost) needed for the control logic.

DABiC4 has a p buried layer, which allowed the A3966 to incorporate substrate-isolated diodes to be used as output ground-clamp and flyback diodes.

DABiC4 is a very cost effective process for ICs such as A3966 that require CMOS logic combined with power outputs.

CONCLUSION

A new low-cost dual H-bridge motor driver IC has been developed that reduces the cost of driving bipolar stepper motors. The A3966 chip, shown in Figure 12, has met the design objectives of offering two H-bridges, plus current-control circuitry that requires few external components, all in an inexpensive package.

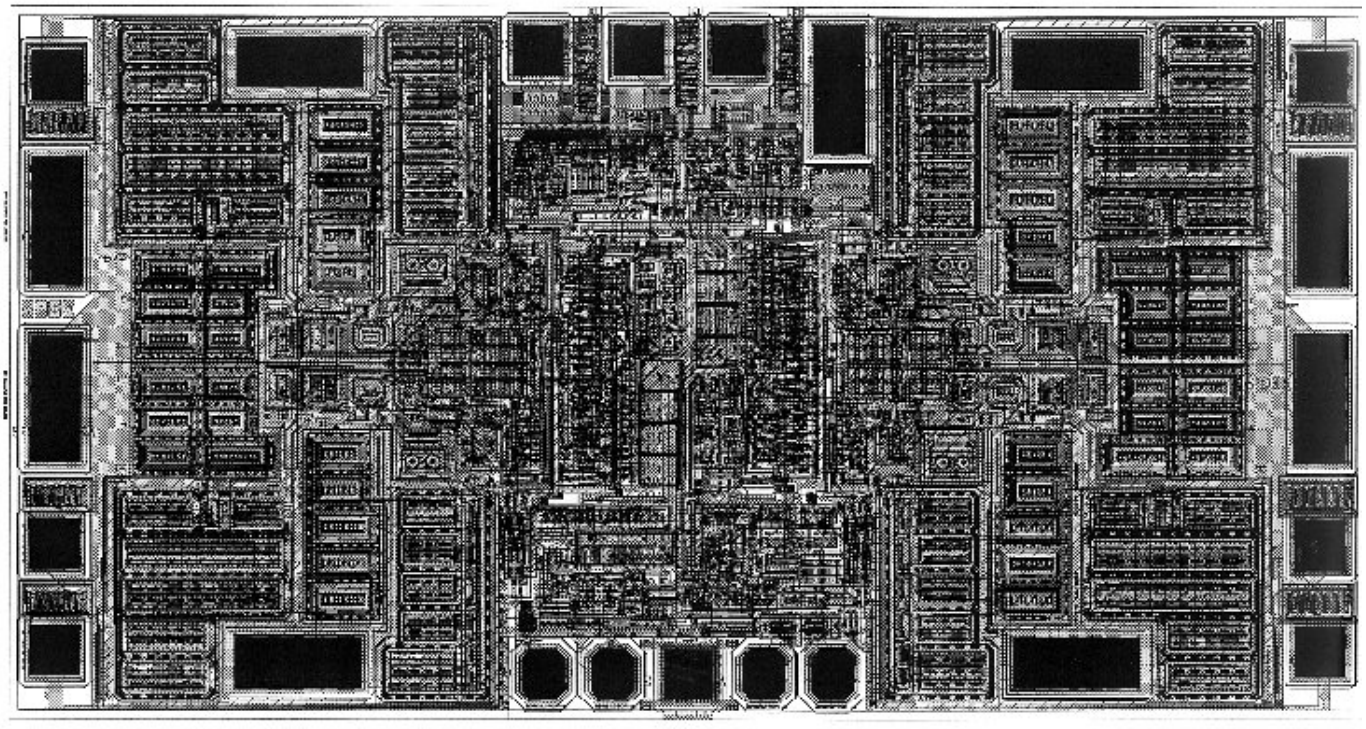

Figure 12: A3966 die layout

REFERENCES

Murari, B., Bertotti, F., Vignola, G.A. (Eds.), "Smart Power ICs", Springer Verlag, 1995.

Emerald, P., "A Design Regimen for Resolving the Selection of Integrated Power Electronic Step Motors", Powersystems World, 1996.

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