ASEK70331, Board, Demo, SOIC8, Bare Board

TED-0002335-FAB
Originator: M. Siopes

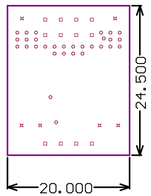
FAB Drawing / FAB Notes and Requirements

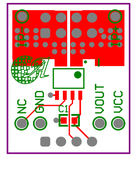
Rev 1
10/10/2017

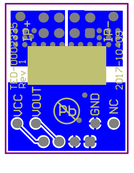
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.40mil	3.5	
3	TopLayer	Copper	2.80mil		
4	Dielectric1	FR-4	55.60mil	4	
5	BottomLayer	Copper	2.80mil		
6	BottomSolder	Solder Resist	0.40mil	3.5	
7	BottomOverlay				

Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
⌖	30	15.00mil (0.381mm)	PTH	Round	Via
⌘	6	36.00mil (0.914mm)	PTH	Round	Pad
□	12	40.00mil (1.016mm)	PTH	Round	Pad
	48 Total				

1. Finished PCB is RoHS
2. Dimensions are in millimeters, unless otherwise noted.
3. Applicable Standards:
   - 3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   - 3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   - 3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   - 4a. Thickness: 0.062inch +/- 10%
   - 4b. Type: high temp FR4
   - 4c. this line left blank
   - 4d. Core/prepreg thickness:
     - 4d.1. See chart to left.
     - 4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
     - 4d.3. No impedance controlled stackup required
5. Copper:
   - 5a. Layer Count: 2
   - 5b. Exterior layers: 2oz min
   - 5c. Interior layers: N/A
   - 5d. Plated through holes: plate to 1mil min copper thickness
   - 5e. Trace separation: 5mil
   - 5f. Trace min width: 8mil
   - 5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   - 5h. No impedance controlled route used; no trace width adjustment required.
6. this line left blank
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   - 9a. Immersion Gold
   - 9b. No hard gold required, no *.gm8 nor *.gm9 layer provided
10. Soldermask:
    - 10a. Top/Bottom soldermask required
    - 10b. Soldermask color shall be green.
    - 10c. Soldermask finish may be matte or glossy.
11. Silkscreen
    - 11a. Top/bottom silkscreen required.
    - 11b. Silkscreen color shall be white.
    - 11c. Min silkscreen line width: 4mil
    - 11d. Epoxy or acrylic ink allowed
    - 11e. Photoimaging or inkject printing shall be used
    - 11f. Allegro Logo shall be printed as accurately as possible.
      - 11f1. Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
12. Drill holes:
    - 12a. No blind or buried vias.
    - 12b. Hole sizes are specified after plating.
    - 12c. No via in pad used. No via filling required.
13. Mill separate according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
    - 15a. Matt Siopes, msiopes@allegromicro.com, 603.626.2610
    - 15b. If fast turn board, 24hr contact info: N/A




NC
GND
C1
VOUT
VCC


VCC
VOUT
GND
NC