ASEK31300, Demo, DFN10

TED-0002209-FAB
Originator: S. Upton

FAB Drawing / FAB Notes and Requirements

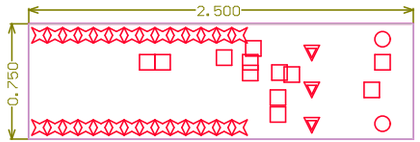
Rev 1
5/26/2017

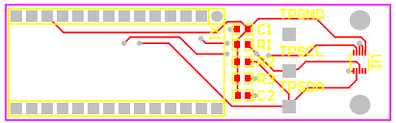
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopPaste				
2	TopOverlay				
3	TopSolder	Solder Resist	0.40mil	3.5	
4	TopLayer	Copper	1.40mil		
5	Dielectric1	FR-4	58.00mil	4	
6	BottomLayer	Copper	1.40mil		
7	BottomSolder	Solder Resist	0.40mil	3.5	
8	BottomOverlay				
9	BottomPaste				

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
○	2	130.00mil (3.302mm)	NPTH	Round
▼	3	62.00mil (1.575mm)	PTH	Round
□	12	15.00mil (0.381mm)	PTH	Round
¤	28	42.00mil (1.067mm)	PTH	Round
	45 Total			

1. Finished PCB is RoHS
2. Dimensions are in inches, unless otherwise noted.
3. Applicable Standards:
   3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   4a. Thickness: 0.062inch +/- 10%
   4b. Type: high temp FR4
   4c. this line left blank
   4d. Core/prepreg thickness:
      4d.1. See chart to left.
      4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
      4d.3. No impedance controlled stackup required
5. Copper:
   5a. Layer Count: 2
   5b. Exterior layers: 1oz min
   5c. Interior layers: n/a
   5d. Plated through holes: plate to 1mil min copper thickness
   5e. Trace separation: 7mil
   5f. Trace min width: 10mil
   5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   5h. No impedance controlled route used; no trace width adjustment required.
6. this line left blank
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   9a. Immersion Gold
   9b. No hard gold required, no *.gm8 nor *.gm9 layer provided
10. Soldermask:
   10a. Top/Bottom soldermask required
   10b. Soldermask color shall be green.
   10c. Soldermask finish may be matte or glossy.
11. Silkscreen
   11a. Top silkscreen required; bottom not required.
   11b. Silkscreen color shall be white.
   11c. Min silkscreen line width: 8mil
   11d. Epoxy or acrylic ink allowed
12. Drill holes:
   12a. No blind or buried vias.
   12b. Hole sizes are specified after plating.
   12c. No via in pad used. No via filling required.
13. Mill separate or V-score according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
   15a. Shawn Upton supton@allegromicro.com, 603.626.2429
   15b. If fast turn board, 24hr contact info: N/A

Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 *.gm8 is top selective hard gold
Mechanical Layer 9 *.gm9 is bottom selective hard gold
Mechanical Layer 10 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperature file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house




TPGND
C1
R1
TPSCL
TPSDA
VIN
GND
SCL
SDA
VCC


ASEK30 Demo (bare board)
2209 R1
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