ASEK71240, Demo, Bare Board

TED-0002302-FAB
Originator: M. Siopes

FAB Drawing

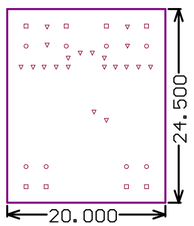
Rev 1
8/31/2017

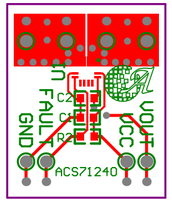
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.40mil	3.5	
3	TopLayer	Copper	2.80mil		
4	Dielectric1	FR-4	25.40mil	4	
5	BottomLayer	Copper	2.80mil		
6	BottomSolder	Solder Resist	0.40mil	3.5	
7	BottomOverlay				

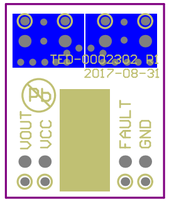
Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
▽	20	15.00mil (0.381mm)	PTH	Round	Via
□	8	24.00mil (0.610mm)	PTH	Round	Pad
○	8	36.00mil (0.914mm)	PTH	Round	Pad
	36 Total				

1. Finished PCB is RoHS
2. Dimensions are in millimeters, unless otherwise noted.
3. Applicable Standards:
   3a. Manufacture in accordance to IPC-6011, IPC-6012.
   3b. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   4a. Thickness: 0.062inch
   4b. Type: FR4
5. Copper:
   5a. Layer Count: 2
   5b. Exterior layers: 2oz
   5c. Interior layers: N/A
   5d. Plated through holes: plate to 1mil min copper thickness
   5e. Trace separation: 5mil
   5f. Trace min width: 10mil
6. Surface Finish:
   6a. Immersion Gold
   6b. This line left intentionally blank.
7. Soldermask:
   7a. Top/Bottom soldermask required
   7b. Soldermask color shall be green.
8. Silkscreen
   8a. Top/bottom silkscreen required.
   8b. Silkscreen color shall be white.
   8c. Min silkscreen line width: 6mil
   8d. Epoxy or acrylic ink allowed
9. Drill holes:
   9a. No blind or buried vias.
   9b. Hole sizes are specified after plating.
10. Mill separate or V-score according to mech1 (*.g1) layer.
11. Contact information:
    11a. Matt Siopes, msiopes@allegromicro.com, 603.626.2610
    11b. If fast turn board, 24hr contact info:

Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperature file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house




U1
FAULT
GND
C2
C1
R2
VOUT
VCC
ACS71240


TFD-0002302 R1
2017-08-31
VOUT
VCC
FAULT
GND