ASEK724-5, Board, Demo, SOIC16

85-0815-003-FAB
Originator: S. Upton

FAB Drawing / FAB Notes and Requirements

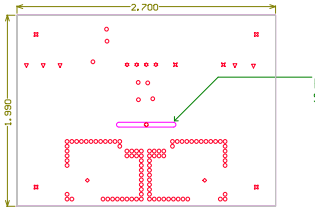
Rev 1
10/2/2015

Layer Stack Up Detail for: 85-0738-003-R1.PCBDOC

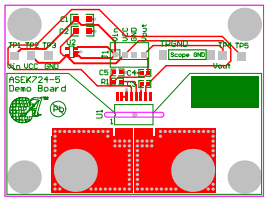
Layer Name	Gerber Document	Copper Thickness
TopLayer	(.GTL)	5.6mil
BottomLayer	(.GBL)	5.6mil

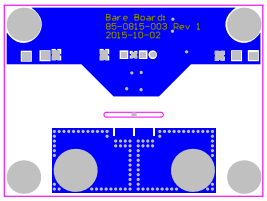
1. Finished PCB is RoHS
2. Dimensions are in inches, unless otherwise noted.
3. Applicable Standards:
   - 3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   - 3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   - 3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   - 4a. Thickness: 0.062inch +/- 10%
   - 4b. Type: high temp FR4
   - 4c. this line left blank
   - 4d. Core/prepreg thickness:
     - 4d.1. See chart to left.
     - 4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
     - 4d.3. No impedance controlled stackup required
5. Copper:
   - 5a. Layer Count: 2
   - 5b. Exterior layers: 4oz min
   - 5c. Interior layers: N/A
   - 5d. Plated through holes: plate to 1mil min copper thickness
   - 5e. Trace separation: 10mil
   - 5f. Trace min width: 10mil
   - 5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   - 5h. No impedance controlled route used; no trace width adjustment required.
6. this line left blank
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   - 9a. Immersion Gold
   - 9b. No hard gold required, no *.gm8 nor *.gm9 layer provided
10. Soldermask:
    - 10a. Top/Bottom soldermask required
    - 10b. Soldermask color shall be green.
    - 10c. Soldermask finish may be matte or glossy.
11. Silkscreen
    - 11a. Top/bottom silkscreen required.
    - 11b. Silkscreen color shall be white.
    - 11c. Min silkscreen line width: 4mil
    - 11d. Epoxy or acrylic ink allowed
    - 11e. Photoimaging or inkject printing shall be used
    - 11f. Allegro Logo shall be printed as accurately as possible.
      - 11f1. Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
12. Drill holes:
    - 12a. No blind or buried vias.
    - 12b. Hole sizes are specified after plating.
    - 12c. No via in pad used. No via filling required.
13. Mill separate according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
    - 15a. Shawn Upton supton@allegromicro.com, 603.626.2429
    - 15b. If fast turn board, 24hr contact info: N/A

Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 *.gm8 is top selective hard gold
Mechanical Layer 9 *.gm9 is bottom selective hard gold
Mechanical Layer 10 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperature file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house



50mil wide slot to be milled here
Feature is on mech1 layer also
Slot is not to be plated


TP1
TP2
TP3
TP4
TP5
TRIGND
Scope GND
Vout
VIN
UCC
GND
C5
C4
R1
ASEK724-5
Demo Board


Bare Board
BB-0015-003 Rev 1
2013-10-02