LAYOUT GUIDELINES FOR PCB LAYOUT OF MOTOR GATE DRIVERS

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ABSTRACT

This application note describes the layout recommendations for printed circuit board (PCB) layouts when designing boards for high frequency, fast switching, and high current for gate driver applications.

Note that the following are only recommendations. Each application is different and may encounter different sensitivities. A driver running a few amperes is less susceptible to EMI than one running hundreds of amperes. Each design must be tested at the maximum current to ensure any parasitic effects are eliminated.

INTRODUCTION

PCB design of motor drive systems in gate driver applications is not trivial and requires special considerations and techniques to achieve the best performance. Power efficiency, high-speed switching frequency, low-noise jitter, and compact board designs are a few primary factors that the PCB layout engineer must consider with electromagnetic interference concerns during the layout of a motor drive system. Allegro drivers are ideal for such systems because they are highly integrated and are well equipped with protection circuitries. In a motor drive system, to mitigate issues related to the combination or interaction of the employed motor inductance, PCB layout, and gate driver, it is essential to have a good PCB layout. For this reason, a proper PCB layout at the early stage of a motor drive system design is crucial, and its importance cannot be overlooked.

To highlight the primary factors of motor drive layout, an Allegro gate driver is used here to provide best-practice layout guidelines that reduce electromagnetic interference and also reduce thermal stress, optimize efficiency, and minimize noise for high-performance motor drive applications.

PLACEMENT OF LAYERS

Many designs can benefit from the use of two or more layers of PCBs. On multilayer PCBs, it can be highly desirable to place the DC ground layer between the high-current power-component layer and the sensitive small signal trace layer. Examples of undesired layer arrangements of the four-layer and six-layer PCBs for gate driver circuits are shown in Figure 1, left. In these examples, the small signal layer is placed between the high-frequency, fast-switching, high-current power layer and the ground layer. These configurations typically increase the capacitive noise coupling between the high-frequency, fast-switching, high-current, or voltage power layer and the small analog-signal layer. Examples of desired layer arrangements that minimize the noise coupling in four-layer and six-layer PCB designs are shown in Figure 1, right. In these two examples, the small signal layer is shielded by the ground layer.

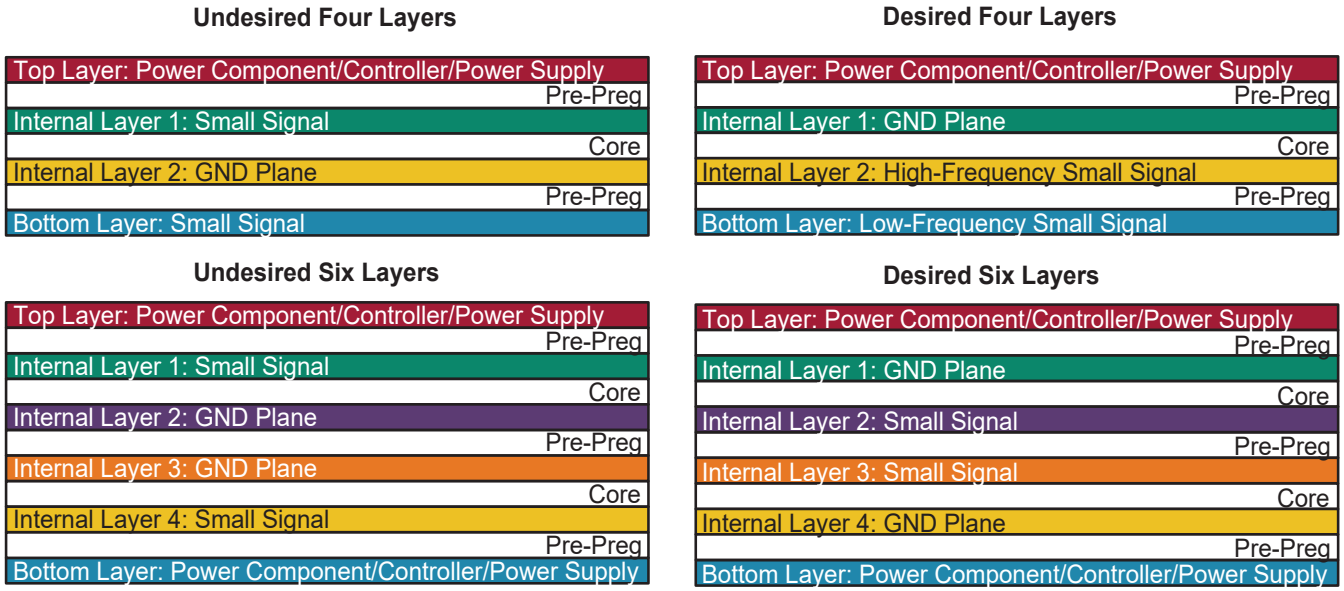


Figure 1: Placement of layers.

Power and ground planes on adjacent layers, with a thin dielectric between them, can also benefit a design. The purpose is not to distribute plane-to-plane decoupling capacitance around the board, but to decrease the inductance loop in the power distribution network, decreasing rail collapse, ground bounce, and electromagnetic interference. To minimize the PCB conduction loss and thermal impedance, a thick copper layer might be beneficial for the external high-frequency, fast-switching, high-current power layers. To minimize noise-fringing effects, ensure PCB traces and planes are kept well away from the edge of the board. A reasonable distance is at least 5 mm.

GROUNDING

Exposed Thermal Pad

The exposed thermal pad should be connected to the ground terminals of the gate driver and should contain thermal vias for adequate heat dissipation.

In the example device in Figure 2, the exposed thermal pad of the Allegro U1 device, highlighted in green, is connected to the ground terminals of the Allegro U1 device. A matrix of thermal vias, five columns by five rows, used to move heat away from the device package to the bottom-layer ground plane is shown in Figure 2.

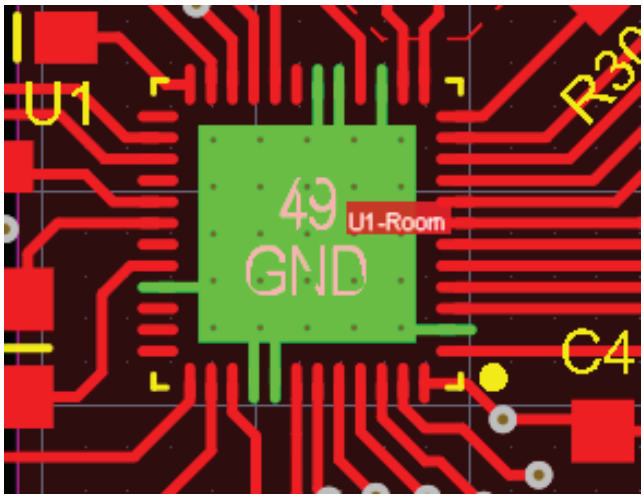


Figure 2: Exposed thermal pad, U1

Ground Terminals

Allegro gate drivers usually include within the device several ground terminals known as analog ground (AGND) and power ground (PGND). These terminals may be internally connected, but they must be connected together on the PCB—as close as practicable to the device—for correct operation. This common point and the high current return of the external MOSFETs should return separately to the negative side of the motor supply filtering capacitor, as shown in the simplified block diagram in Figure 3. This approach minimizes the effect of switching noise on the device logic and analog reference.

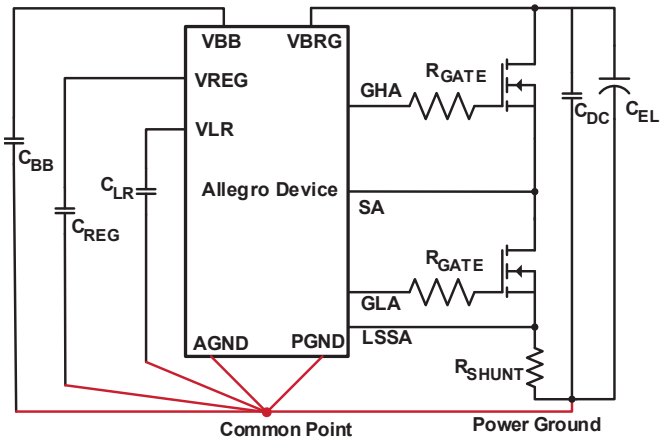


Figure 3: Common-point ground connection

Quiet Ground

If sensitive connections are present—such as the dead-time setting terminal and fault threshold voltage terminal, which have very little ground current—the connections should be made to the quiet ground, which is connected independently, closest to the analog ground terminal, as shown in Figure 4. These sensitive components should never be connected directly to the supply common or to a common ground plane. They must be referenced directly to the analog ground terminal. If layout space is limited, the quiet ground and the controller supply ground may be combined. In this case, ensure that the ground return of the dead-time resistor is located close to the analog ground terminal.

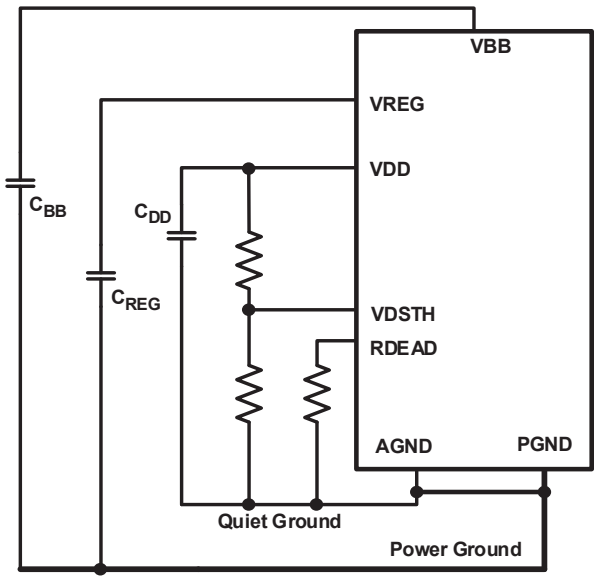


Figure 4: Quiet ground connection

PCB CONNECTIONS

Power MOSFET Traces

Stray inductance should be minimized by using short, wide, copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This minimizes voltages induced by the fast switching of large load currents. Gate-charge drive paths and gate-discharge return paths may carry a large transient current pulse. Therefore, the traces from gate terminals and low-side source terminals should be as short as practicable to reduce trace inductance. To further minimize self-inductance, particular attention should be paid to the area of the gate current loops shown in Figure 5; the GHx/GLx and Sx/LSSx traces should be placed close to one another, which increases the partial mutual inductance between them and thereby reduces the total loop self-inductance. Also, the load connection terminals and the low-side source terminals —Sx and LSSx, respectively—of the MOSFET-gate-discharge return paths should be kept as short as practicable. Any inductance on these terminals is likely to cause negative transitions on the corresponding device terminals, which may exceed the absolute maximum ratings. To limit the negative excursion on terminals with respect to the ground terminal of the device, use of clamping diodes and a capacitor between the LSSx terminals and ground should be considered, as shown in Figure 6.

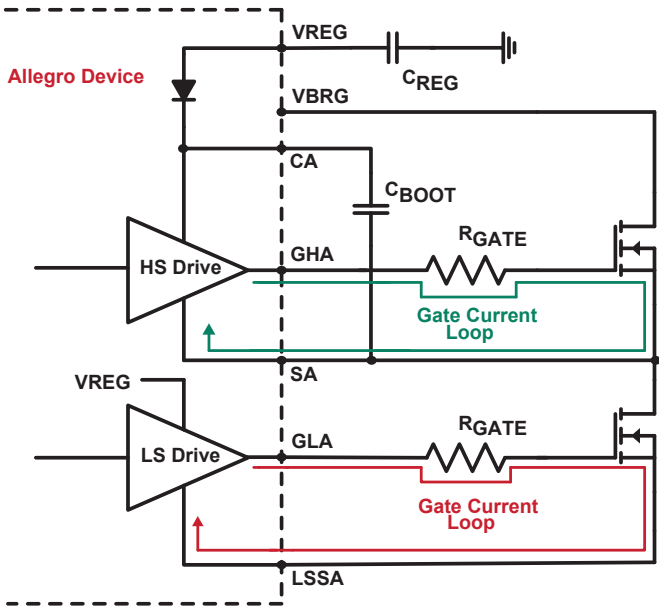


Figure 5: Gate current loops

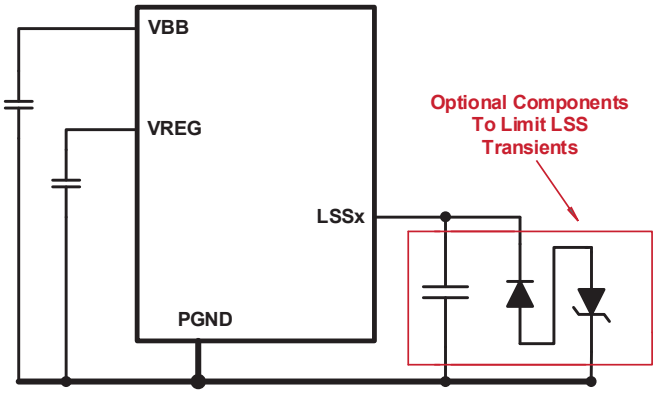


Figure 6: Optional components to limit LSSx transients

Provide an independent connection from each low-side source terminal to the source of the corresponding low-side MOSFET in the power bridge. Connection of the low-side source terminals directly to the ground terminals is not recommended due to the potential for noise to be injected into sensitive functions, such as the various voltage monitors.

Sense Amplifier Connections

If a sense amplifier is present, the current sense positive input terminal and current sense negative terminal should have independent circuit traces. For the best results, they should be matched both in length and route. To minimize losses, the sense amplifier resistor typically has a small resistance value. This is because any series trace resistances can significantly increase the differential sense voltage measured by the current shunt resistor, R_{SH}. Therefore, the addition of a sense amplifier resistor results in error observed on the output of the sense amplifier. The layout of the current shunt resistor is particularly important. This is because shunt resistors have resistance that is, on an order of magnitude, similar to PCB traces. To eliminate any impact of board trace resistances, use of the Kelvin connection and symmetric input traces is recommended. This approach requires extra care when wiring. Different layouts for the current sense resistor of a gate driver are shown in Figure 7: The layout shown at top is not recommended because any error due to voltage drop across the solder joints and PCB traces can be measured on the output of the sense amplifier; the recommendation is to select the good or best method shown (center and bottom, respectively), depending on the value of the current shunt resistor. If the value of the current shunt resistor is lower than approximately 1 mΩ, the best method shown at bottom should be preferred because the error due to the voltage drop across the solder joints shown at center could affect the reading. Also, in the best method shown at bottom, the load current is free from the sense contacts.

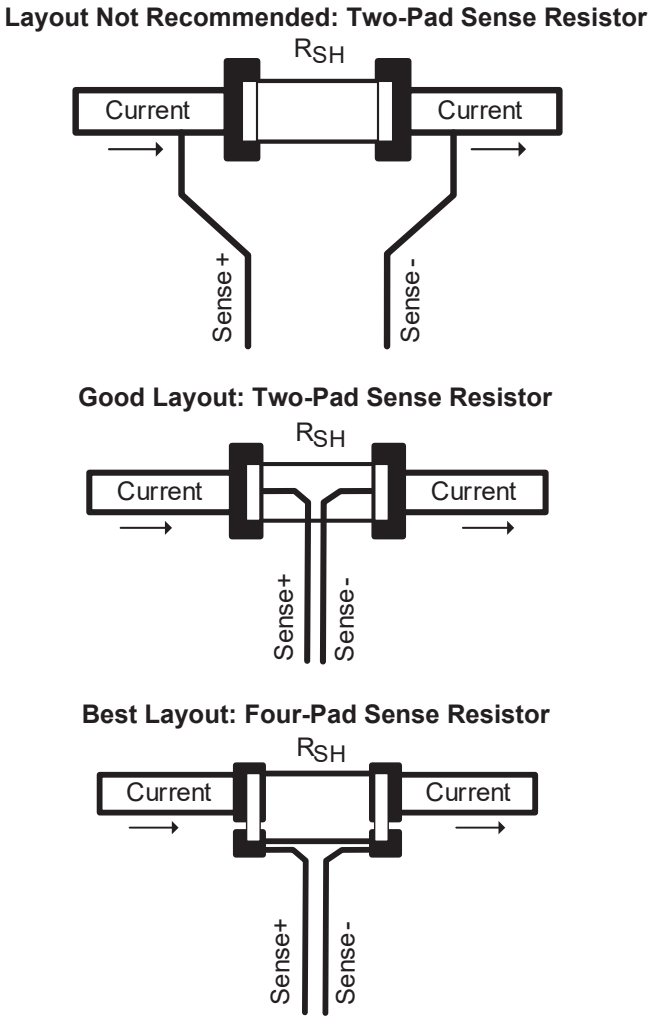


Figure 7: Layout comparisons

Many modern CAD tools implement features that can help the layout engineer correctly route the PCB layout. The net-tie feature described in this section is included as a component type in the Altium Designer tool. However, many other tools have similar features. In the case of the current sense amplifier, the negative input terminal could be directly connected to the ground terminal, and the positive input terminal could be directly connected to the source terminal of the low-side MOSFET. To avoid this situation, net-ties can be placed between the high-impedance input terminals of the sense amplifier of the gate driver and the shunt resistor, and as close as practicable to the current shunt resistor, as shown in Figure 8, to maintain accuracy of the sense amplifier output.

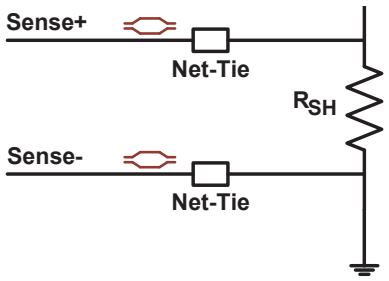


Figure 8: Net-tie placement

CAPACITORS

Supply Decoupling

In switching circuits, such as the example Allegro gate drivers, current spikes from all supplies occur at the switching points. As with all such circuits, the power supply connections should be decoupled with a ceramic capacitor between the supply terminal and ground. These capacitors should be connected as close as practicable to the device supply terminals V_{BB}, V_{DD}, and V_{IO}, and the ground terminal, as shown in Figure 9, in which the V_{BB} supply decoupling capacitor, C16, highlighted in green, is placed on the bottom layer as close as practicable to the Allegro U1 device.

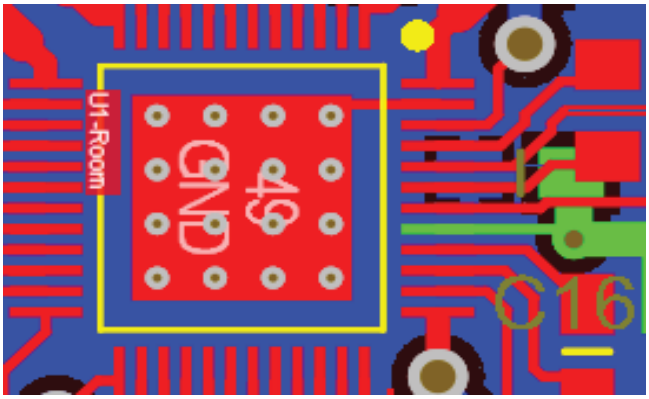


Figure 9: V_{BB} decoupling capacitor, C16

Charge Pump Capacitor

Internal regulator charge pumps provide Allegro devices with a source of regulated voltage for systems internal to the device. When active, to maintain the required supply, the charge pump charges and discharges a flying capacitor at a frequency of 62.5 kHz. The charging and discharging can be a source of noise, so the charge pump capacitors should be placed as close as practicable to the two charge pump terminals. An example of this placement is presented in Figure 10, in which a ceramic capacitor, C21, highlighted in orange, was selected and connected on the top layer as close as practicable to the Allegro U1 device.

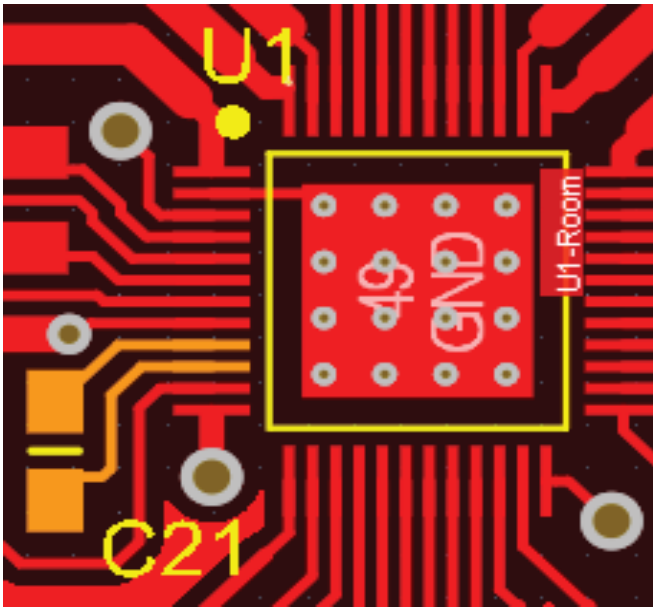


Figure 10: Charge pump capacitor, C21

DC-Link Capacitor

The purpose of the DC-link capacitor is to balance the instantaneous power coming from the main supply, such as the battery power rail, for the purpose of stabilizing the voltage ripple caused by the switching of the MOSFETs in the power bridge. This capacitor needs to be selected as a function of the maximum voltage ripple allowed in the system and its harmonics. Furthermore, to minimize its power dissipation, this capacitor needs to show low equivalent series resistance (ESR) and, for better performance, it should be placed as close as practicable between the drain terminal of the high-side MOSFET (M1), highlighted in pink in Figure 11, and the source terminal of the low-side MOSFET (M2). This is illustrated in Figure 11 by the DC-link capacitor, C18, on the bottom layer of the designed board.

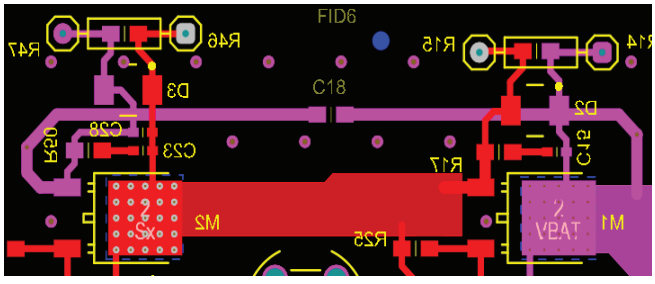


Figure 11: DC-link capacitor, C18

V_{REG} Capacitor

The V_{REG} terminal supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned-on, the gate-drive circuit provides the gate with the high transient current needed to quickly turn on the MOSFET. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the V_{REG} regulator, but must be supplied by an external capacitor connected to the V_{REG} terminal. Thus, the V_{REG} capacitor should be connected independently close to the ground terminal, as close as practicable to the V_{REG} terminal, as shown in Figure 12, in which a V_{REG} capacitor, C6, highlighted in light blue, is placed on the top layer as close as practicable to the Allegro U2 device.

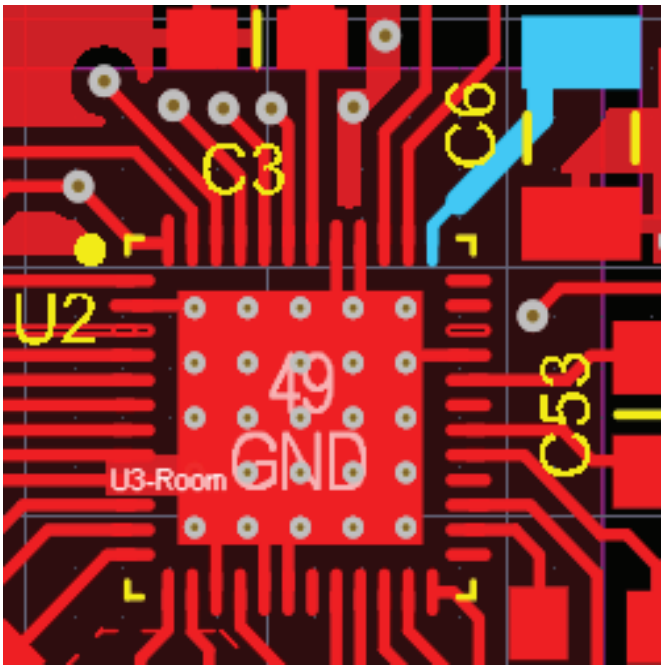


Figure 12: V_{REG} capacitor, C6

Bootstrap Capacitor

The high-side driver supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals—CA, CB, and CC—and the corresponding high-side reference terminals—SA, SB, and SC. The bootstrap capacitors are independently charged to approximately the V_{REG} voltage of a given gate driver when the associated reference Sx terminal is low. For better results, the bootstrap capacitors should be connected as close as practicable to the gate driver between the CA, CB, and CC terminals and their corresponding high-side reference terminals, SA, SB, and SC. This concept is presented in Figure 13, where bootstrap capacitors C53, C54, and C55, highlighted in pink, are connected as close as practicable to the Allegro U2 device.

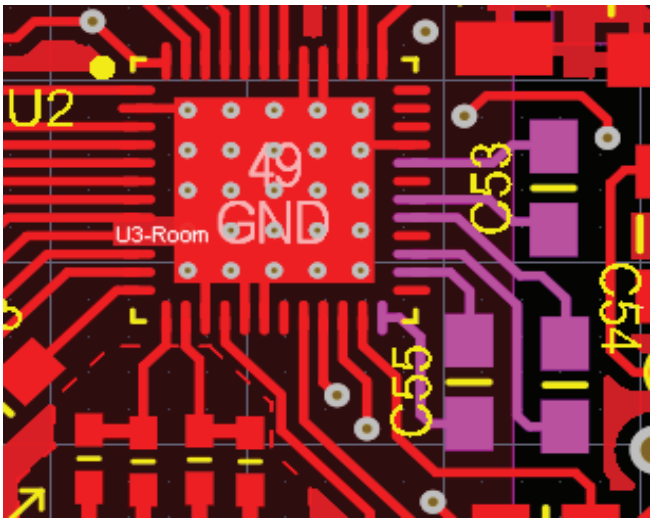


Figure 13: Bootstrap capacitors, C53, C54, and C55

SNUBBER NETWORK

To limit the fast transient voltage spikes caused by the inductance of the circuit trace and the load, use of a small ceramic decoupling capacitor across the sources and drains of the power MOSFETs should be considered. A resistor in series with the decoupling capacitor can be used to dissipate the capacitive energy stored. Therefore, the resistor should be rated to dissipate the capacitive power. The lossless snubber circuit can reduce the effects of the voltage overshoot and ringing when the parasitic components resonate. An example of a snubber network formed by a resistor, R27, and a capacitor, C4, for the high-side MOSFET, M3, is presented in Figure 14. A more detailed analysis of snubber network design is available in the application note Motor Driver Discrete MOSFET Bridge Circuit Design and Layout (AN296215) at www.allegromicro.com.

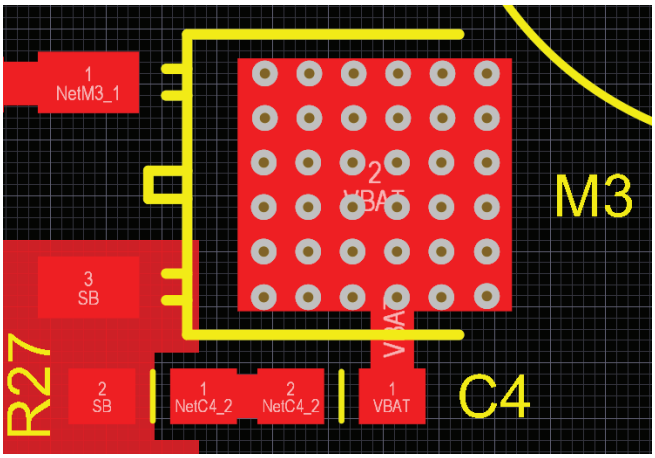


Figure 14: Snubber network, R27 and C4

BUCK REGULATOR

Some Allegro gate drivers have built-in buck regulator circuitry to allow the gate driver to operate using a 48 V battery supply. The buck regulator shown in Figure 15 is a step-down converter that converts the high V_{BB} voltage down to the V_{REG} voltage level, typically 12.5 V, operating at a fixed frequency of 410 kHz. When the transistor (DMOS) is turned on, the diode (D_{BUCK}) is reverse biased and voltage $V_{BB} – V_{REG}$ is impressed across the inductor (L_{BUCK}), causing a linear rise in current. When the transistor is turned off, the inductor current is diverted through the freewheel diode. Reverse voltage V_{REG} is then impressed across the inductor, causing a linear decrease in current. Buck regulator operation is typically formed with three loops—the input, output, and hot loops—as illustrated in Figure 15.

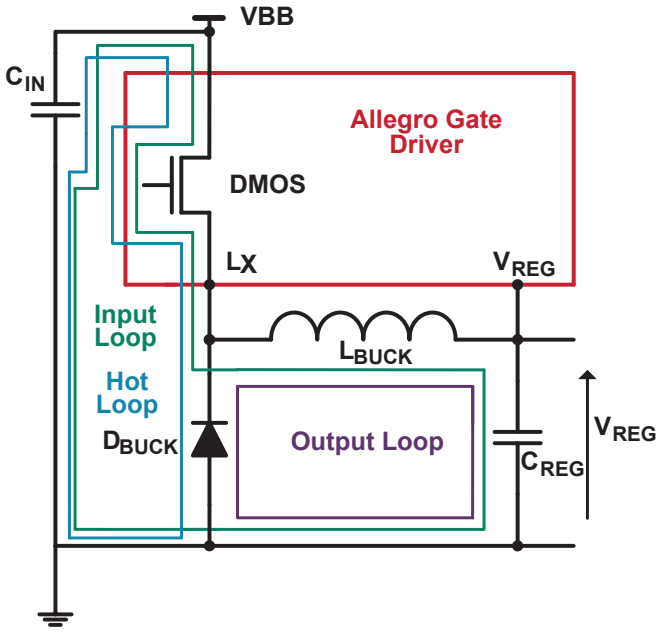


Figure 15: Simplified block diagram of the buck regulator

The input loop is formed when the transistor is turned on. During this time, the forward current flows from the input capacitor, C_{IN} (typically, the V_{BB} supply decoupling capacitor), through the transistor switch, through the inductor, through the output capacitor, C_{REG}, and back to the input capacitor, C_{IN}. The output loop is formed while the transistor switch is turned off. During this cycle, the forward current flows from the inductor to the output capacitor, C_{REG}, and returns from the output capacitor, C_{REG}, through the diode and back to the inductor.

The input, output, and hot loops are more critical connections in a buck regulator. These paths should take priority over all others during layout. The routing of the components that form the input, output, and hot loops need to be routed with short and low-inductance traces. The current path of the input loop should match the current path of the output loop, and the areas of the input and output loops should be minimized as much as practicable to reduce any unwanted electromagnetic interference.

The output switch of the buck regulator is typically called the switch node (L_X terminal) and is part of both the input and output loops, as shown in Figure 15. This node can carry fast-switching, high-amplitude voltage ringing (dV/dt) together with high peak currents. The connection of the switch node should be as short as practicable, low in inductance, and wide enough to allow the current to flow through it. Widening the connection of the switch node to compensate for a longer-distance trace is not recommended because the likelihood of the switch node connection becoming an antenna and radiating electromagnetic interference may be directly linked to its trace length.

Another point to consider when laying out the components for the buck regulator is the dI/dt loop. The dI/dt loop is known as the output loop, as shown in Figure 15. The output loop is one of the problematic paths for the buck regulator. The output loop has a very fast charging current, more so when the cathode of the diode (D_{BUCK}) is connected to the switch node (L_X terminal). This part of the output loop transitions from zero to full current very quickly when the transistor (DMOS) is turned off. Thus, keeping the output loop as small as practicable can result in minimizing any unwanted electromagnetic interference.

Extra care should be taken during layout of the hot loop, as presented in Figure 15. The hot loop, which has a current path with the highest dI/dt, is the loop that generally requires minimization with attention to routing of the tracks. The input capacitor, C_{IN}, and the transistor (DMOS) undergo a much larger dI/dt when the transistor is closed. The current transitions from zero current to very high current through the inductor (L_{BUCK}), then follows the inductor current on the upward rise until the transistor (DMOS) is opened, at which point the current rapidly falls back to zero. Thus, the loop creating the most electromagnetic interference is the hot loop involving the input capacitor C_{IN}, transistor (DMOS), and diode (D_{BUCK}).

THERMAL VIAS

Allegro gate drivers are offered in multiterminal packages, from a choice of wettable-flank quad-flat no-lead (QFN) packages, quad-flat packages (QFPs), or thin-shrink small-outline packages (TSSOPs) with exposed thermal pads on the bottom of the device. The thermal pad creates a low-impedance thermal path between

the die and the exterior of the package and provides excellent heat dissipation from the device to the PCB. In the PCB, thermal vias are typically used to conduct heat away from the device and to transfer heat from the top copper layer of the PCB to the inner copper layers or bottom copper layer, or to the outside environment, and thermal vias are typically arranged in arrays, as shown in Figure 16, top. Placement of via holes underneath the exposed thermal pad of the device is recommended because the PCB acts as a heat sink by mainly using the ground plane for the improved thermal power dissipation. A matrix of 16 thermal pad vias formed by four rows and four columns under an Allegro U1 device is shown in Figure 16, bottom.

The via matrix of the exposed 48-pin QFP U1 (Allegro AMT49106 [1]) device thermal pad was estimated by taking into consideration the exposed thermal pad area (5 mm × 5 mm) of the Allegro U1 device and the via pitch (1.2 mm). The matrix can be expressed as:

Equation 1:

$$\text{Via Matrix,U1} = [(5 \times 5)/(1.2 \times 1.2)] = 17.3611$$

To achieve better power dissipation, use of thermal vias is also recommended under and around the MOSFET drain and source pads. This concept is illustrated in Figure 16, bottom, which shows a matrix of 25 thermal pad vias created by five rows and five columns under the drains of the M3 and M4 MOSFET pads. Following the approach presented in Equation 1 for estimating the via matrix, the via matrix for MOSFETs M3 and M4 (D-Pak TO-252AA package) was selected by considering the area of the exposed thermal pad (5.7 mm × 6.2 mm) of MOSFETs M3 and M4 and the via pitch (1.2 mm). The matrix can be estimated as:

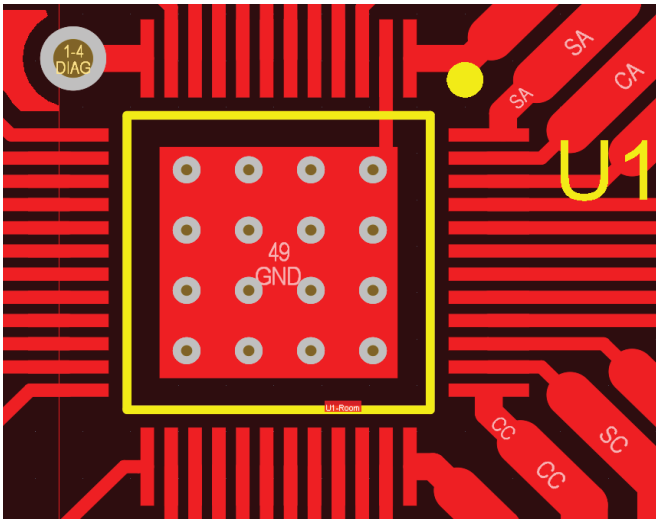
Equation 2:

$$\text{Via Matrix,M3 and M4} = [(5.97 \times 6.35)/(1.2 \times 1.2)] = 26.326$$

From Equation 1 and Equation 2, the thermal via matrices were selected to be 16 for the Allegro U1 device and 25 for MOSFETs M3 and M4, as presented in Figure 16, top and bottom, respectively. However, the matrix of thermal vias varies depending on the application and customer requirements, and the number of thermal vias depends on the amount of heat that must be moved away from the device package. The thermal via diameters and pitch sizes are shown in Figure 16 for the Allegro U1 device (top) and M3 and M4 (bottom).

To ensure adequate power dissipation of the device in the system, the parameters of the thermal pad vias should be selected according to the EIA/JEDEC standard (JESD51-5). To avoid any unwanted electromagnetic interference, the minimum via plating thickness used should be 0.025 mm throughout the via barrel. The decision to use thermal vias should depend on the application and customer requirements and should be avoided if adequate heat-sinking can be obtained by other means. The field of clearance holes can result in increased current density in the power and ground planes and, therefore, the total loop inductance of the power distribution network.

U1 Thermal Pad Vias



M3 and M4 Thermal Pad Vias

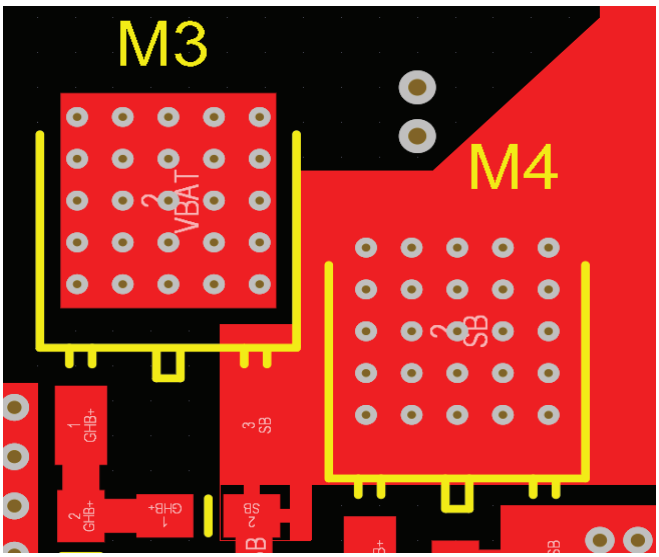


Figure 16: Thermal pad vias: U1 (top) and M3 and M4 (bottom)

Table 1: Thermal Pad Via Sizing

Parameters	U1	M3 and M4	JESD51-5
Isolation Clearance Diameter [mm]	0.6	0.6	Not less than 0.6
Via Diameter [mm]	0.25	0.25	0.3 ± 0.08
Pitch [mm]	1.2	1.2	1 to 1.3

[1] See https://www.allegromicro.com/en/products/motor-drivers/bldc-drivers/amt49106-amt49107

PCB VIA STITCHING AND SHIELDING

PCB via stitching is a method used to tie together larger copper areas on different layers, in effect creating a strong vertical connection through the PCB structure, which helps to maintain a low impedance and short return loops. While PCB via shielding has a different function, via shielding is used in gate driver applications to help reduce crosstalk and electromagnetic interference in a route that is carrying a high-frequency signal. A via shield, also known as a via fence or a picket fence, is created by placing one or more rows of vias alongside the signal route path. It is not recommended to have many via stitches or shields placed closely to one another. Closely placed via stitches or shields can cause large cuts in the power or ground plane and can create a current loop around the vias, as shown for via stitching in the example in Figure 17, top. An example of the correct via stitching placement that avoids a cut in the power plane and avoids current loop creation around the via stitching on the power plane is shown in Figure 17, bottom.

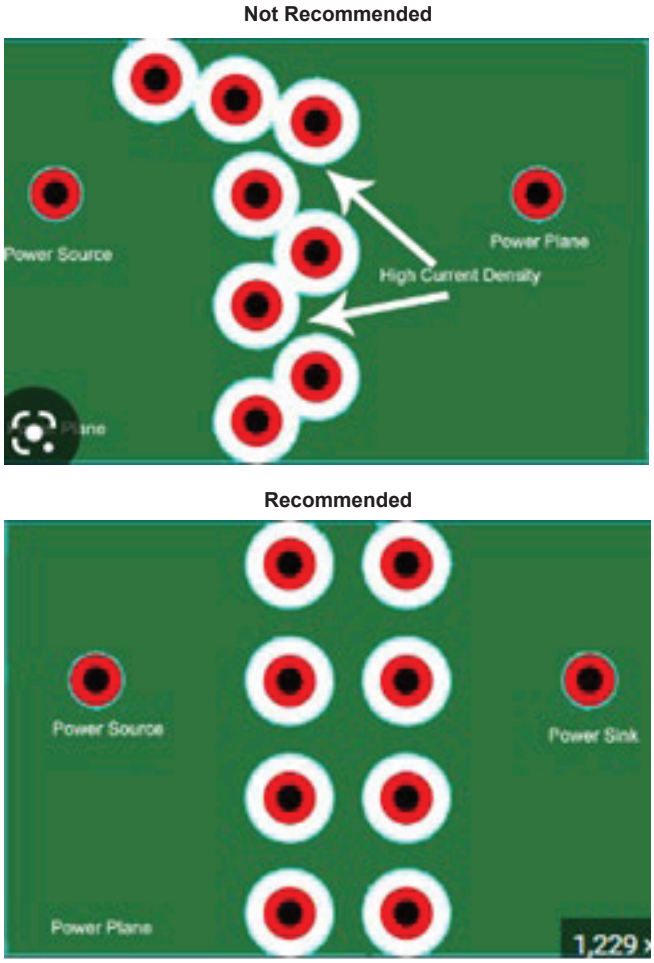


Figure 17: Via stitching placement

SUMMARY

Correct PCB layout is extremely important for motor gate driver designs that require high frequency, fast switching, high currents, and sensitive control signals. Increased power losses, output ripple, electromagnetic interference emissions, and inaccurate gate driver performance are direct consequences of an improper layout. To achieve high-performance solutions for motor gate driver applications, the guidelines provided in this application note should be considered.

Revision History

Number	Date	Description	Responsibility
–	December 23, 2022	Initial release	Dr. K. Tshiloz
1	January 30, 2026	Publish to website with minor editorial changes throughout	Dr. K. Tshiloz