



DESIGN OF TRANSFORMERS FOR USE WITH AHV85000 + AHV85040 CHIP SET

Dermot Dobbyn, Senior Applications Engineer
Allegro MicroSystems

ABSTRACT

This application note describes how to design a transformer for use with the AHV85000 + AHV85040 isolated gate drive chip set.

INTRODUCTION

The AHV85000 + AHV85040 is a cost-optimized isolated gate drive chip set for gallium-nitride (GaN) field-effect-transistor (FET) devices. When combined with an external transformer, it provides a self-powered isolated gate drive solution that is ideal for GaN FETs in multiple applications and topologies.

The chip set transmits both the pulse-width-modulated (PWM) signal and the gate bias power through the external transformer, eliminating the need for any external gate drive auxiliary bias supply or high-side bootstrap. This greatly simplifies the system design and reduces electromagnetic interference (EMI) through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch at any location in a switching-power topology.

The AHV85000 + AHV85040 chip set forms the primary-side transmitter (TX) and secondary-side receiver (RX) for an isolated GaN FET gate driver. The chip set relies on an external transformer, connected between the TX and RX ICs, to achieve isolated transmission of both the PWM

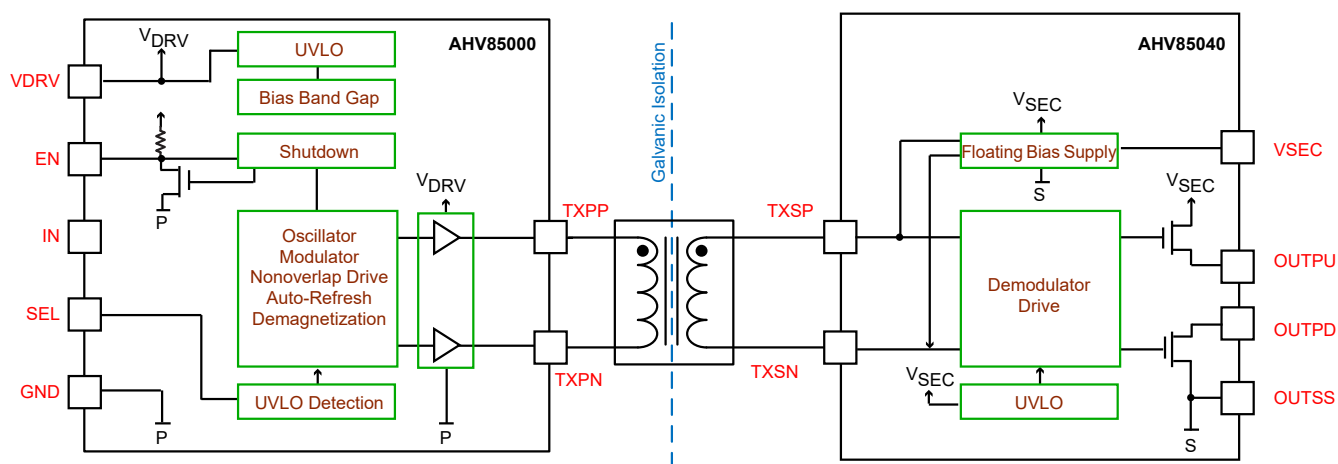


Figure 1: Block Diagram

signal and the gate bias power to the secondary side. The required transformer consists of a simple two-winding, four-pin structure—a primary-referenced TX winding and a secondary-referenced RX winding.

Expert designers can choose to use a custom transformer design of their own.

This application note describes the key transformer parameters that must be maintained to ensure compatibility with the AHV85000 + AHV85040 chip set. Also described are operation of the AHV85000 + AHV85040 chip set and how to verify that the transformer is operating correctly.

This application note describes only the electrical and magnetic design of the transformer. It does not discuss the isolation requirements and design because these factors are system dependent and are beyond the scope of the electrical design. End users can choose a transformer based on their isolation needs. This gives maximum flexibility, allowing for reinforced isolation for higher voltages or basic isolation where needed, which is unique to the AHV85000 + AHV85040 chip set solution.

OPERATION OVERVIEW

The AHV85000 primary-side IC delivers PWM and gate bias power, V_{SEC} , by driving the external transformer. The AHV85040 secondary-side IC decodes the transformer output into a PWM signal to drive the OUTPU and OUTPD pins

and bias supply to form V_{SEC} voltage. An external decoupling capacitor, C_{SEC} , is required from V_{SEC} to OUTSS. This should be located as close as practical to the device.

The principle operating waveforms relative to the input PWM IN signal are detailed in Figure 2. The primary-side TXPP drive is activated upon every rising edge of the input IN signal with the TXPN drive held low. Upon every falling edge of the input IN signal, the TXPN drive is activated and the TXPP drive is held low. This operation occurs regardless of the input frequency.

In cases where the IN PWM signal frequency is low or where IN is set to continuous 1 or 0, the AHV85000 implements an internal clock of $12\ \mu\text{s}$ ($T_{REFRESH}$) in order to prevent V_{SEC} voltage decay. When $T_{REFRESH}$ elapses, the driver recharges the V_{SEC} rail to maintain the output voltage. This condition persists until IN changes states.

The isolated V_{SEC} bias rail on the secondary is a derived open-loop from the primary 12 V supply, V_{DRV} . Because losses occur across the transformer, it is important to adhere to the limits of the transformer parameters listed in the Transformer Parameters section across the entire operating range, supply voltage, and temperature of the system.

The V_{SEC} rail level regulates quite well versus the PWM switching frequency, F_{SW} , at the IN pin, for a given fixed V_{DRV} level, and for a fixed-load, C_{LOAD} , at the OUTx drive pins (the load presented by the gate of the GaN FET being driven).

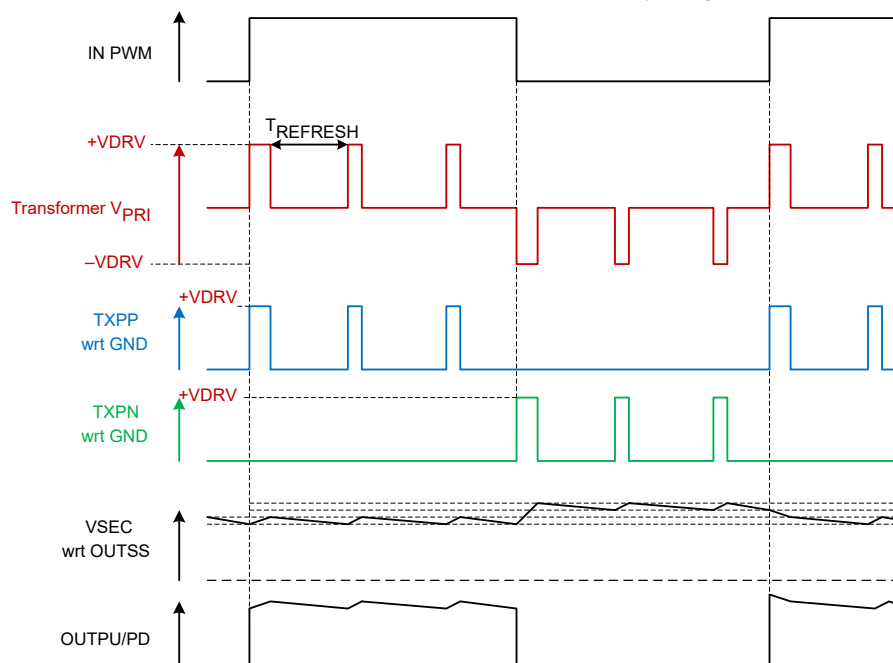


Figure 2: Principle Operating Waveforms

This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the FET gate, so there is a good charge balance across a wide frequency range.

However, the V_{SEC} rail varies with the effective loading of the gate of the FET being driven; as the V_{SEC} level falls, more charge is available to be delivered to the secondary side while the charge consumed by the FET gate decreases with the falling V_{SEC} level. Therefore, the V_{SEC} rail droops as far as needed until the charge delivered matches the charge consumed. For this reason, it is also very important to minimize the amount of charge diverted into any external load(s). For example, an external circuit with very low bias power can be powered using V_{SEC} ; however, to minimize the charge diverted away from the gate of the FET, the consumption should be minimal. Similarly, if a gate-source pull-down resistor is desired on the load FET (to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible.

BIPOLAR OUTPUT DRIVE

For systems such as enhancement mode GaN FETs, which require a regulated positive gate-source voltage, a bipolar output can be added as shown in Figure 3.

The total secondary-side bias voltage, V_{SEC} , is primarily a function of V_{DRV} . The Zener diode clamps the amplitude of the positive V_{GS} swing during the on-time, and the balance

of the V_{SEC} voltage appears as a negative V_{GS} during the off-time.

For example, if $V_{DRV} = 11$ V, which then generates $V_{SEC} = 8$ V, the positive V_{GS} with $V_Z = 5.6$ V is:

$$V_{GS_POS} = V_Z = 5.6 \text{ V}$$

$$|V_{GS_NEG}| = |V_{SEC} - V_Z| = 2.4 \text{ V}$$

If V_{DRV} is then increased to 12 V, V_{SEC} increases to approximately 9 V. V_{GS_POS} remains regulated at 5.6 V while $|V_{GS_NEG}|$ increases to 3.4 V.

This circuit can also provide protection in the event of a false turn-on caused by parasitic circuit components. For full details, see the application note “FET Gate Drive and Bipolar Output Applicable to AHV85110 Gate Drivers” (AN296268).^[1]

INCREASING V_{SEC}

When a 1:1 turns-ratio transformer is used, the total secondary-side bias voltage, V_{SEC} , is always less than the primary-side supply voltage, V_{DRV} , due to internal losses and losses in the transformer. For systems that require a higher V_{SEC} level and, hence, a higher gate-drive voltage level, such as cascode GaN FETs, the turns-ratio of the transformer can be increased.

In this case, it is important to adhere to the recommended maximum operating conditions of the AHV85040 IC listed in the [datasheet](#).^[2]

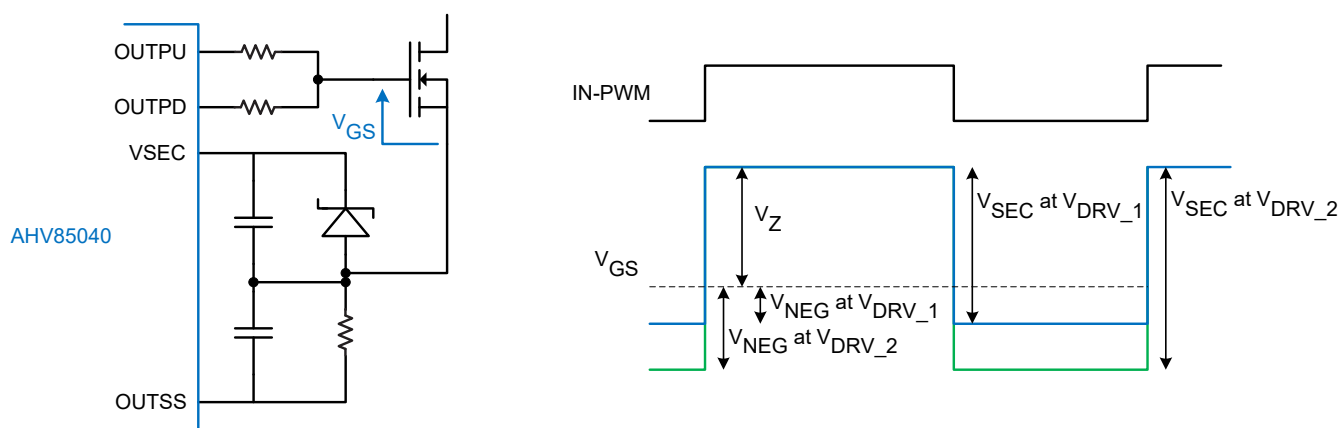


Figure 3: Bipolar Circuit

^[1] https://www.allegromicro.com/-/media/files/application-notes/an296268-fet-gate-drive-and-bipolar-output.pdf?sc_lang=en

^[2] https://www.allegromicro.com/-/media/files/datasheets/ahv85000-ahv85040-datasheet.pdf?sc_lang=en

OPERATING FREQUENCY AND THERMAL DERATING

The maximum recommended PWM frequency is 1 MHz. However, the internal dissipation of the device, application PCB layout, and ambient temperature must also be taken into account to ensure that the internal recommended $T_{J(MAX)}$ of 125°C is not exceeded.

TRANSFORMER DESIGN

Transformer Parameters

The acceptable ranges of key transformer parameters that must be maintained to ensure compatibility with the AHV85000 + AHV85040 chip set are listed in Table 1.

Table 1: Transformer Parameters

Transformer Parameter	Symbol	Min.	Nom.	Max.	Units
Primary Magnetising Inductance	L_{MAG}	5	6	7	μH
Leakage Inductance	L_{LK}	—	600	700	nH
Volt-Seconds	$V \cdot s$	2.5	4	—	$V \times \mu s$
Primary Resistance	DCR_{PRI}	—	1	1.2	Ω
Secondary Resistance	DCR_{SEC}	—	1	1.2	Ω
Turns Ratio	N_P/N_S	—	1:1	—	—
Frequency	F	—	0.4	1 [1]	MHz

[1] The maximum operating frequency can be limited by the thermal performance of the design.

Table 2: Required Transformer Connections

Transformer Connection	AHV85000 Pin	AHV85040 Pin
Primary Start	TXPP	—
Primary End	TXPN	—
Secondary Start	—	TXSP
Secondary End	—	TXSN

Design Example

- Selected core—Würth Elektronik part number 150-3987:
 - $A_{E_MIN} = 1.93 \text{ mm}^2$
 - $A_L = 250 \text{ nH/T}^2$
 - B_{SAT} at 100°C = 400 mT
- Calculate primary turns:
 - $N = \sqrt{(L_{MAG}/A_L)} = \sqrt{(6\mu/250 \text{ nH})} = 4.9$; round to 5T
- Check volt-seconds (V·s):
 - Assume maximum flux density at maximum temperature of 300 mT
 - $V \cdot s = B_{MAX} N A_{E_MIN} = 0.3 \times 5 \times 1.93 \times 10^{-6} = 2.98 \text{ V}\mu s$

Measurements

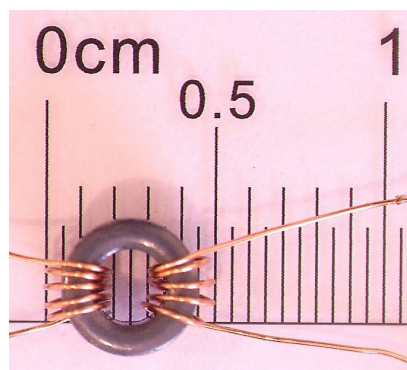


Table 3: Design Example—5T:5T 0.15 mm² Wire

Parameter	Test Conditions [1]	Value	Units
Magnetizing Inductance	100 kHz, 1 V rms	6.5	μH
Leakage Inductance	Short-circuit secondary Measure primary 100 kHz, 1 V rms	320	nH
DC Resistance	at 20°C	75	m Ω

[1] Measured with Fluke PM6304 LCR meter.

CHECK SATURATION LEVEL

The saturation level of the transformer can be checked with the circuit shown in Figure 4.

Monitor the primary magnetizing current while applying DC voltage, V_{DC} , to the transformer. Starting with a narrow pulse, increase the pulse width until the magnetizing current changes from linear to tailing up. This is the onset of saturation.

Because the maximum flux density varies with temperature, it is important to check the saturation level over the entire operating range of the transformer.

The measurement of the design example transformer is shown in Figure 4. The onset of saturation can be observed

at an applied DC voltage of 20 V and a duration of 150 ns. This is equivalent to 3 V·s, which is within the operating limits of the AHV85000 + AHV85040 chip set.

The reference trace in orange is the measurement at a temperature of 120 °C, which has a volt-seconds value of 2.75 V·s.

TYPICAL CIRCUIT MEASUREMENTS

A typical test circuit using the AHV85000 + AHV85040 chip set is shown in Figure 5. This circuit uses:

- A fixed 1 nF capacitor load to emulate a GaN FET
- The transformer described in the Design Example section.

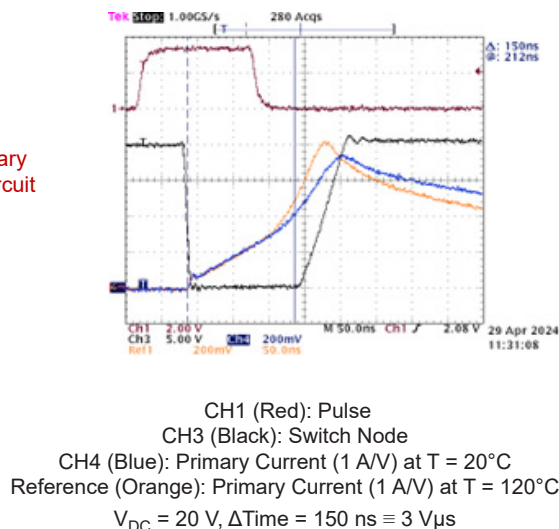
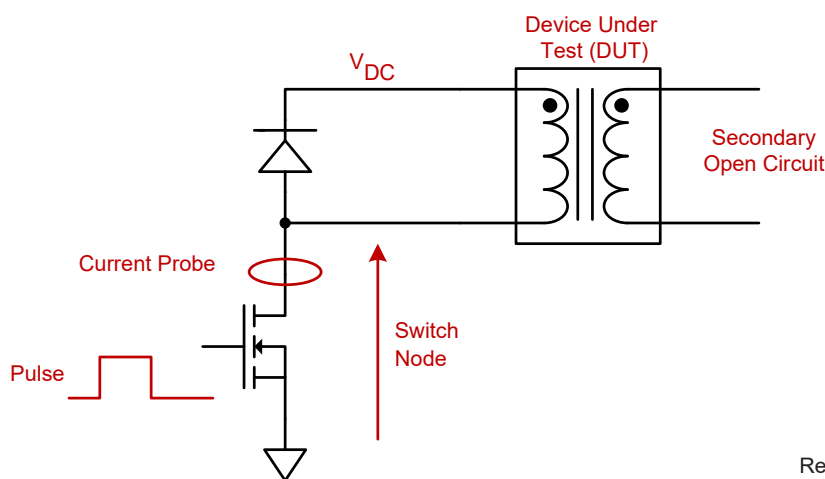


Figure 4: Saturation Test Circuit and Test Result

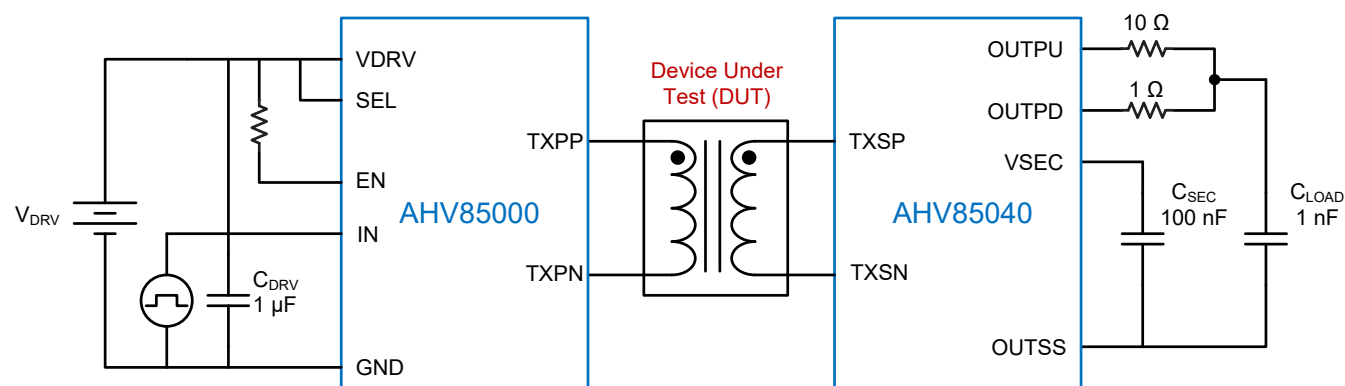


Figure 5: Typical Test Circuit

SECONDARY BIAS SUPPLY

The secondary-side bias voltage, V_{SEC} , is measured versus the frequency of the input IN signal. This measurement (see Figure 6) shows the same primary with two different turns-ratios—5T:5T and 5T:6T. The effect of the increased turns-ratio can be clearly observed.

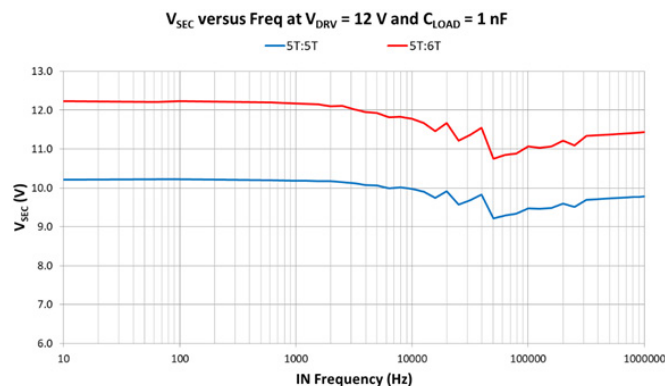


Figure 6: Secondary-Side Bias Voltage versus Frequency

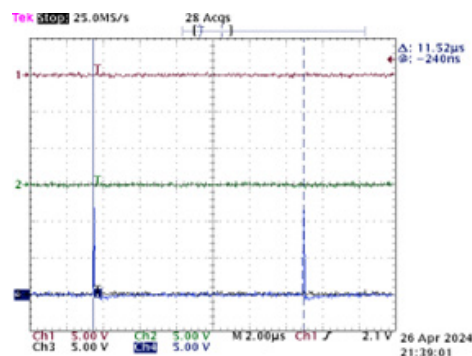
TYPICAL CIRCUIT WAVEFORMS

The waveforms presented in this section were recorded using the test circuit of Figure 5 and the transformer designed as previously described in the design example.

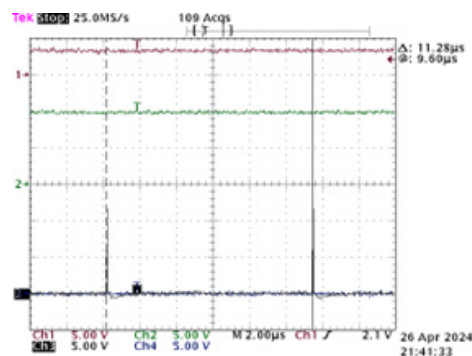
Typical waveforms when IN is fixed low, fixed high, or fixed at 100 kHz are shown in Figure 7. When IN is:

- Fixed low (DC = 0; top plot), the secondary-side bias voltage is generated from refresh pulses applied to TXPN, as described in the Operation Overview section. The refresh period measured for this example is 11.52 μs . It should be noted that the AHV85000 applies dithering to the refresh period. Hence, the refresh pulses jitter in time by, typically, $\pm 0.5\text{ }\mu\text{s}$.
- Fixed high (center plot), V_{SEC} is generated from TXPP pulses and dithering is again visible. Notice that the output, V_{GATE} , is fixed high at a level equal to V_{SEC} .
- 100 kHz with 50% duty cycle (bottom plot), the output, V_{GATE} , has a TXPP pulse that occurs at the rising edge of the input IN signal and a TXPN pulse that occurs at the falling edge of the input IN signal. Given that the duration of the high and low portions of the input IN signal are less than the refresh period, refresh pulses are not necessary to maintain V_{SEC} .

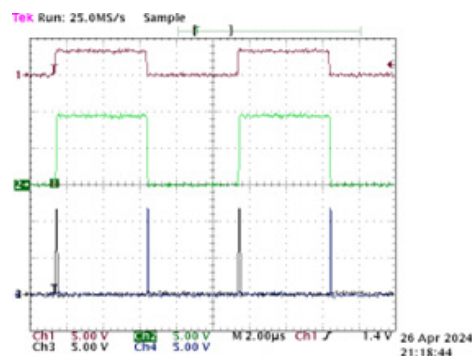
Zooms of the plots of the TXPP and TXPN signals are shown in Figure 8, which also shows the typical propagation delay



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Primary TXPN
 $V_{DRV} = 12\text{ V}$, IN = 0

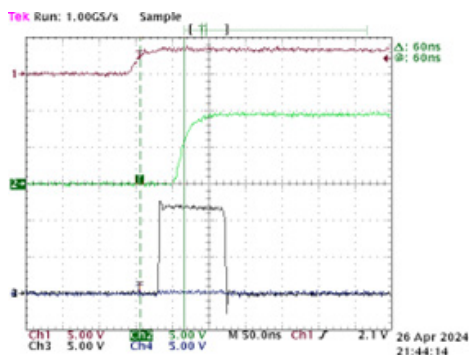


CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Primary TXPN
 $V_{DRV} = 12\text{ V}$, IN = 3.3 V

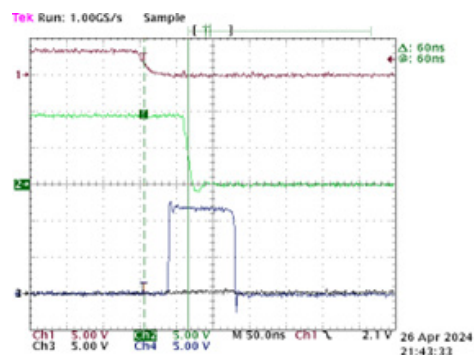


CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Primary TXPN
 $V_{DRV} = 12\text{ V}$, IN = 100 kHz

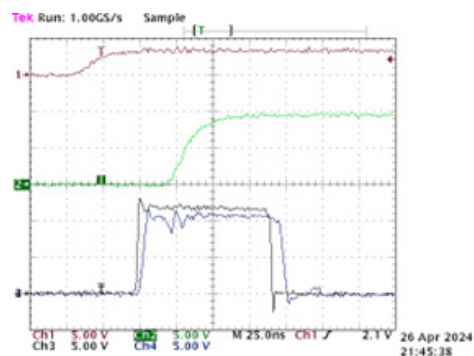
Figure 7: Typical Primary Waveforms



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Primary TXPN
 $V_{DRV} = 12\text{ V}$, $IN = 100\text{ kHz}$



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Primary TXPN
 $V_{DRV} = 12\text{ V}$, $IN = 100\text{ kHz}$



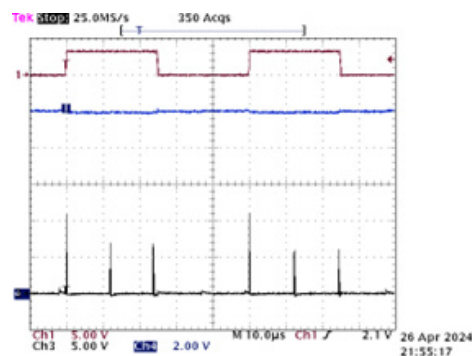
CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
CH3 (Black): Primary TXPP
CH4 (Blue): Secondary TXSP
 $V_{DRV} = 12\text{ V}$, $IN = 100\text{ kHz}$

Figure 8: Zoom of TXPP and TXPN Signals

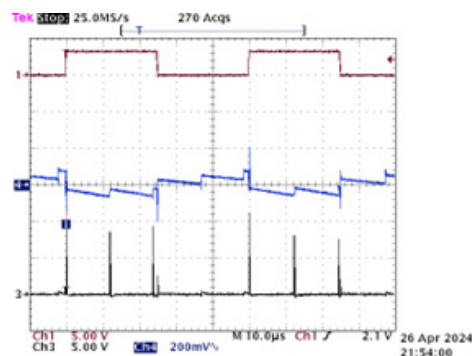
from IN to V_{GATE} . The secondary-side transformer waveform, TXSP, is also shown in Figure 8, bottom, in relation to the primary-side TXPP. The resulting falling edge of the IN signal shows similar TXPN and TXSN signals.

In cases where the period of the IN signal is longer than the refresh period, V_{SEC} is supplemented with refresh pulses. This can be observed in Figure 9, where the IN frequency is 10 kHz—For clarity, the refresh pulses on the TXSN signal when IN is low are not shown. Also note that, due to the time scales involved, the oscilloscope capture of the TXSP signal exhibits aliasing: Its amplitude is the same as that shown in Figure 8.

Cases where V_{SEC} is DC-coupled/AC-coupled are shown in Figure 9, top/bottom, respectively. The ripple on V_{SEC} can be observed clearly. This ripple can be reduced, if necessary, by increasing the C_{SEC} decoupling capacitor at the expense of a slower start-up time.



CH1 (Red): IN—PWM
CH2 (Green): —
CH3 (Black): Secondary TXSP
CH4 (Blue): V_{SEC}
 $V_{DRV} = 12\text{ V}$, $IN = 10\text{ kHz}$

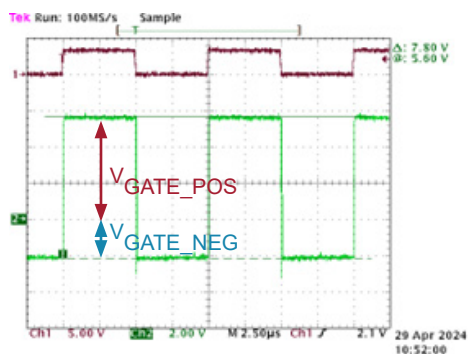


CH1 (Red): IN—PWM
CH2 (Green): —
CH3 (Black): Secondary TXSP
CH4 (Blue): V_{SEC} AC-coupled
 $V_{DRV} = 12\text{ V}$, $IN = 10\text{ kHz}$

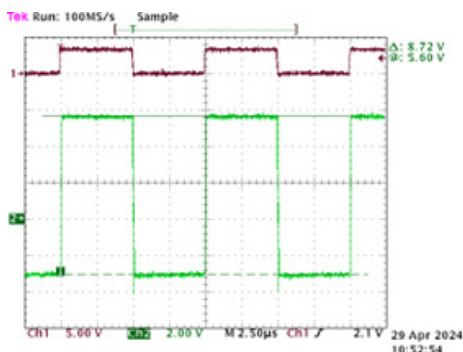
Figure 9: Typical V_{SEC} at $IN = 10\text{ kHz}$

BIPOLAR CIRCUIT

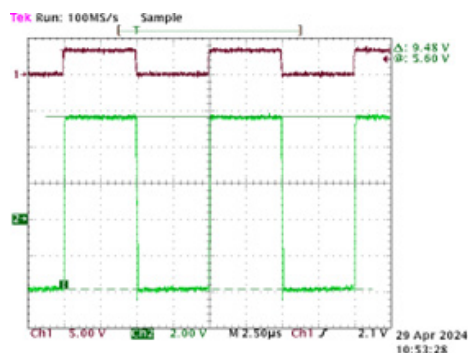
The test circuit of Figure 5 can be easily modified to include a bipolar output circuit as shown in Figure 3. With this circuit, using a 5.6 V Zener diode, the output V_{GATE} is as shown in Figure 10.



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
 $V_{DRV} = 10.5\text{ V}$, IN = 100 kHz



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
 $V_{DRV} = 12\text{ V}$, IN = 100 kHz



CH1 (Red): IN—PWM
CH2 (Green): V_{GATE}
 $V_{DRV} = 13.2\text{ V}$, IN = 100 kHz

Figure 10: Bipolar Circuit Output

The three plots in Figure 10 show the V_{GATE} output for three different V_{DRV} levels. It can be observed, as explained in the Bipolar Output Drive section, that the positive V_{GATE} voltage is regulated to the Zener diode, 5.6 V; and that, while the V_{DRV} supply increases, the negative V_{GATE} increases.

CONCLUSION

The AHV85000 + AHV85040 chip set offers the unique versatility of allowing an experienced user to design a transformer to optimize the performance, size, and cost of a system.

Custom transformer designs can also be optimized for enhancement-mode GaN FETs or cascode-mode GaN FETs by selecting the appropriate turns-ratio.

This application note has described the requirements of such a transformer and how it can be tested in an end application.

As noted, the performance must be considered in terms of the system as a whole. Therefore, it is critical to test the solution over the entire operating range of the system and to ensure that the AHV85000 and AHV85040 devices are used within their specified limits.

Revision History

Number	Date	Description	Responsibility
–	May 17, 2024	Initial release	D. Dobbyn

Copyright 2024, Allegro MicroSystems.

The information contained in this document does not constitute any representation, warranty, assurance, guaranty, or inducement by Allegro to the customer with respect to the subject matter of this document. The information being provided does not guarantee that a process based on this information will be reliable, or that Allegro has explored all of the possible failure modes. It is the customer's responsibility to do sufficient qualification testing of the final product to ensure that it is reliable and meets all design requirements.

Copies of this document are considered uncontrolled documents.