ALLEGRO APM81815 BUCK POWER MODULE FOR 48 V BUS: INSIGHTS ON POWER LOSS AND THERMAL PERFORMANCE

By Alessandro Dago, Luca Morinelli, and Samuel Locke
Allegro MicroSystems

INTRODUCTION

The transition from 12 volts to 48 volts for low-voltage rails in the automotive environment promises a reduction in distribution power losses, as well as lower weight and cost associated with reduced wiring. However, it would be impossible to take advantage of the aforementioned benefits without the use of dedicated power management devices compliant with the 48 V bus specifications.

The APM81815 is a regulated buck converter designed and optimized for 48 V automotive systems. Figure 1 shows an example application diagram using APM81815 as a pre-regulator for components not rated up to 48 V. APM81815 integrates 80 V power FETs, drivers, an average current-mode controller, and faults diagnostic on a single chip. This device is also a power module which includes the bootstrap capacitor and a high-frequency input capacitor in a single package for optimized EMI performance.

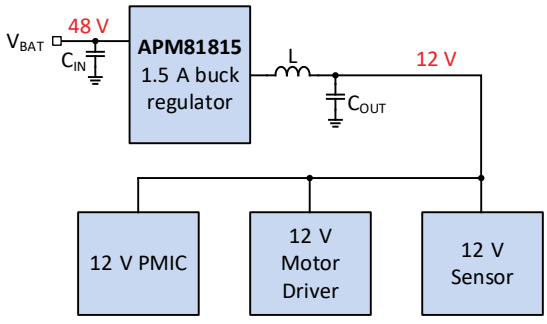

Figure 1: APM81815 application diagram for 48 V architecture.

The APM81815 operates at a 2.15 MHz switching frequency (f_{SW}); however, it can be reconfigured with an external resistor in the 400 kHz to 2.5 MHz range. In the definition of the device switching frequency, the designer shall take into consideration two main factors: 1) the inductor current ripple (dI_L) is inversely proportional to the inductance value (L) and to the switching frequency; 2) the switching losses are directly proportional to the switching frequency.

Equation 1:

$$dI_L = \frac{V_{IN}\,(1 - D)\,D}{f_{SW}\,L}$$

In Equation 1, the inductor current ripple as a function of the input voltage (V_{IN}) and the duty cycle ($D = V_{OUT} / V_{IN}$) is reported. As can be seen, the higher the switching frequency, the lower the inductance value required to get the same current ripple, with consequent reduction of the system size and cost. Unfortunately, as the frequency increases, the associated switching losses increase consequently.

Despite switching losses in this range of switching frequencies are not generally a problem for 12 V converters, they can become a dominant loss source for higher input voltages, and they must be taken into consideration for switching frequency definition to avoid thermal issues in the device. In this application note, a detailed analysis of the buck converter losses is conducted. Their impact on thermal performance of the APM81815 is then discussed and validated throughout measurement results on Allegro APM81815 evaluation board (EVB). Finally, a strategy for switching frequency and inductor selection is presented.

BUCK CONVERTER LOSSES

Conduction Losses

Conduction losses are the ohmic losses on the high-side (HS) and low-side (LS) FETs of the buck converter, respectively during t_{ON} and t_{OFF} conduction period, where $t_{ON} = D / f_{SW}$ and $t_{OFF} = (1 - D) / f_{SW}$. Their contribution can be evaluated simply calculating the route mean square (RMS) value of the high-side and low-side currents (shown in Figure 2), and then multiply it by the $R_{ds(on)}$ resistance of the corresponding FET.

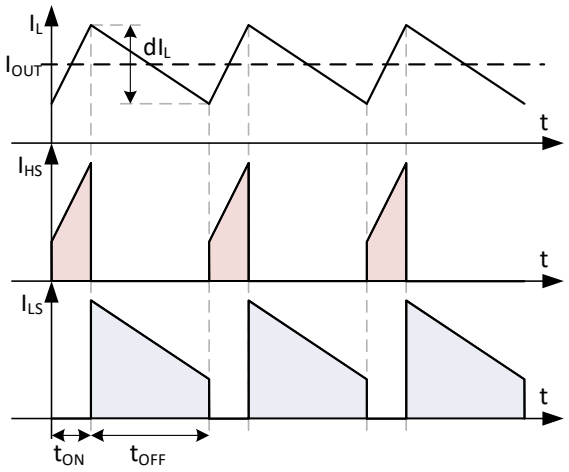

Figure 2: High-side and low-side FETs currents of a buck converter

Equation 2:

$$P_{cond(HS)} = R_{ds(on)HS} \times D \times I_{OUT}^2 \left(1 + \frac{1}{3}\left(\frac{dI_L}{2I_{OUT}}\right)^2\right)$$

Equation 3:

$$P_{cond(LS)} = R_{ds(on)LS} \times D \times I_{OUT}^2 \left(1 + \frac{1}{3}\left(\frac{dI_L}{2I_{OUT}}\right)^2\right)$$

In Equation 2 and Equation 3, the formulas for the high-side and low-side conduction losses are respectively reported.

C_{OSS} Losses

C_{OSS} losses are the losses caused by the charging and discharging of the switching node parasitic capacitance (mainly C_{OSS} capacitance of the high-side and low-side FETs) as reported in Figure 3. Note that, while the energy for the charging of the switching node is provided by the high-side FET channel, resulting in a power loss, the energy released during the discharging of the switching node flows to the output node, not corresponding to an energy loss.

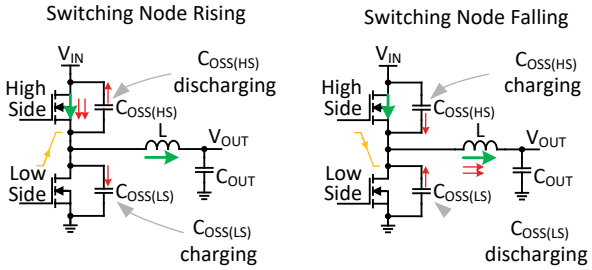

Figure 3: C_{OSS} charging and discharging mechanism

This power loss contribution can be evaluated with the following formula:

Equation 4:

$$P_{COSS} = \frac{1}{2}\left(C_{OSS(HS)} + C_{OSS(LS)}\right) \times V_{IN}^2 \times f_{SW}$$

Current-Voltage Overlap Losses

Current-voltage overlap losses are caused by simultaneous non-zero voltage and current across the high-side FET during the switching node transition.

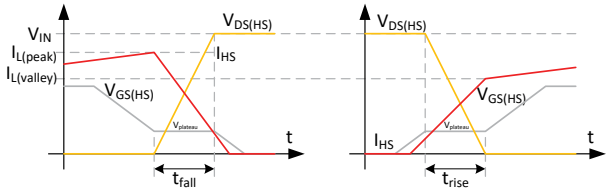

Figure 4: Falling and rising waveforms of the high-side FET in a buck converter

In Figure 4, the voltage and current waveforms on the high-side FET during switching node falling and rising edges are reported. The corresponding current-voltage overlap losses can be approximated with the triangle formula, distinguishing the case in which $I_{L(valley)} > 0$ ($I_{OUT} > dI_L / 2$) and the case in which $I_{L(valley)} < 0$ ($I_{OUT} < dI_L / 2$) as the APM81815 operates in CCM.

Equation 5:

$$P_{IV} = V_{IN}\left(I_{L(peak)}\, t_{rise} + I_{L(valley)}\, t_{fall}\right)\frac{f_{SW}}{6} \qquad I_{OUT} > \frac{dI_L}{2}$$

$$P_{IV} = V_{IN}\left(I_{L(peak)}\, t_{fall}\right)\frac{f_{SW}}{6} \qquad I_{OUT} < \frac{dI_L}{2}$$

where t_{rise} and t_{fall} can be calculated as a function of the switching node slew rate, which is controlled by the APM81815: $t_{rise} = SR_{rise} \times V_{IN}$ and $t_{fall} = SR_{fall} \times V_{IN}$.

Note that, because of EMI requirements, switching node slew

rate in 48 V systems is comparable to the one in 12 V systems, with consequent increase of t_{rise} and t_{fall} values. Since APM81815 integrates the high-frequency input capacitance in the package, the critical input loop is minimized, allowing to meet EMI requirements even with a higher switching node slew rate compared to traditional solutions, minimizing the impact of current-voltage overlap losses at high switching frequency.

Reverse Recovery Charge Losses

Reverse recovery charge losses are caused by the reverse recovery charge accumulated on the body diode of the low-side FET, and can be evaluated as:

Equation 6:

$$P_{QRR} = Q_{RR} \times V_{IN} \times f_{SW}$$

As can be observed in Equation 4, Equation 5, and Equation 6, all the switching losses terms are proportional to the switching frequency and to the input voltage, or the squared of it. Transitioning from a 12 V to a 48 V system, considering the same switching frequency and switching slew rate, the switching losses impact multiplies by a factor 4 for Equation 5 and Equation 6, and by a factor 16 for Equation 4.

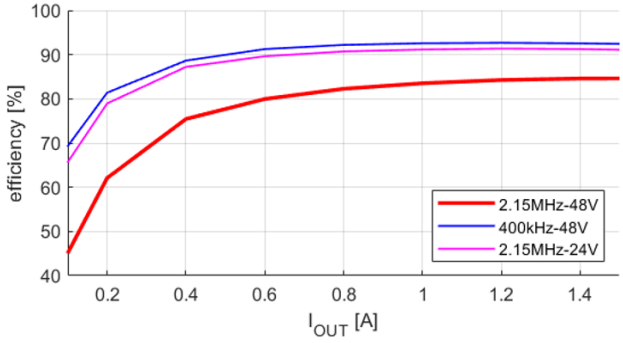

Figure 5: APM81815 measured efficiency curves dependency on switching frequency and input voltage, at T_A = 25°C and V_{OUT} = 12 V

In Figure 5, the effect of switching losses on conversion efficiency (and therefore on power losses), can be observed. As the switching frequency or the input voltage are reduced with respect to the 2.15 MHz 48 V condition, the conversion efficiency noticeably increases, as effect of reduced C_{OSS}, current-voltage overlap, and reverse recovery charge losses.

THERMAL BUDGET

The maximum allowable internal power dissipation is limited by the thermal conductivity of the device. The die is flip-chip assembled, which uses copper pillars instead of the traditional wire bond solution. This solution also allows for optimizing the thermal conductivity from the die to the PCB.

A traditional wire-bond approach (Figure 6a) conducts the heat through the die substrate, which thermal conductivity is roughly 100 W/mK. In Figure 6b, the MIS package cross-section of APM81815 is sketched. As can be seen, the thermal path from the active area (where the heat is generated) and the PCB (where the heat is dissipated) is uniquely composed of copper features, which thermal conductivity is roughly 400 W/mK. This allows the APM81815 to achieve higher thermal dissipation performance.

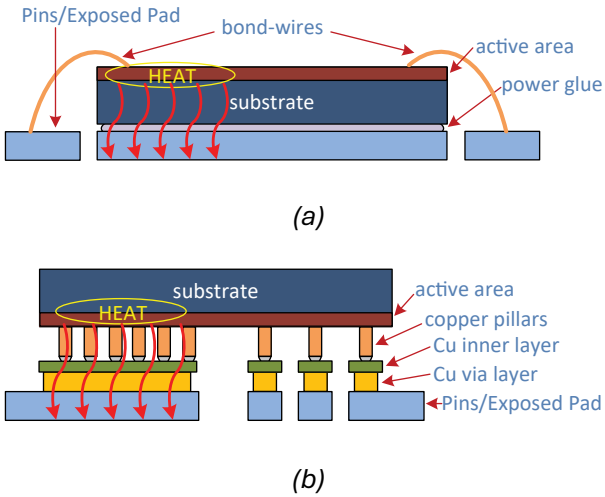

Figure 6: (a) Traditional QFN, and (b) Flip-Chip MIS package thermal flow diagram

The thermal performances of a device are analyzed by means of its junction-to-ambient thermal resistance ($R_{\theta JA}$). This parameter represents how much the device resists the flow of heat from the junction (where the heat is generated) to the surrounding ambient air. It can be used to determine the junction temperature (T_J) as a function of the ambient temperature (T_A) and the power dissipated inside the device ($P_{LOSS} = P_{cond(HS)} + P_{cond(LS)} + P_{COSS} + P_{IV} + P_{QRR}$).

Equation 7:

$$T_J = T_A + R_{\theta JA} \times P_{LOSS}$$

$R_{\theta JA}$ not only depends on the package, but also on the PCB layout on which the device is mounted. For this reason, the thermal performance of the APM81815 should be evaluated case-by-case on the final application board. Allegro APM81815 EVB is a 4-layer 50 mm x 60 mm PCB with 1-oz internal layers and 2-oz external layers, showing a measured $R_{\theta JA}$ = 33°C/W. As a rule of thumb, $R_{\theta JA}$ can be reduced by increasing the number of layers (improving the lateral heat transfer), increasing the number of vias (improving the heat transfer to the bottom of the board), and increase the exposed copper area (improving the PCB to ambient heat transfer).

To get a clear estimation of the final application $R_{\theta JA}$ value, different solutions exist.

Design Phase

PCB layout thermal simulations can be conducted to get an initial estimation of the expected performance and optimize the PCB layout to improve the heat dissipation.

Evaluation Phase

The internal junction temperature T_J of the device can be measured after an ESD diode characterization when the device is off and mounted on the application board. As an example, APM81815's SYNC pin to GND ESD diode forward voltage can be characterized in a thermal chamber initially by applying a small forward current from GND to SYNC pin (1 mA is sufficient), then, measuring its forward voltage by varying the ambient temperature T_A (which corresponds to T_J when the device is off). Following the ESD diode characterization, the device shall be heated up by dissipating some power (P_{LOSS}) internally—for example, applying a 1 A forward current to the high-side FET body diode, located between SW to VIN pins. When in this condition, T_J is derived measuring the ESD diode forward voltage, T_A is externally controlled in the thermal chamber, $P_{LOSS} = I_{SW} \times (V_{SW} - V_{VIN})$, and so, $R_{\theta JA}$ is derived as:

Equation 8:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{LOSS}}$$

APM81815's performances are guaranteed up to a maximum T_J of 150°C; above this limit, its performance degrades, or it sustains permanent damage. To protect the device, a junction temperature sensor is integrated into the device—if the junction temperature rises above 175°C (typical) the device stops switching (thermal shutdown (TSD)); it recovers if T_J falls below 155°C (typical).

MEASURED PERFORMANCE

The Allegro APM81815 shows best in class performance when compared to alternative 48 V buck converter products available on the market.

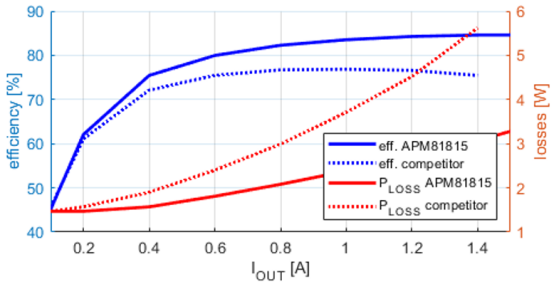

Figure 7: 48 to 12 V conversion efficiency and related power losses, measured on APM81815 and a competitor device, at 25°C ambient temperature, at 2.15 MHz switching frequency, with the same 4.7 µH inductance

Figure 7 shows conversion efficiency and related power losses, for 48 V to 12 V conversion at 2.15 MHz, measured on APM81815 and a competitor product. As can be seen, APM81815 presents lower power losses and higher efficiency. As a comparison, APM81815 losses at 1 A load corresponds to 2.4 W, while competitor device dissipates a total of 3.7 W. In this operating condition, the selected inductor (Wurth Elektronik 784778047) is responsible for roughly 0.22 W. From Equation 7, it can be obtained that, considering for both devices a 175°C TSD threshold and $R_{\theta JA}$ = 33°C/W, the maximum ambient temperature the devices can sustain are 103°C and 60°C for APM81815 and competitor device, respectively.

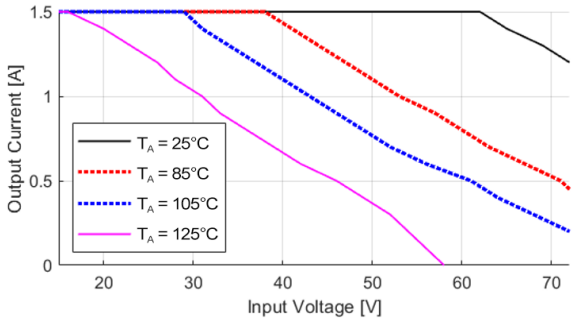

Figure 8: APM81815 EVB input voltage / output current operating boundaries at f_{SW} = 2.15 MHz, limited by TSD of the device

APM81815 ensures full input voltage (up to 72 V) and output current (up to 1.5 A) operation below TSD when operated at f_{SW} = 400 kHz, up to 125°C ambient temperature. However, when operating at f_{SW} = 2.15 MHz, the effect of the increased switching losses in Equation 4, Equation 5, and Equation 6, causes the junction temperature in Equation 7 to reach TSD limit in certain input voltage/output current/ambient temperature conditions. In Figure 8, the APM81815 EVB's operating boundaries measured at 2.15 MHz are reported. For each ambient temperature line, the device triggers TSD if the output current or input voltage are higher than the boundary line (top right corner of the graph). Below these boundaries, the junction temperature is therefore ensured to be lower than 175°C.

Design Considerations

When using the APM81815 in a design, thermal behavior and device performance can be predicted with the aid of the design tool.

First, maximum output current, input voltage, and ambient temperature must be identified.

Variables	Min	Typ	Max	Unit
Ambient Temperature	–	–	85	°C
Operating Input Voltage	20	48	60	V
Output Voltage	–	–	12	V
Load Current	–	–	0.8	A

Then, the corresponding total power dissipated inside the device is calculated.

Variables	Min	Typ	Max	Unit
Total IC Power Loss	0.5888	1.6646	2.2106	W
Total Power Loss	0.7654	2.0516	2.6384	W
Maximum Junction Temperature	104.4317	139.9302	157.9487	°C

For reliable device operation, the customer shall guarantee that the typical value of junction temperature does not exceed 150°C. Moreover, the maximum value of the junction temperature shall be lower than the TSD threshold.

In the example, both thermal constraints are met, which means the device can be used at 2.15 MHz switching frequency. In this case, a 4.7 µH or a 6.8 µH inductor is suggested.

In case the typical value of the junction temperature results higher than 150°C, or the maximum value results higher than TSD, operation at lower switching frequency is suggested. Choosing 400 kHz switching frequency relaxes the junction temperature and makes the APM81815 usable in every input voltage/output current/ambient temperature condition (T_A < 125°C). However, a higher inductor value of at least 22 µH is required.

CONCLUSION

In this application note, the main issues related to power conversion in 48 V systems have been analyzed. While reducing the distribution current by a factor of 4 with respect to 12 V bus, conversion efficiency in switching regulators is strongly impacted by increased switching losses. As a main consequence in integrated power converters, the heat generated in the switching devices causes the junction temperature to increase, eventually above junction temperature rating or TSD threshold, causing shutdown of the device.

The Allegro APM81815 is a buck converter for 48 V automotive bus with EMI optimized design and best in class performance. The MIS package integrates the input capacitance to minimize the critical loop, moreover, the frequency dithering option allows to further reduce the EMI. Thanks to the implemented techniques, the SW node slew rate can be increased, with consequent reduction of switching losses. When compared with alternative devices, APM81815 shows higher conversion efficiency and lower power dissipation. With some limitations in maximum ambient temperature, input voltage, and output current, this device can be used at a switching frequency above the AM band, which allows to reduce the size of the coil, and therefore, the PCB footprint.

Revision History

Number	Date	Description
–	May 21, 2025	Initial release

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM