ADVANCED NEGATIVE VOLTAGE TRANSIENT TEST FOR GATE DRIVERS IN AUTOMOTIVE APPLICATIONS

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ABSTRACT

In automotive applications, negative voltage greatly impacts the gate drivers. This is especially true at the high-side and low-side source terminals of the gate driver, which are typically connected to the motor load. This application note investigates the sensitivity of the gate driver when exposed to transient negative voltage conditions using tests of the Allegro AMT49100 48 V gate driver. A new test method is described, and the tested performance of the internal protective electrostatic discharge (ESD) structure in the AMT49100 gate driver when exposed to negative voltage conditions is presented for both the high-side and low-side source terminals.

INTRODUCTION

The use of gate drivers in automotive applications requires large currents to be switched into inductive loads at high speed. During turn-off of the bridge MOSFETs, negative voltage transients are generated, and these transients affect performance. For instance, when driving a gate, if the flow of a 100 A current stops quickly, an inductance of approximately 10 nH can result, which generates negative voltage swings. The energy released by such a voltage swing is usually clamped to lower voltages and dissipated within the circuit elements, including the gate drivers.

For example, a typical half-bridge topology that consists of two power MOSFETs, MA and MB, is used to drive, for instance, a motor as the load. When turn-on of high-side MOSFET MA occurs, the load receives power from the main power supply terminal (VBB) or the high-side drain voltage sense terminal (VBRG) supply. When turn-off of MOSFET MA is commanded, the presence of the inductive load prevents an immediate change in direction of the load current. Thus, the freewheeling diode of low-side power MOSFET MB conducts the freewheeling current. Because the source terminal of power MOSFET MB is grounded, the drain terminal of MOSFET MB, which is connected to the source terminal of MOSFET MA, shows a negative voltage. This negative voltage combines with circuit parasitics, which can be introduced by the PCB layout. As a result, a considerably large transient negative voltage can occur on the source terminal of MOSFET MA.

The large transient negative voltage on the source terminal of MOSFET MA is typically connected to the high-side source terminal of the Allegro gate driver. The negative voltage that appears at the high-side source terminal detrimentally impacts typical operation of the gate driver, which can lead to a malfunction or damage to the gate driver. Therefore, the source terminals of the gate driver must be tolerant to such behavior. To accommodate certain levels of transient negative pulses, internal protective ESD structures are often used.

This paper describes a new method to test the negative transient condition on the load connection phase B (SB) and low-side source Phase B (LSSB) source terminals of the AMT49100 gate driver. In the proposed method, AMT49100 source terminals SB and LSSB are exposed to repetitive negative voltage transients, during which AMT49100 source terminals SA and SC are constantly switched to the on state. The goal of this study is to develop a negative-voltage pulse energy measurement and recording technique that is more accurate and more reliable than the typical method, which is to use an inductor as a flywheel to induce negative voltage transient conditions. The purpose is to ensure that the negative voltage levels chosen are not destructive and to provide a significant level of confidence that the gate driver can tolerate the negative voltage transient stress conditions specified in the datasheet of the AMT49100. The experimental tests documented in this application note push the tested AMT49100 gate driver to its limits. By pushing the device to its limits, the test is designed to reveal possible operational gate-driver anomalies induced by dynamic pulsed negative voltages at cold, room, and hot temperatures of –40°C, 25°C, and 150°C, respectively.

TEST METHOD DESCRIPTION

The susceptibility of the AMT49100 gate driver to negative voltage was studied by employing pulse tests or dynamic tests that use a proposed method based on fast-edge voltage pulses obtained from a half-bridge configuration using power gallium-nitride field-effect transistor (GaNFET) devices. In practical applications, Allegro gate drivers might undergo exposure to negative pulses, including high-amplitude and relatively short-duration pulses. During typical circuit operation, energy released by MOSFET switching events might cause these negative pulses to appear frequently at the source terminals of the gate driver.

To prevent damage to circuitry, the gate driver must be able to handle these negative pulses in combination with circuit parasitics, such that the gate driver maintains typical malfunction-free operation during switching events. For this study, power GaNFET devices were selected for the ability to deliver fast (i.e., 1 µs or 1.25 µs) transition or switching of –18 V and –8 V excursions on source terminals SB and LSSB, respectively, as specified in the AMT49100 gate driver datasheet.

Power GaNFET devices also deliver exceptional robust low on-resistance and provide enhanced power density through reduced conduction and reduced switching losses. The test method used in the experimental test of the negative voltage transients reported in this application note is based on fast-edge voltage pulses obtained from a half bridge that employs power GaNFET devices. The test method set-up is divided into the three circuits illustrated in the simplified block diagrams in Figure 1, Figure 2, and Figure 3.

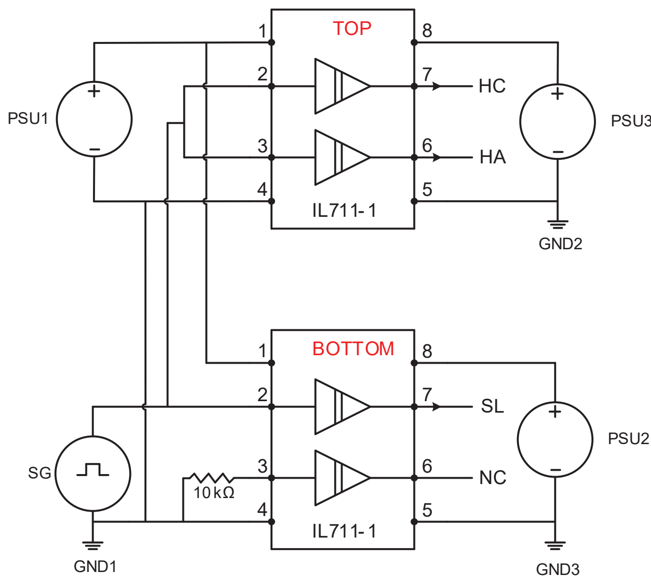

Figure 1: Negative Transient Test, Motherboard

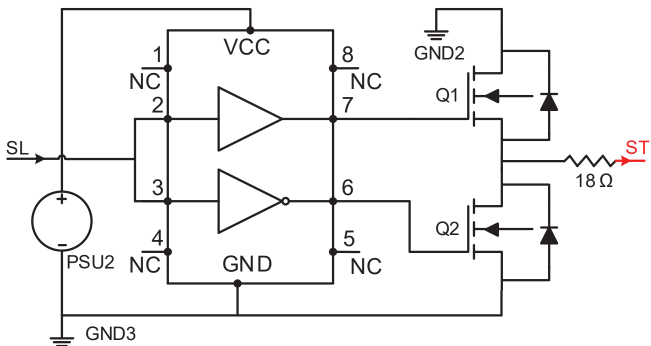

Figure 2: GaNFET Driver, EPC9014, Daughterboard

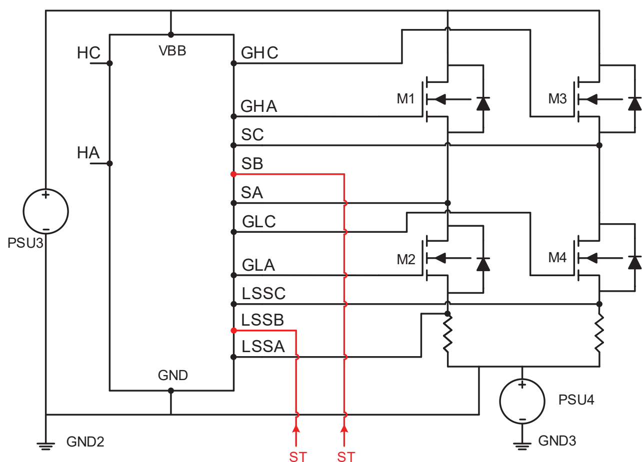

Figure 3: AMT49100 Gate Driver, 48 V

- The first circuit (see Figure 1) acts as a motherboard. It consists of two high-speed two-channel digital isolators (IL711–1); three power supplies, PSU1 (8 V), PSU2 (8 V) and PSU3 (48 V); and a signal generator to provide a triggering signal for the pulse signal (SL). Signal SL is then used as an input signal of the half-bridge power GaNFET devices presented in Figure 2.

  The circuit in Figure 1 also includes high-side control logic input signals HA and HC, which are used to command the high-side gate-drive-phase output signals GHA and GHC of the AMT49100 gate driver. A 10 kΩ resistor controls the input current of the second input terminal of the bottom high-speed two-channel digital isolator. This resistor is used because the second output terminal (NC) of the bottom high-speed two-channel digital isolator is an unused terminal.

- The second circuit of the test setup (see Figure 2) acts like a daughterboard that contains two GaNFET devices in a half-bridge configuration with a GaNFET gate driver and a gate-driver supply (PSU2) of 8 V. This circuit generates the negative voltage transient test signal (ST). Signal ST is the midpoint of the half-bridge configuration created by the GaNFET devices; and, to determine the robustness of the AMT49100 gate driver during bench test evaluation, it is connected in turn to the SB or LSSB terminals. The stress induced with test signal ST should exceed the limits specified in the AMT49100 datasheet; and, to prevent damage to the device under test and to ensure malfunction-free performance after application of the negative voltage transient, a series resistor of 18 Ω is connected between the midpoint of the half-bridge GaNFET devices and terminal ST. This resistor limits current into terminals SB and LSSB when exposed to negative voltage transients.

- The third circuit (see Figure 3) represents the AMT49100 gate driver investigated in this analysis. This circuit is supplied by a power supply (PSU3) of 48 V. The AMT49100 gate driver is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for 48 V automotive power applications with high-power inductive loads, such as a brushless DC (BLDC) motor or a permanent magnet synchronous motor (PMSM). The negative voltage transient analysis presented in this application note was performed on phase B of the AMT49100 gate driver. Phase B was selected for tests based on the physical location of the phase B internal ESD structure for the AMT49100 gate driver: During operation, phase B undergoes higher total parasitic capacitance

values than phase A or phase C. This is because the phase B internal ESD structure is located in the middle and in parallel to phase A and phase C. Thus, the total parasitic capacitance of phase B is almost twice that of phase A or phase C. In high-frequency, fast-switching, and high-current gate driver applications, the parasitic capacitance produced by the internal ESD structure becomes especially important. However, the negative-transient test method presented in this application note can also be used to test either phase A or phase C of the AMT49100 gate driver.

The HA and HC logic input signals generated from the top high-speed two-channel digital isolator (shown in Figure 1) used for turn-on of the GHA and GHC gate outputs of the AMT49100 gate driver, while turn-on of the GLA and GLC gate output signals is not commanded, is also shown in Figure 3, as is power supply PSU4. In this analysis, PSU4 is used to set the negative voltage of –18 V or –8 V on the SB and LSSB terminals, by varying the PSU4 voltage power supply between 0 V and 35 V, respectively.

IMPORTANT: For proper operation of the transient test circuit presented in Figure 1, Figure 2 and Figure 3, ground signal GND3 should be independent of both ground signals GND1 and GND2. The negative voltage pulses on the LSSB and SB terminals should be measured using a differential probe.

ELECTROSTATIC DISCHARGE STRUCTURE

Automotive applications often require high-current driving and hard switching to drive large loads. This hard switching of the power MOSFETs, in combination with layout constraints, often leads to negative transient voltages at the gate driver source terminals, SA, SB, SC, LSSA, LSSB, and LSSC, in the Allegro AMT49100 gate driver.

To handle short negative transient pulses at the source terminals of the gate driver, most Allegro gate drivers are designed with a built-in internal ESD structure, such as that of the Allegro AMT49100 gate driver illustrated in Figure 4 and Figure 5. This structure is designed to clamp a short (less than 1 µs) transient voltage pulse that varies in voltage from –18 V to the value of the bootstrap capacitor voltage:

- On the high side, this variation is typically 9.1 V plus 0.3 V for the high-side source terminals, SA, SB, and SC, as shown in Figure 4.
- On the low-side, this variation is typically –8 V to 18 V for the low-side source terminals, LSSA, LSSB and LSSC, as shown in Figure 5.

Depending on application and customer requirements, the negative transient voltages on the high-side and low-side source terminals should be limited to the equivalent values of the clamping ESD structure, as presented in Figure 4 and Figure 5. Any excessive negative excursions on the high-side and low-side source terminals of the gate driver can damage the internal ESD structure and can affect the performance of the AMT49100 gate driver. Thus, to prevent device damage, energy into the source terminals of the gate driver must be limited such that the power dissipated by the internal ESD structure is able to protect the device.

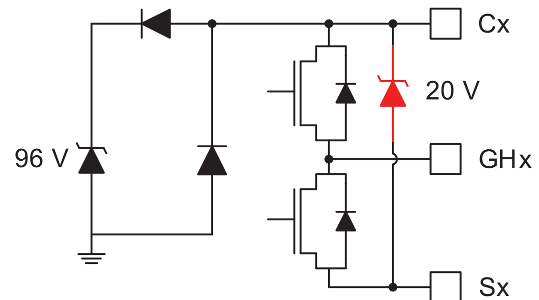

Figure 4: High-Side Internal ESD Structure

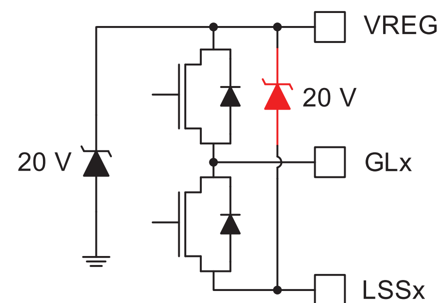

Figure 5: Low-Side Internal ESD Structure

EXPERIMENTAL RESULTS

The performance of the negative-transient test method presented in Figure 1 through Figure 3 was verified on the bench using several experiments performed with the AMT49100 gate driver.

The test bench contains:

- DC power supplies
- 70 MHz Tektronix TBS2000B scope
- Signal generator that provides a signal (SG) switching at a frequency of 20 kHz
- Driver for GaNFETs
- Four-layer AMT49100 Allegro demonstration board
- 200 MHz Tektronix TMDP0200 differential probe used to measure the negative voltage pulses
- 20 A Tektronix TCP0020 current probe used to monitor the current during negative transient conditions
- 69 mm by 89 mm, four-layer, negative transient test motherboard (see Figure 6), designed and populated to ensure good radio-frequency parameters of the coupling and decoupling networks
- Stitching of ground vias, used to tie together larger copper areas on layers, in effect creating a strong vertical connection through the board structure, maintaining a low impedance, and providing short return loops for the negative transient test motherboard.

Components in the experimental test were selected to satisfy several parameters:

- GaNFETs Q1 and Q2 devices were selected to have operating drain-to-source voltage, V_{DS}, of greater than 200 V, and fast propagation delay during device switch-on and switch-off, typically 25 ns. Additional parameters are presented in Table 1.
- MOSFETs M1, M2, M3, and M4 were selected based on their maximum total gate charge of 100 nC by ensuring that the average current used by the AMT49100 gate driver is within the specified limit of 100 mA, with a typical regulator voltage of 12.5 V, as specified in the AMT49100 datasheet. Additional parameters are presented in Table 1.

The experimental tests were performed by application of a negative pulse voltage of 1 µs or 1.25 µs on the LSSB and SB terminals of the AMT49100 gate driver; this corresponds to approximately 98% and 97.5% duty cycles of signal SG, respectively, with signal SG generated from a signal generator switching at a frequency of 20 kHz.

Terminal performance in response to a negative transient pulse, during device operation at cold, room, and hot temperatures of –40°C, 25°C and 150°C, respectively, is illustrated in:

- Figure 7, Figure 8, and Figure 9, for the LSSB terminal.
  - The measured energies and powers generated on the LSSB terminal with a –10 V pulse of 1 µs period obtained from the experimental tests presented in these figures are also presented Table 2.
- Figure 10, Figure 11, and Figure 12, for the SB terminal.
  - The measured energies and powers generated on the SB terminal with a –18.4 V pulse of 1 µs period obtained from bench evaluation presented in these figures are also presented in Table 3.

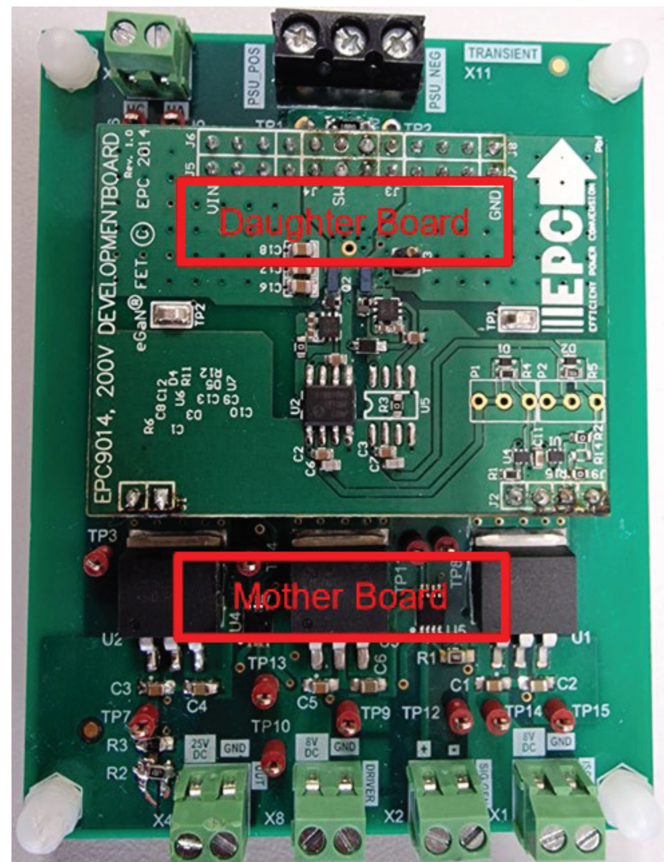

Figure 6: Designed Negative Transient Test Board

Table 1: GaNFET and MOSFET Parameters

Parameter	Q1 = Q2	M1 = M2 = M3 = M4	Unit
R_{DSON}	22	18	mΩ
V_{DS}	200	100	V
I_{DS}	8.5	42	A

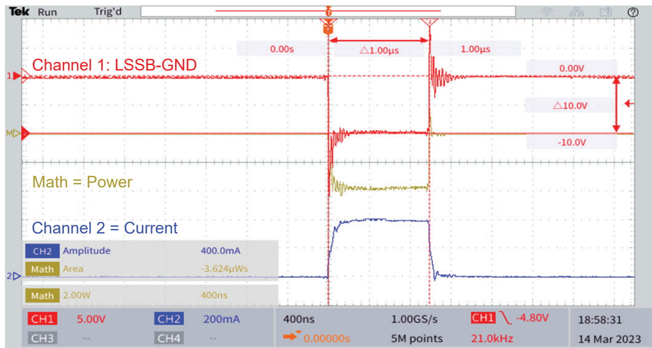

Figure 7: LSSB Terminal, –10 V at –40°C, 1 µs Pulse

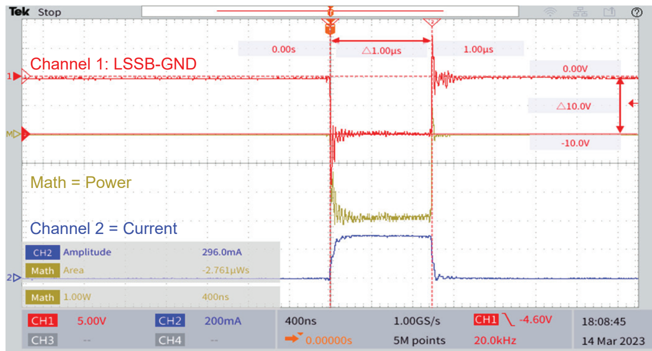

Figure 8: LSSB Terminal, –10 V at 25°C, 1 µs Pulse

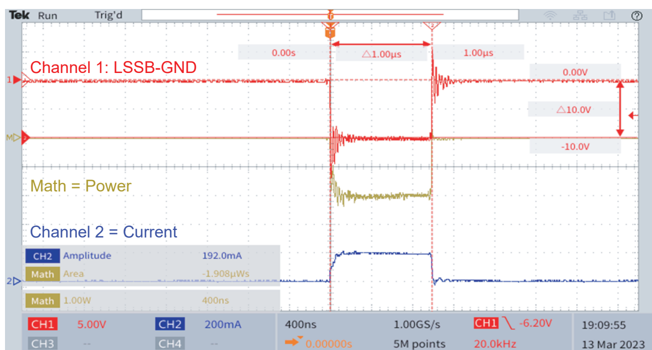

Figure 9: LSSB Terminal, –10 V at 150°C, 1 µs Pulse

The energies (E) produced and the powers (P) dissipated can also be estimated as:

Equation 1:

$$E = Voltage \times Current \times t_{pulse}$$

Equation 2:

$$P = Voltage \times Current \times t_{pulse} \times f_{sw}$$

The experimental tests were performed in a controlled temperature chamber. To estimate the junction temperature of the AMT49100 gate driver, the internal voltage of the silicon on the diagnostic (DIAG) terminal was measured. This closely represents the surface temperature of the silicon, as described in the AMT49100 datasheet.

The results of tests using a –10 V pulse with a 1 µs period applied to the LSSB terminal of the AMT49100 gate driver are

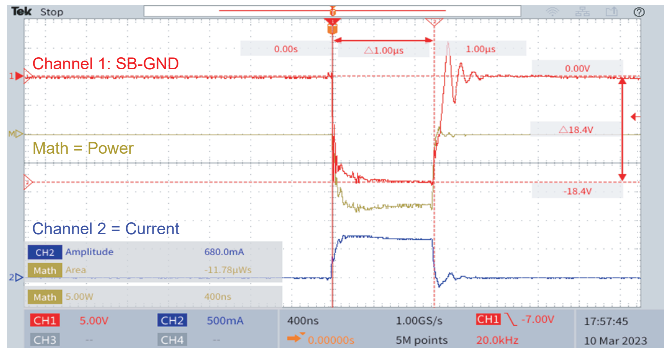

Figure 10: SB Terminal, –18.4 V at –40°C, 1 µs Pulse

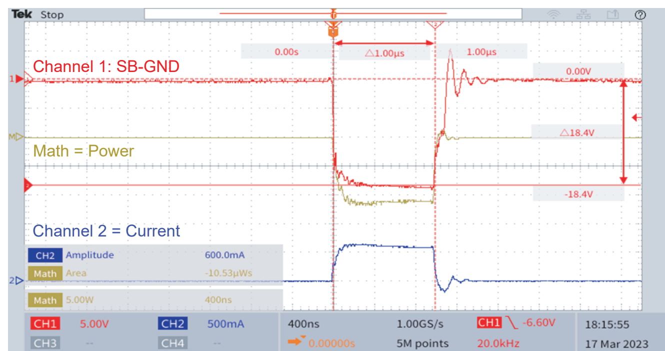

Figure 11: SB Terminal, –18.4 V at 25°C, 1 µs Pulse

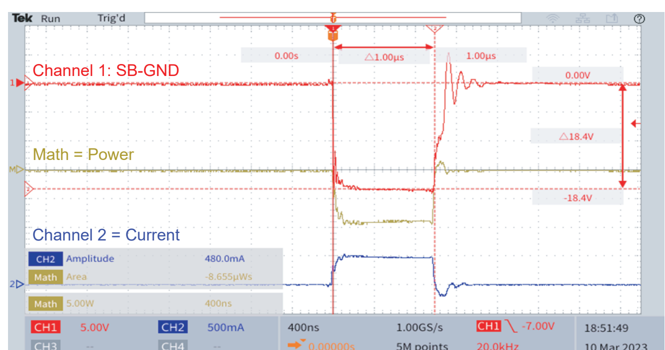

Figure 12: SB Terminal, –18.4 V at 150°C, 1 µs Pulse

shown in Table 2. The data show less energy generation at high temperature: The measured energy of the hot-temperature test is 1.91 µJ, which is 47% less than the 3.6 µJ measured in the cold-temperature test.

The results of tests using a –18.4 V pulse with a 1 µs period applied to the SB terminal of the AMT49100 gate driver are shown in Table 3. The data show less energy generation at high temperature: The measured energy of the hot-temperature test is 8.66 µJ, which is 27% less than the 11.78 µJ measured in the cold-temperature test.

The susceptibility of the AMT49100 to negative voltage pulse was furthermore investigated by increasing the pulse-width period from 1 µs to 1.25 µs on the LSSB and SB terminals. The generated energies were measured and are presented in Table 4 for the LSSB terminal and Table 5 for the SB terminal.

Table 2: LSSB Terminal, Measured Energy, 1 μs Pulse

LSSB Terminal, –10 V and Negative Pulse of 1 μs				
Tempera-ture [°C]	Current [mA]	Estimated Energy [μJ]	Measured Energy [μJ]	Estimated Power [mW]
–40	400	4	3.60	80
25	266	2.96	2.76	59
150	190	1.92	1.91	38

Table 3: SB Terminal, Measured Energy, 1 μs Pulse

SB Terminal, –18.4 V and Negative Pulse of 1 μs				
Tempera-ture [°C]	Current [mA]	Estimated Energy [μJ]	Measured Energy [μJ]	Estimated Power [mW]
–40	680	12.4	11.78	250
25	600	11	10.93	220
150	480	8.83	8.66	176

Table 4: LSSB Terminal, Measured Energy, 1.25 μs Pulse

LSSB Terminal, –9 V and Negative Pulse of 1.25 μs				
Tempera-ture [°C]	Current [mA]	Estimated Energy [μJ]	Measured Energy [μJ]	Estimated Power [mW]
–40	310	3.48	3.23	70
25	250	2.8	2.58	55
150	160	1.8	1.864	36

Table 5: SB Terminal, Measured Energy, 1.25 μs Pulse

SB Terminal, –18 V and Negative Pulse of 1.25 μs				
Tempera-ture [°C]	Current [mA]	Estimated Energy [μJ]	Measured Energy [μJ]	Estimated Power [mW]
–40	640	14.44	13.94	288
25	540	12.15	12	243
150	440	9.9	10	198

The energies produced using a –9 V pulse with a 1.25 μs period applied to the LSSB terminal of the AMT49100 gate driver are shown in Table 4. The data show less energy generation at high temperature: The measured energy of the hot-temperature test is 1.864 μJ, which is almost 42% less than the 3.23 μJ measured in the cold-temperature test.

The energies produced using a –18 V pulse with a 1.25 μs period applied to the SB terminal of the AMT49100 gate driver are shown in Table 5. The data show less energy generation at high temperature: The measured energy of the hot-temperature test is 10 μJ, which is approximately 42% less than the 13.94 μJ measured in the cold-temperature test.

For both the increased voltage amplitude stress condition (shown in Table 2 and Table 3) and the increased pulse width stress condition (shown in Table 4 and Table 5), the internal built-in ESD structure of the AMT49100 device successfully sustained the stresses, the device did not malfunction, and the SPI register of the AMT49100 device did not exhibit a fault; this includes consideration for temperature warning and overtemperature shutdown. However, any attempt to further increase the amplitude and period of the negative pulse voltage on the LSSB and SB terminals of the device results in excessive stress that can damage the internal protective ESD structure and can cause a loss in functionality of the AMT49100 device.

SUMMARY

This paper provides a new method that can be used to verify the reliability and robustness of the internal protective ESD structure of the most-prevalent Allegro automotive gate drivers, such as the A4911, A4913, A4916, A4918, A89199, AMT49100, AMT49101, AMT49105, AMT49106, and AMT49107. Experimental results demonstrate that, for both the increased voltage-amplitude stress condition and the increased pulse-width stress condition, the internal protective ESD structure of the AMT49100 device can sustain stresses without a device malfunction from a cold temperature of –40°C to a hot temperature of 150°C.

Revision History

Number	Date	Description	Responsibility
–	February 12, 2026	Initial release	K. Tshiloz

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