ALLEGRO FIELD CURRENT SENSORS: UNDERSTANDING TOPOLOGIES AND PACKAGES

By Florian Kulla
Allegro MicroSystems

INTRODUCTION

Allegro MicroSystems offers a comprehensive portfolio of field current sensors designed to meet the diverse needs of modern electronic systems. These sensors are critical for precise current measurement in the range of <100 A to >10 kA in automotive and industrial applications. To select the proper field current sensor for the application, its topology must be understood—specifically, whether it uses a C-core, U-core, or fully coreless design—as well as the associated package types that facilitate optimal integration and performance. This application note explores the different topologies and identifies the Allegro packages used for each. Allegro field sensor package dimensions and drawings are provided in the appendix. For simulation, the latest updates and three-dimensional (3D) model files of the packages are provided on the Allegro website.

TABLE OF CONTENTS

C-CORE TOPOLOGY

C-core field current sensors are typically designed to work with an external ferromagnetic core that concentrates the magnetic field generated by the current-carrying conductor. This design provides the highest signal-to-noise ratio (SNR), allowing for very accurate measurements and the highest resolution. The external core also shields the sensor from stray magnetic fields, improving crosstalk immunity while amplifying the magnetic field generated by the conductor.

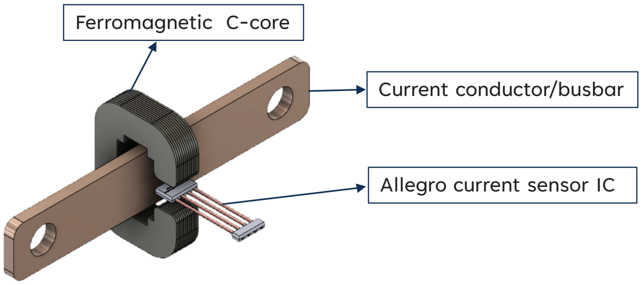


Figure 1: C-Core Topology Current Sensor

Allegro Packages for C-Core Sensors

Allegro offers a wide variety of single in-line packages (SIPs) and surface-mount device (SMD) packages that can be used for C-core applications.

KT Package (4-Pin SIP)

The KT package is a single in-line package. It is the most popular Allegro package because its 1 mm thickness enables very narrow air gaps. The highest-accuracy, safety-rated Allegro devices—ACS37601, ACS37503, and ACS70310/1—feature this package, as well as multiple legacy Allegro devices. Traditionally this package is offered with straight leads (TN) and is assembled as a through-hole device. Different lead-formed options are available to enable surface-mount assembly and to optimize different system requirements.

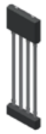
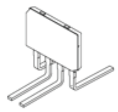
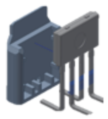
- **TH:** The V-shape design acts as a spring that improves resilience to mechanical vibration
- **TG:** Ideal for systems where the printed circuit board (PCB) and the C-core are situated in close proximity to each other
- **TY:** Offers added protection to the package and leads

These variations can be important for specific manufacturing processes, board layouts, or environmental considerations, ensuring robust connections and optimal performance. Other options might be possible; to inquire about possibilities, contact Allegro.

The leadform option is indicated in the device catalog part number as follows, shown in bold:

- ACS37503LKTA**TN**-001B5-C
- ACS37503LKTA**TH**-001B5-C
- ACS37503LKTA**TG**-001B5-C
- ACS37503LKTA**TY**-001B5-C

KT package leadforms

TN	TH	TG	TY
			

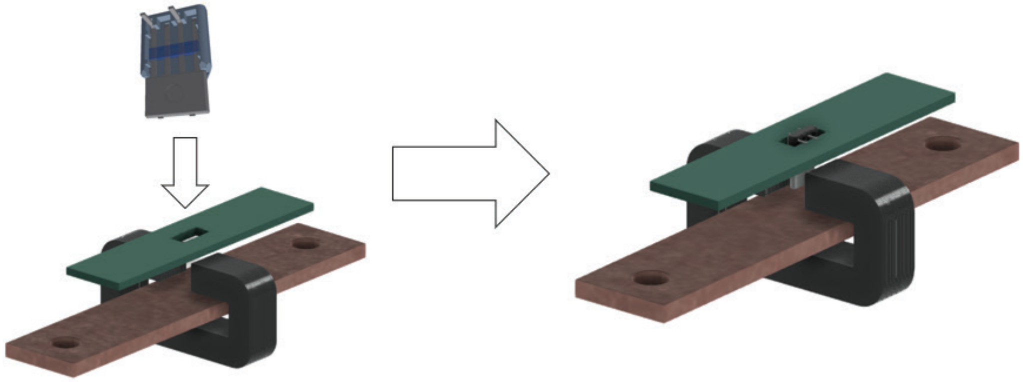


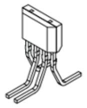
Figure 2: C-Core Assembly Example Using KTTY Package

OK Package (4-Pin SIP)

The OK package is a single in-line package that offers thicker leads relative to the KT package. The thicker leads make the OK package ideal for designs with very high levels of mechanical vibrations. The long leads of the package enable PCB-less module designs. The most popular Allegro devices—ACS37601, ACS70311, and ACS37600K—are offered in this package. Currently, the OK package is available in one leadformed option:

- **TX:** This V-shape design acts as a spring that improves resilience to mechanical vibration. Coupled with thick leads, it is a very robust option for a SIP with an SMD assembly.

More options are in development.

OK package leadforms	
TN	TX
	

UA Package (3-Pin SIP)

The UA package is a three-pin single in-line package. Compared to the KT package, this package offers a more-compact size with thicker and longer leads. This is the most cost-effective solution from Allegro. For a list of devices offered in this package, contact Allegro.

UA


LU Package (8-Pin TSSOP)

The thin-shrink small-outline package (TSSOP) enables native SMD assembly in a C-core topology. Although use of this package is less common, some systems benefit from this configuration, where the PCB is inserted in the air gap of the C-core. The higher pin count also enables additional features, for example dedicated reference voltage and overcurrent pins. Allegro devices ACS37600 and A1363 feature this package.

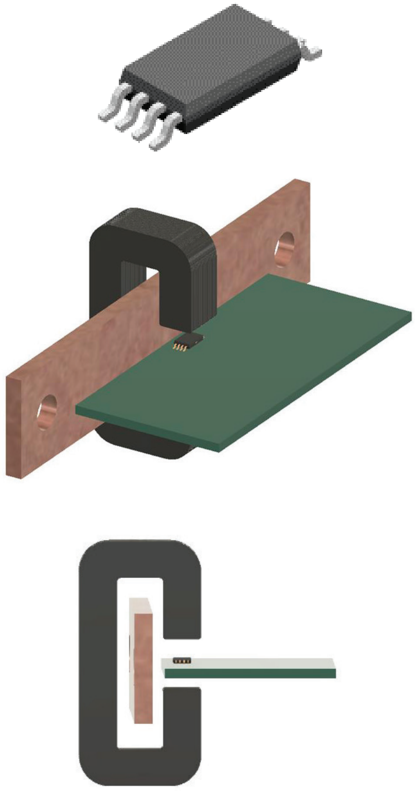


Figure 3: C-Core Assembly Example Using TSSOP

U-CORE TOPOLOGY

U-core field current sensors rely on an external U-shaped magnetic concentrator. Compared to a C-core system, the "U" shape often implies a more-compact design and a simpler assembly process because the core can be integrated directly onto a PCB or within a module. While offering many advantages, the SNR, linearity, and stray-field immunity of a U-core system are typically lower than a C-core system and the cost is comparable because both the C-core and U-core must be laminated if a high-frequency response is desired. In applications where the current is traveling through the PCB, instead of a busbar, U-core designs should be compared to coreless designs (discussed in the Coreless/Contactless Topology section). All the U-core products can also be used without the U-shield to reduce cost and size if the performance is acceptable and concerns of stray fields are not present. The SOIC-8 package is a common choice for current sensors used in U-core systems.

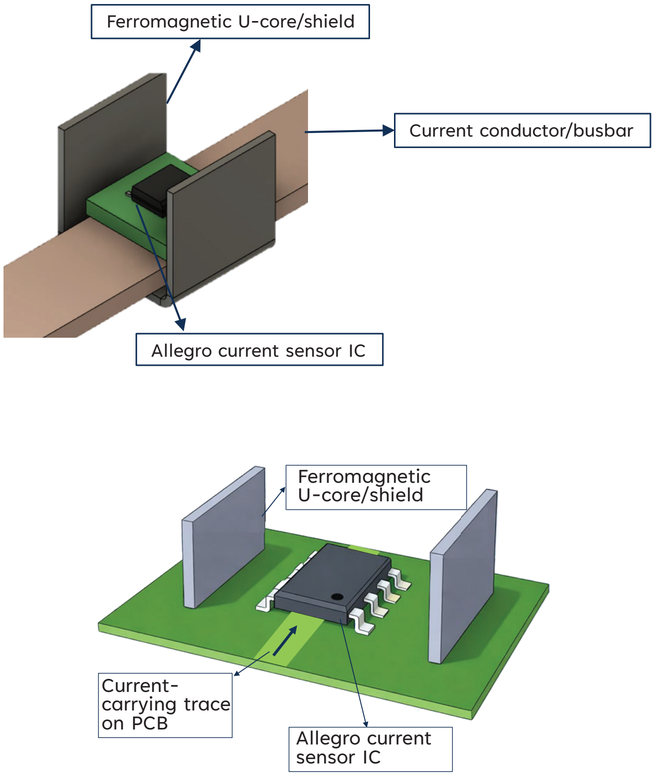
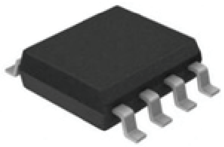


Figure 4: U-Core Assembly Example with Busbar or PCB Trace

Allegro Packages for U-Core Sensors

OL Package (SOIC-8)

The 8-lead small-outline integrated circuit (SOIC) package is a versatile surface-mount option used in Allegro products that go into a U-core topology. Allegro current sensors available in this package include the ACS37630 and CT455. The SOIC-8 package offers a balance of size and performance, making it suitable for applications where space is a consideration and an SMD sensor is required.



8-lead SOIC

TSSOP (8-Pin)

The Allegro CT455 is also offered in an eight-pin, thin-shrink small-outline package (TSSOP), which provides flexibility in package choice for this product.

8-lead TSSOP

SOT23-5 Package

The 5-pin small-outline transistor (SOT23-5) is a very small cost-effective package. For example, the Allegro CT220 offered in an SOT23-5 package can be used similarly to other coreless devices, placed directly over a PCB trace or busbar. To improve the resolution and to provide a shield from external fields, the CT220 has a uniform field measurement that allows it to also be used with a U-shield if needed. The CT220 is the perfect solution for a low-cost simple current measurement.

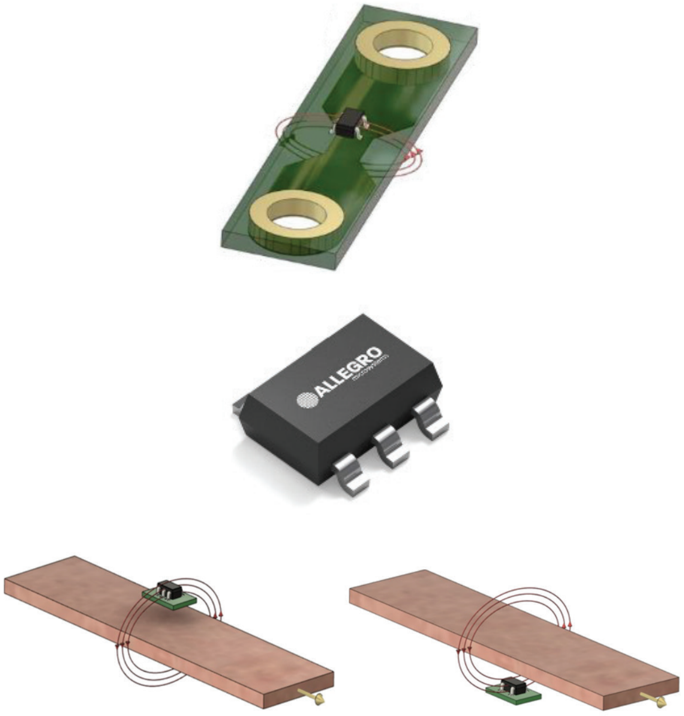


Figure 5: CT220 Assembly Example

CORELESS/CONTACTLESS TOPOLOGY

Coreless field current sensing is a revolutionary approach pioneered by Allegro. It eliminates the need for an external ferromagnetic concentrator by measuring directly the magnetic field generated from a current-carrying busbar or PCB trace. This sensing method offers significant advantages in terms of size, weight, cost, reduction of bill of materials (BOM), and design flexibility. It employs differential sensing to reject common-mode magnetic fields, ensuring high immunity to external interference.

Allegro has published multiple application notes highlighting design guidelines and advantages of this coreless topology. This document focusses on the physical aspects of the system and the available packages.

NOTE: While not recommended by Allegro, U-core products are sometimes used in coreless systems. In such a system, the U-core product does not offer immunity to stray magnetic fields, and the coupling factor is lower.

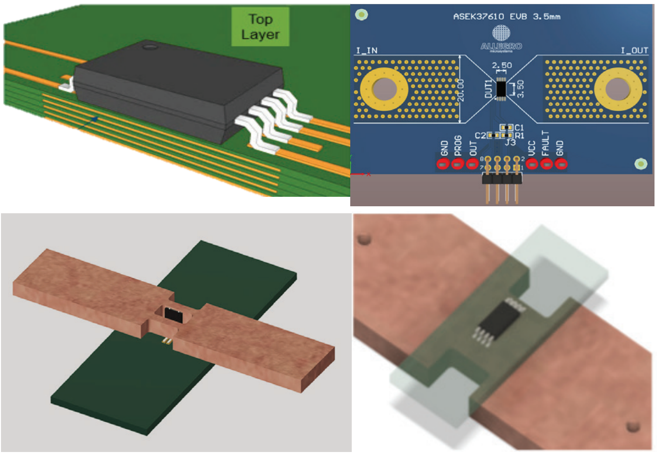
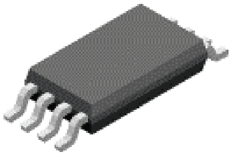


Figure 6: Coreless Assembly Examples

Allegro Packages for Coreless Sensors

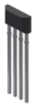
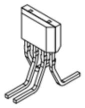
TSSOP (8-Pin)

The TSSOP is a popular package choice for coreless sensors due to its small footprint and low profile, which are crucial in space-constrained designs. Prime examples of coreless high-precision Hall-effect current sensor ICs housed in an 8-pin TSSOP are the Allegro ACS37611, ACS37610, and ACS37612. These devices are designed for contactless current sensing directly from a busbar or PCB trace, offering integrated overcurrent and overtemperature detection, and robust common-mode field rejection. The Allegro CT456, a tunneling magnetoresistance (TMR) based differential coreless current sensors, also uses the 8-lead TSSOP, providing high bandwidth and programmability.



OK Package (4-Pin SIP)

While traditionally associated with C-core designs, a 4-pin SIP, such as the Allegro OK package, is also used in coreless products. For example, the Allegro ACS37610OK performs differential coreless measurement inside the SIP. This package facilitates the ability to use a coreless topology when the sensor is required to be inserted through the busbar, an approach that is natively more tolerant to displacement error over the life of the product. Both straight leadform (TN) and V-shaped leadform (TX) options are available for this product.

OK package leadforms	
TN	TX
	

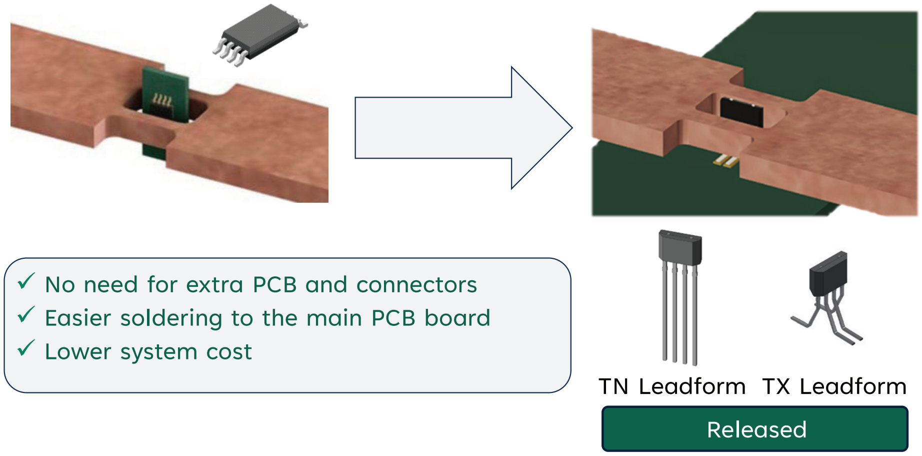


Figure 7: Dual-Bridge Assembly Example with TSSOP and SIP

CONCLUSION

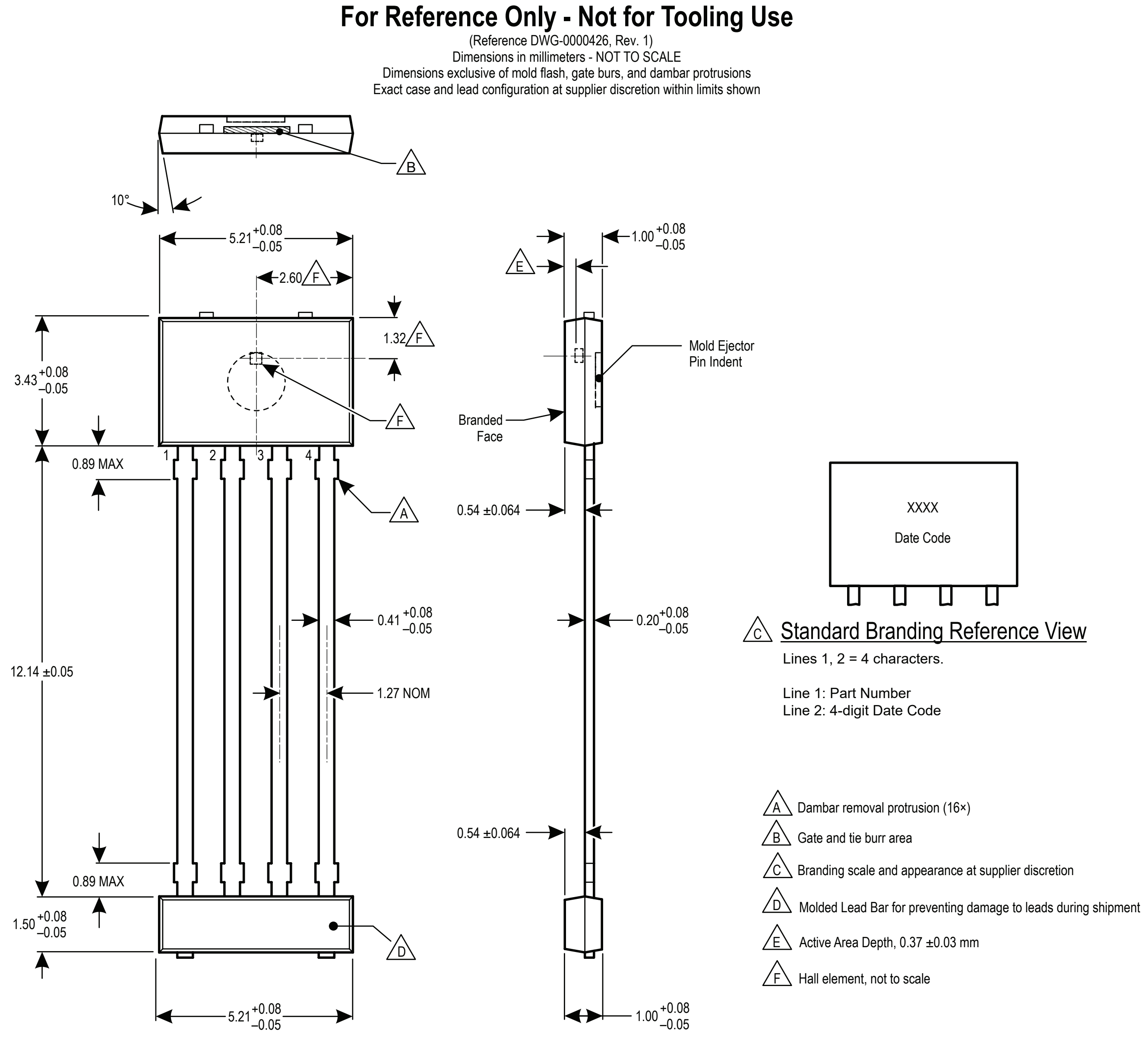
Allegro MicroSystems provides a diverse range of field current sensors across C-core, U-core, and coreless topologies. Each topology offers unique advantages for specific application requirements. By understanding the characteristics of each topology and the associated package types—including SIP variants like the Allegro KT, OK, and surface-mount package options, including TSSOP and SOIC-8 packages—designers can select the optimal solution for specific current-sensing needs, ensuring high accuracy, reliability, and efficient system integration. Information about the physical dimensions and drawings of such solutions are presented in the appendix.

APPENDIX: PACKAGE OUTLINE DRAWINGS AND PACKING INFORMATION

Drawing and dimensions of the Allegro packages discussed in this application note are presented in this appendix. All information is for reference purposes only, not for tooling use. For additional information, see https://www.allegromicro.com/en/design-support/packaging.

KT Package Options

KT Package, TN Leadform



For Reference Only - Not for Tooling Use

(Reference DWG-0000426, Rev. 1)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

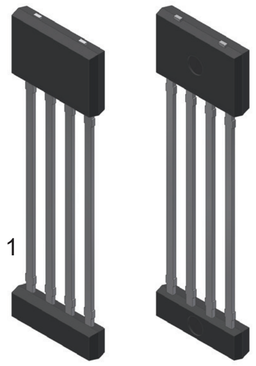
C Standard Branding Reference View

Lines 1, 2 = 4 characters.

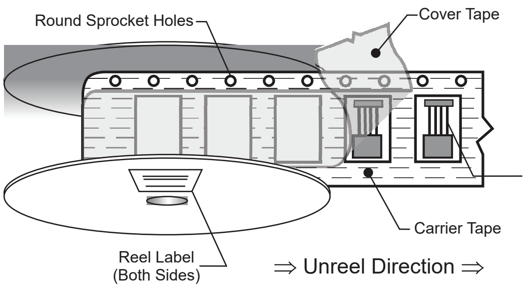
Line 1: Part Number
Line 2: 4-digit Date Code

A Dambar removal protrusion (16×)
B Gate and tie burr area
C Branding scale and appearance at supplier discretion
D Molded Lead Bar for preventing damage to leads during shipment
E Active Area Depth, 0.37 ±0.03 mm
F Hall element, not to scale

Figure 8: KT Package, TN Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)

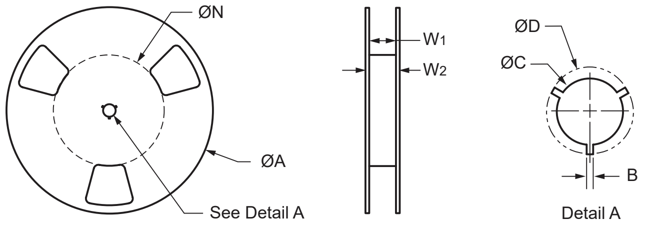


Terminals: 4
Straight
Untrimmed
Unformed (flat)
Non-JEDEC Standard



- Embossed tape and reel
- 4000 devices per 13 in. reel
- 25 min. trailer pockets
- 55 min. leader pockets
- Branded face outward
- Device body on left side
- Elongated sprocket holes on left side
- Pin 1 on leading device edge

Leader pockets are the first off the reel when the tape is unreeled for dispensing devices. Trailer pockets are the last pockets off the reel when unreeled for dispensing devices.

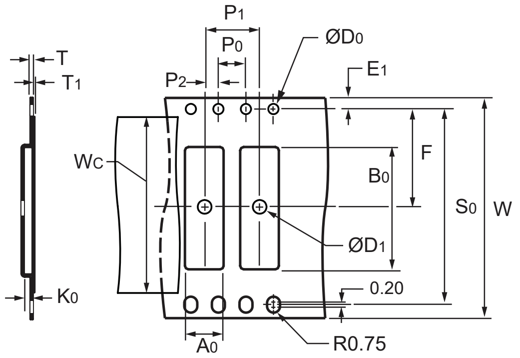


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)			32.4 (Min)		
W_2 (outside, at Hub)			38.4 (Max)		

Reference EIA 481

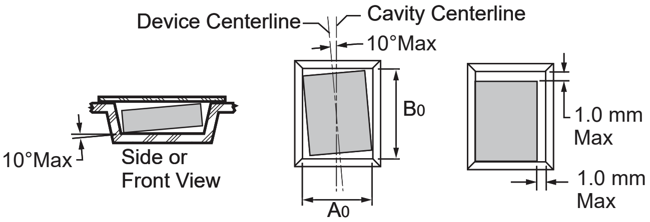


Dimensions in mm, may vary with supplier

Carrier Tape			Cover Tape
W: 32.00 ±.3 E_1: 1.75 ±.1 F: 14.20 ±.1 T: 0.30 (0.1 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 8.00 ±.1 P_2: 2.00 ±.1 S_0: 28.40 ±.1	A_0: 5.60 B_0: 17.70 K_0: 1.30 D_1: 2.00 MIN	W_C: 25.5 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3 mm above bottom of pocket.

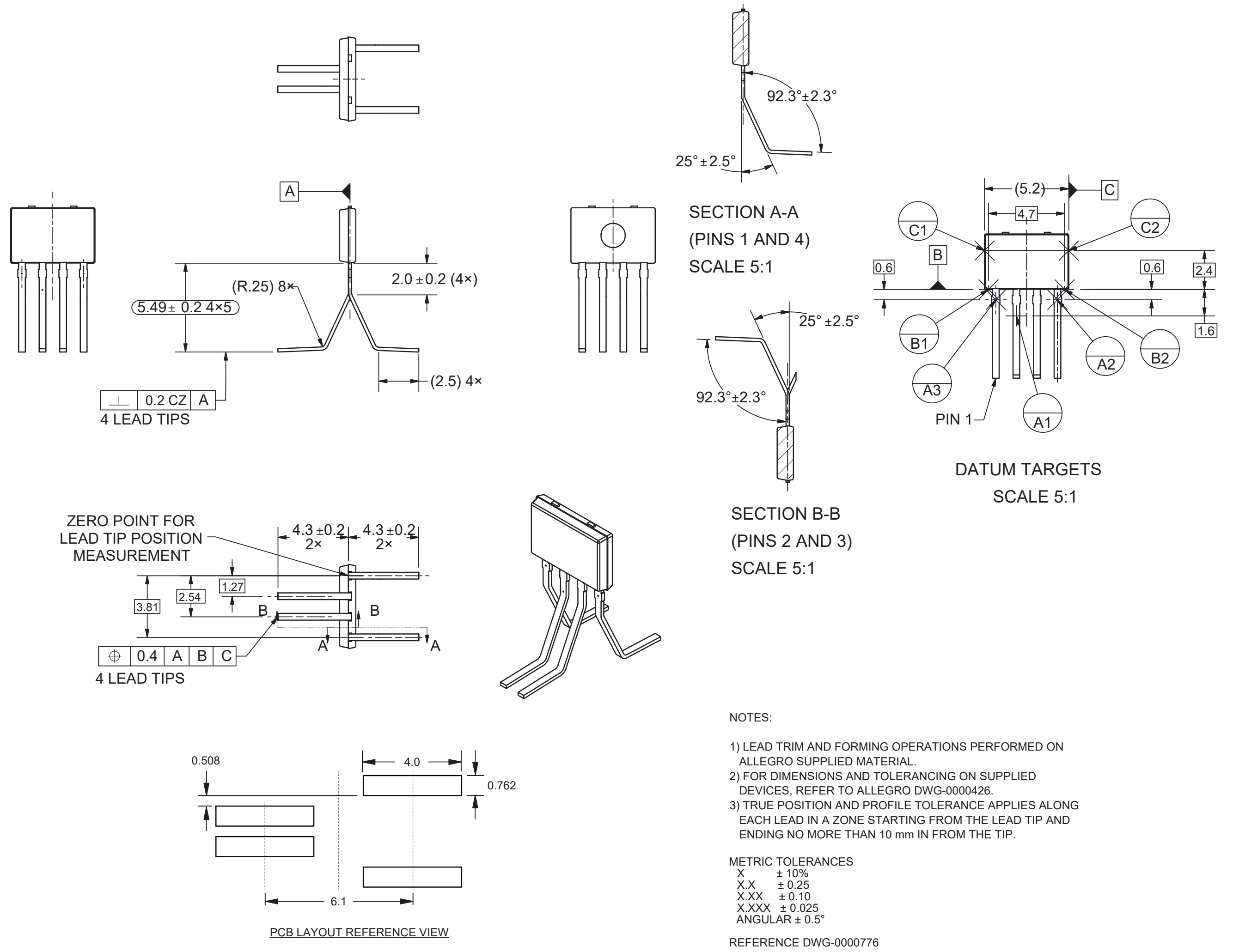
Reference EIA 481



Reference EIA 481

Figure 9: KT Package, TN Leadform, Packing Information (For Reference Only; Not For Tooling Use)

KT Package, TH Leadform



NOTES:

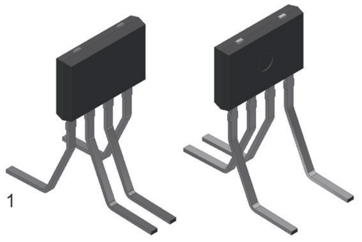
1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES

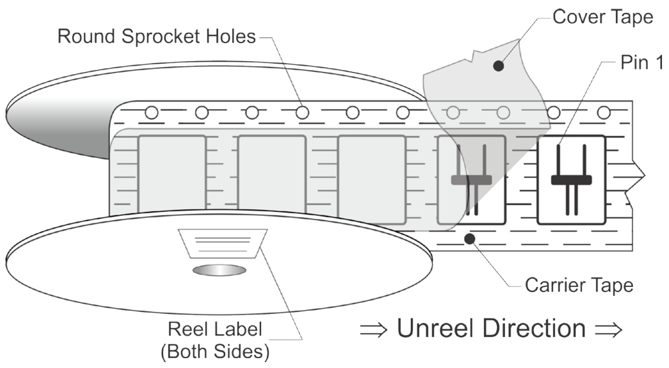
X	± 10%
X.X	± 0.25
X.XX	± 0.10
X.XXX	± 0.025
ANGULAR	± 0.5°

REFERENCE DWG-0000776

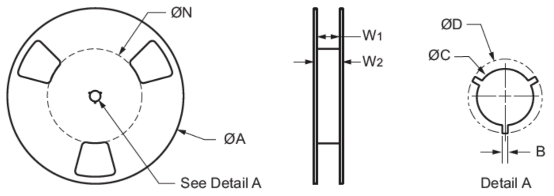
Figure 10: KT Package, TH Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 4
Through hole pins
Customer Specific Leadform



- Embossed tape and reel
- 500 devices per 13 in. reel
- 35 min. trailer pockets
- 100 min. leader pockets
- Pin 1 on trailing device edge, sprocket hole side

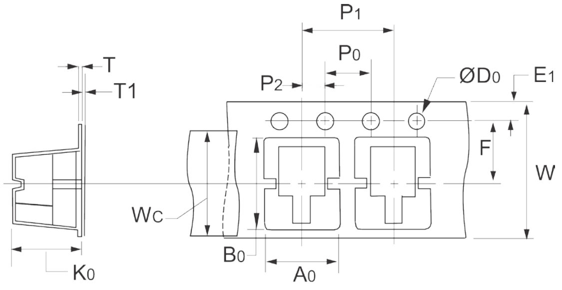


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)			32.4 (Min)		
W_2 (outside, at Hub)			38.4 (Max)		

Reference EIA 481

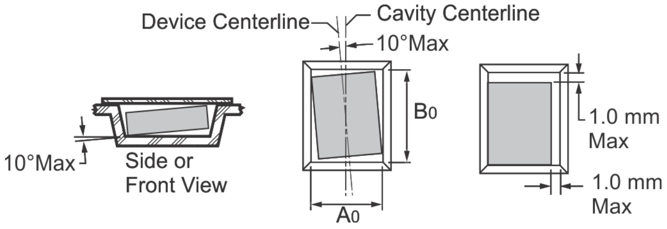


Dimensions in mm, may vary with supplier

Carrier Tape			Cover Tape
W: 16.00 ±.3 E_1: 1.75 ±.1 F: 7.50 ±.1 T: 0.40 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 12.00 ±.1 P_2: 2.00 ±.1	A_0: 8.50 B_0: 9.48 K_0: 9.12	W_C: 13.10 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

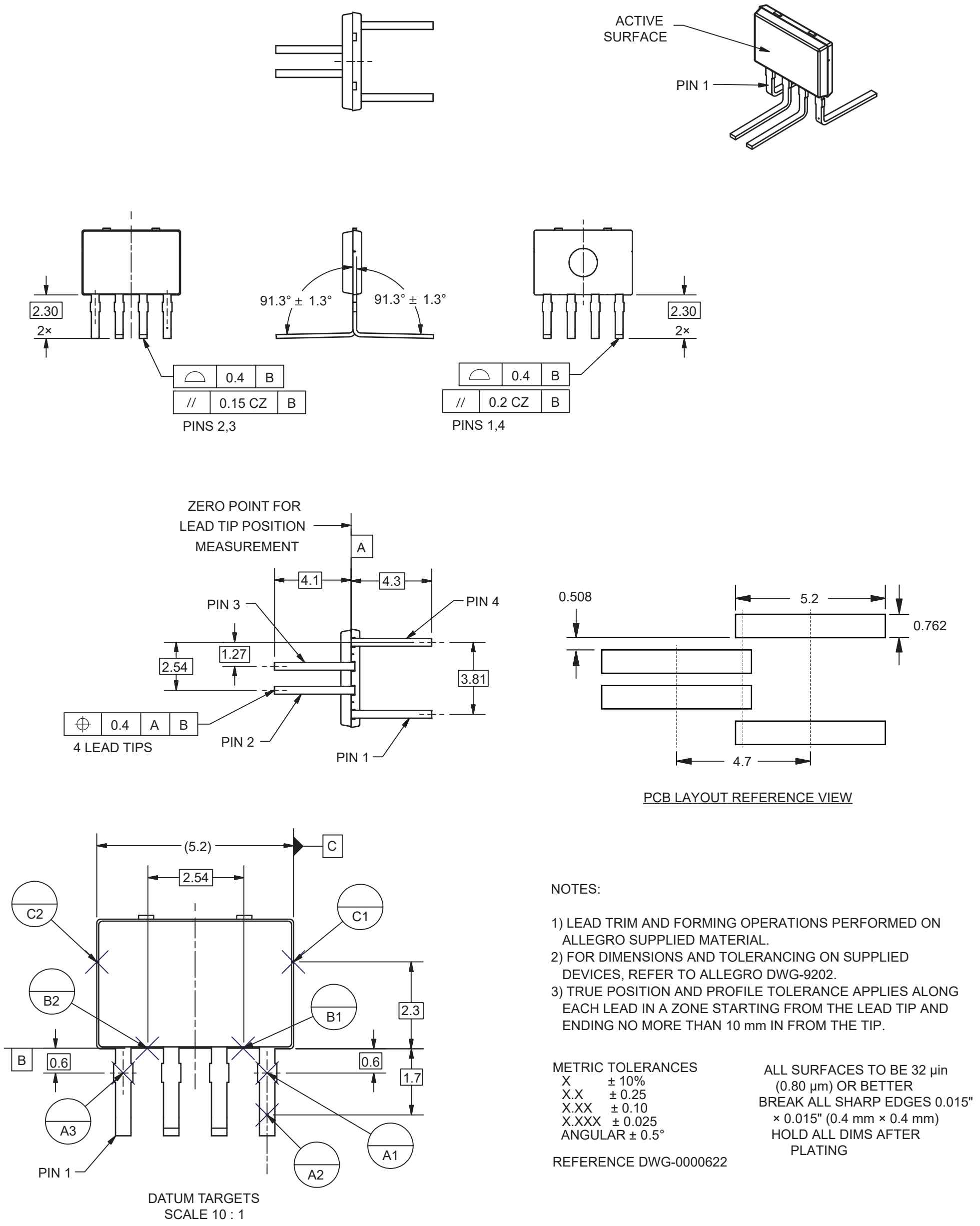
Reference EIA 481



Reference EIA 481

Figure 11: KT Package, TH Leadform, Packing Information (For Reference Only; Not For Tooling Use)

KT Package, TG Leadform



NOTES:

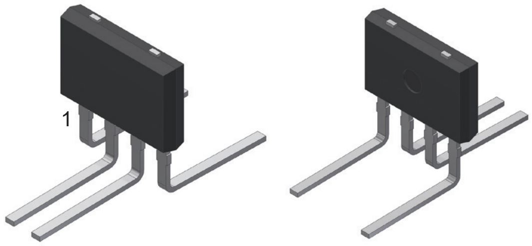
1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-9202.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES	
X	± 10%
X.X	± 0.25
X.XX	± 0.10
X.XXX	± 0.025
ANGULAR	± 0.5°

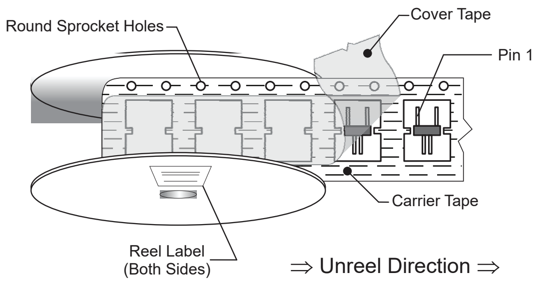
REFERENCE DWG-0000622

ALL SURFACES TO BE 32 µin (0.80 µm) OR BETTER
BREAK ALL SHARP EDGES 0.015" × 0.015" (0.4 mm × 0.4 mm)
HOLD ALL DIMS AFTER PLATING

Figure 12: KT Package, TG Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)

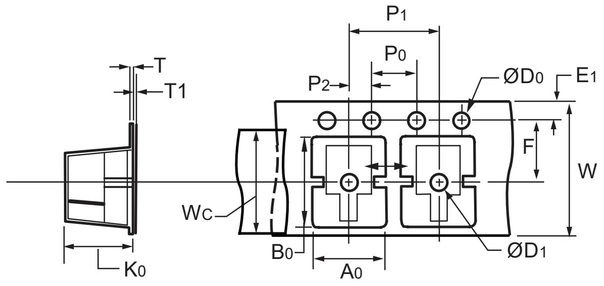


Terminals: 4
Through hole pins
Customer Specific Leadform



- Embossed tape and reel
- 750 devices per 13 in. reel
- 25 min. trailer pockets
- 100 min. leader pockets
- Pin 1 on trailing device edge, sprocket hole side

Leader pockets are the first off the reel when the tape is unreeled for dispensing devices. Trailer pockets are the last pockets off the reel when unreeled for dispensing devices.

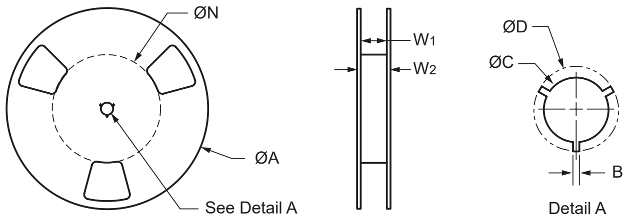


Dimensions in mm, may vary with supplier

Carrier Tape			Cover Tape
W: 16.00 ±.3	D_0: 1.50 +.1/-.0	A_0: 8.00	W_C: 13.1 T_1: 0.061 (0.1 MAX)
E_1: 1.75 ±.1	P_0: 4.00 ±.1	B_0: 9.10	
F: 7.50 ±.1	P_1: 12.00 ±.1	K_0: 6.31	
T: 0.40 (0.6 MAX)	P_2: 2.00 ±.1	D_1: 1.50 MIN	

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3 mm above bottom of pocket.

Reference EIA 481

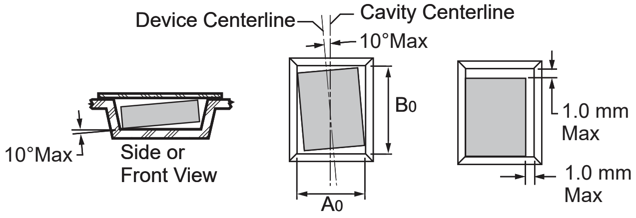


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)			16.4 (Min)		
W_2 (outside, at Hub)			22.4 (Max)		

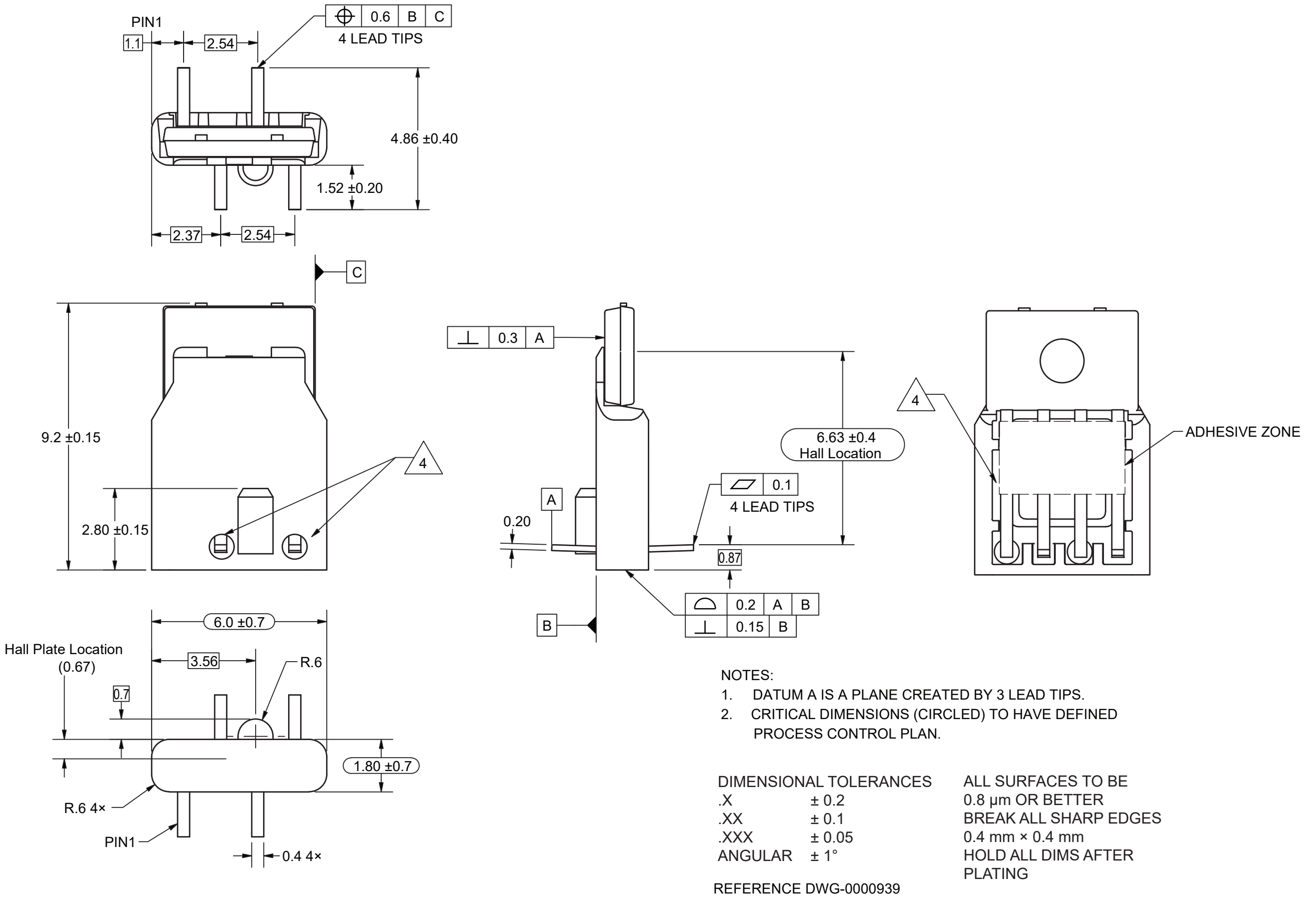
Reference EIA 481



Reference EIA 481

Figure 13: KT Package, TG Leadform, Packing Information (For Reference Only; Not For Tooling Use)

KT Package, TY Leadform



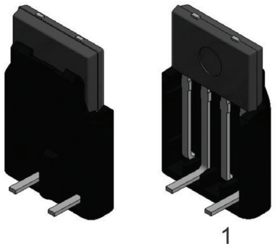
NOTES:
1. DATUM A IS A PLANE CREATED BY 3 LEAD TIPS.
2. CRITICAL DIMENSIONS (CIRCLED) TO HAVE DEFINED PROCESS CONTROL PLAN.

DIMENSIONAL TOLERANCES
.X ± 0.2
.XX ± 0.1
.XXX ± 0.05
ANGULAR ± 1°

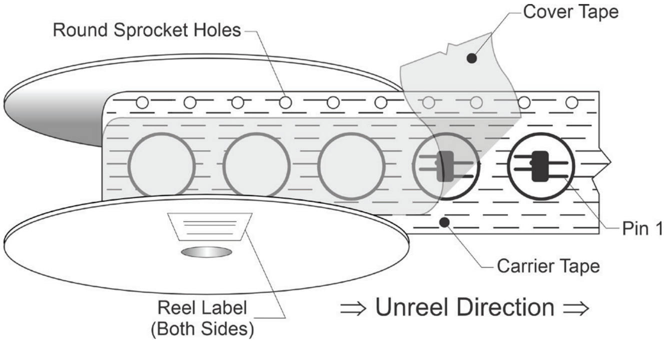
ALL SURFACES TO BE 0.8 µm OR BETTER
BREAK ALL SHARP EDGES 0.4 mm × 0.4 mm
HOLD ALL DIMS AFTER PLATING

REFERENCE DWG-0000939

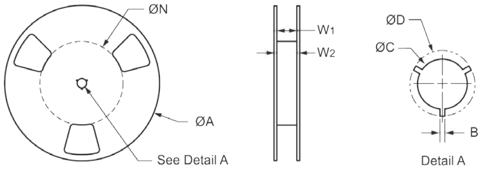
Figure 14: KT Package, TY Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 4
Through hole pins
Customer specific leadform



- Embossed tape and reel
- 250 devices per 13 in. reel
- 50 min. trailer pockets
- 120 min. leader pockets
- Pin 1 on leading device edge, opposite sprocket hole side

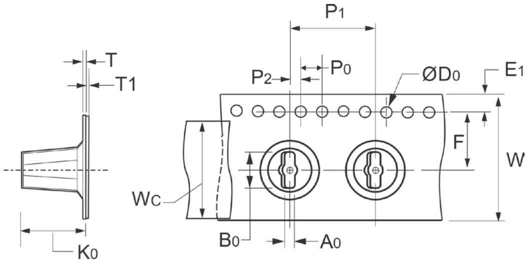


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	13 +0.5 / -0.2	20.2 (Min)	102 (Nom)
W1 (inside, at hub)		24.4 (Min)			
W2 (outside, at hub)		30.4 (Max)			

Reference EIA 481

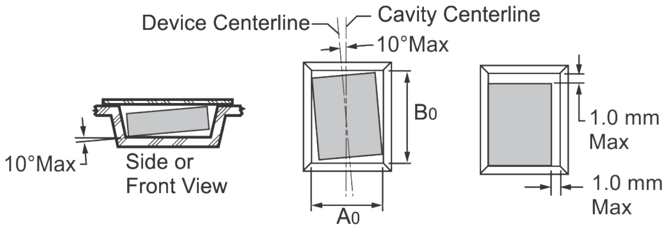


Dimensions in mm, may vary with supplier

Carrier Tape			Cover Tape
W: 24.00 ±.3 E_1: 1.75 ±.1 F: 11.50 ±.1 T: 0.50 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 16.00 ±.1 P_2: 2.00 ±.1	A_0: 2.00 B_0: 6.10 K_0: 9.50	W_C: 21.10 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

Reference EIA 481



Reference EIA 481

Figure 15: KT Package, TY Leadform, Packing Information (For Reference Only; Not For Tooling Use)

OK Package Options

OK Package, TN Leadform

For Reference Only - Not for Tooling Use

(Reference DWG-0000395)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

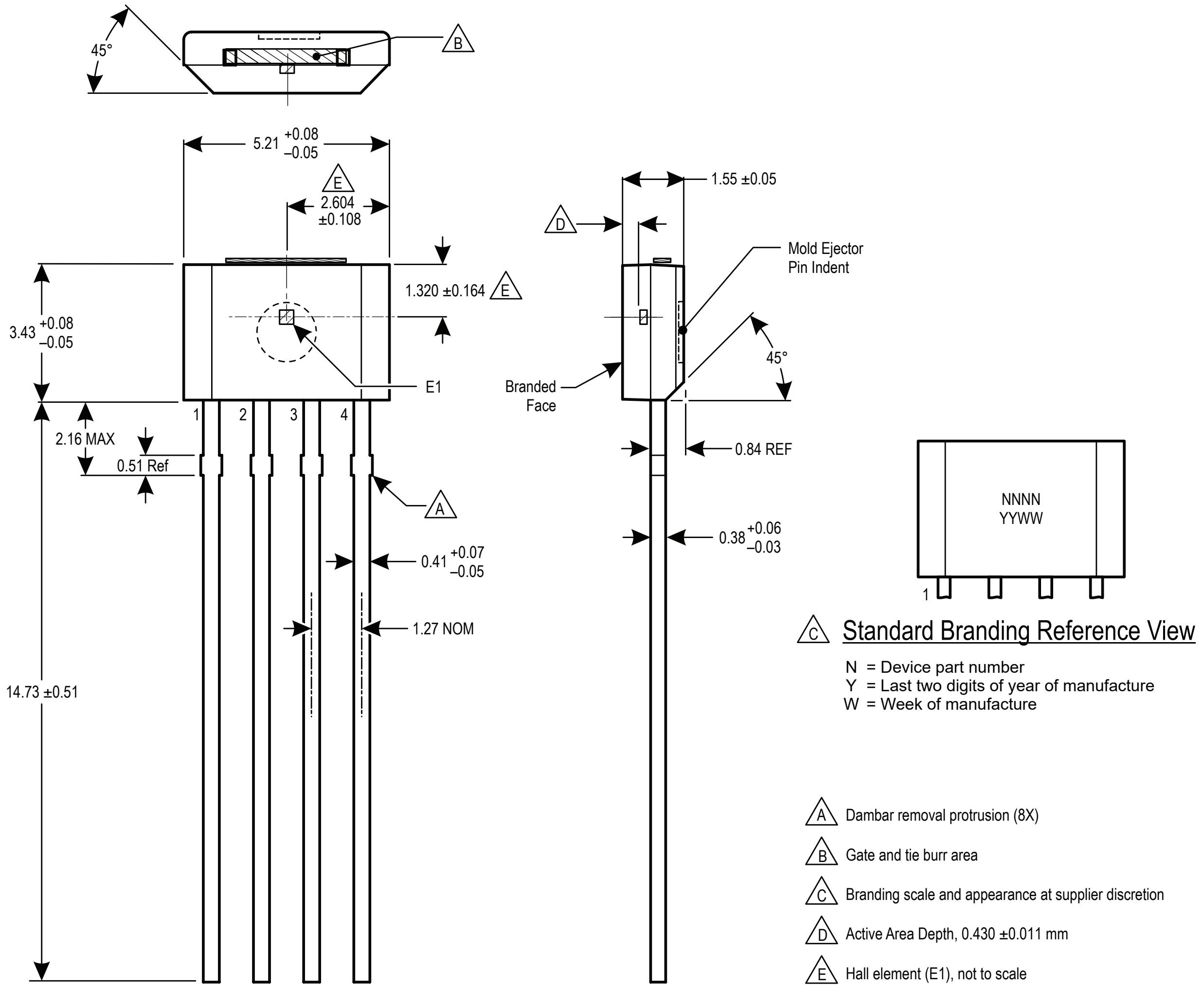
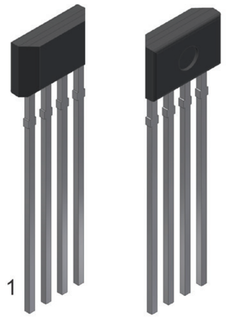
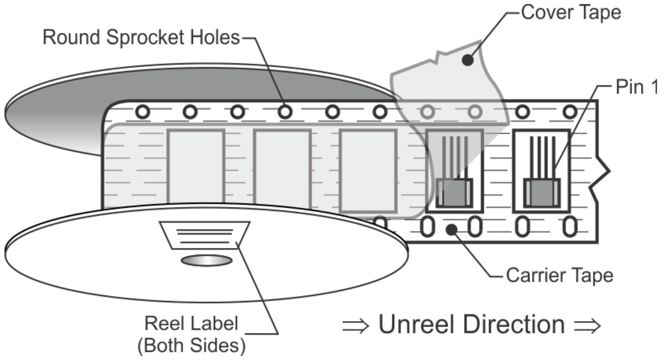
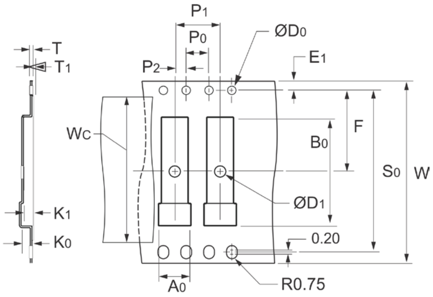


Figure 16: OK Package, TN Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 4
Straight
Untrimmed
Unformed (flat)
Non JEDEC standard





Dimensions in mm, may vary with supplier

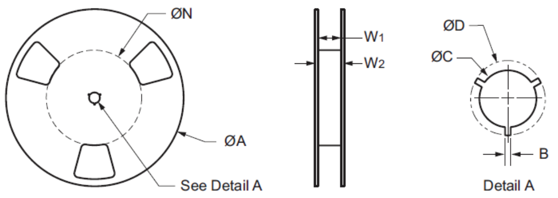
Carrier Tape			Cover Tape
W: 32.00 ±.3 E_1: 1.75 ±.1 F: 14.20 ±.15 T: 0.30 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 8.00 ±.1 P_2: 2.00 ±.15 S_0: 28.40 ±.1	A_0: 5.80 B_0: 19.20 K_0: 1.90 K_1: 1.50 D_1: 2.00 MIN	W_C: 25.50 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

Reference EIA 481

- Embossed tape and reel
- 4000 devices per 13 in. reel
- 25 min. trailer pockets
- 55 min. leader pockets

- Branded face outward
- Device body on left side
- Elongated sprocket holes on left side
- Pin 1 on leading device edge

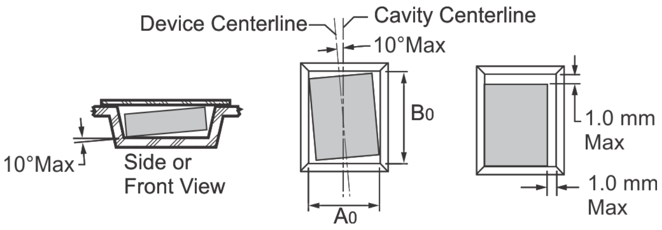


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)		32.4 (Min)			
W_2 (outside, at Hub)		38.4 (Max)			

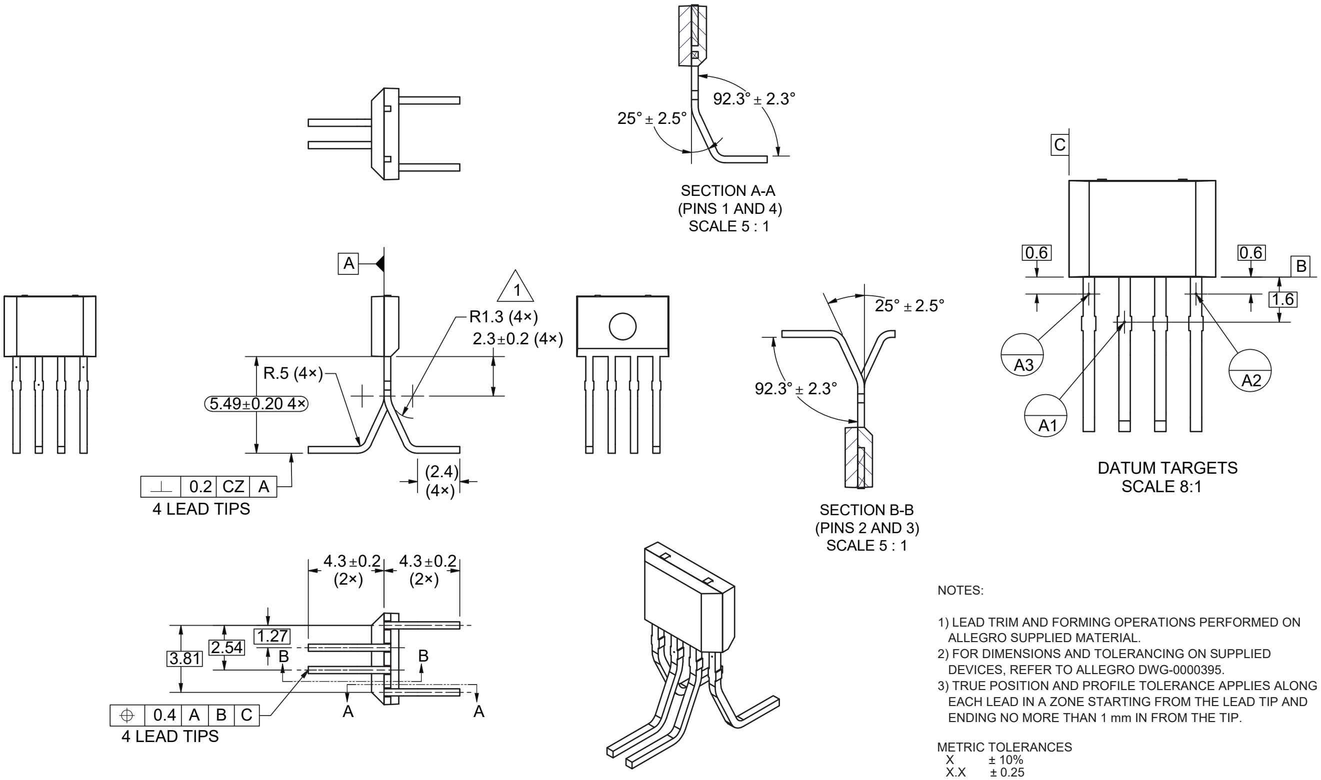
Reference EIA 481.



Reference EIA 481.

Figure 17: OK Package, TN Leadform, Packing Information (For Reference Only; Not For Tooling Use)

OK Package, TX Leadform



NOTES:

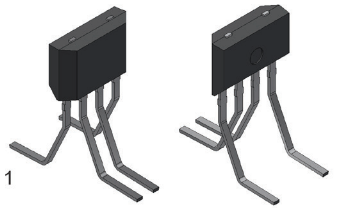
1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000395.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 1 mm IN FROM THE TIP.

METRIC TOLERANCES

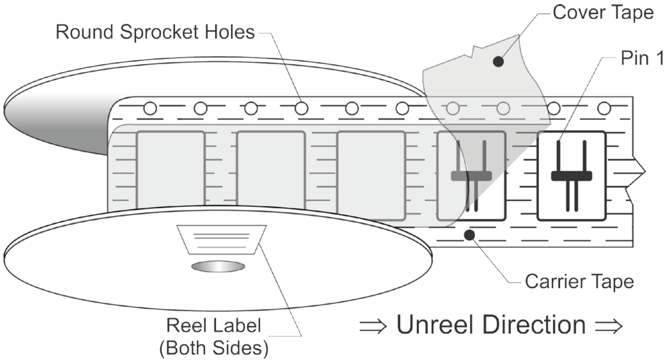
X	± 10%
X.X	± 0.25
X.XX	± 0.10
X.XXX	± 0.025
ANGULAR	± 0.5°

REFERENCE DWG-0000869, Rev. 1

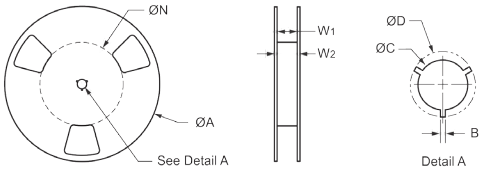
Figure 18: OK Package, TX Leadform, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 4
Through hole pins
Customer specific leadform



- Embossed tape and reel
- 450 devices per 13 in. reel
- 35 min. trailer pockets
- 100 min. leader pockets
- Pin 1 on trailing device edge, sprocket hole side

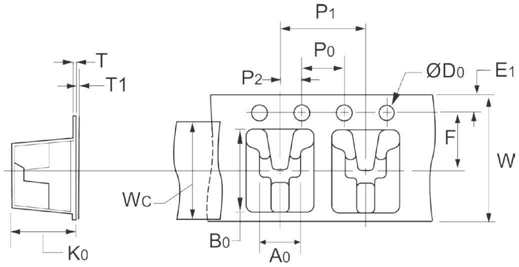


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	13 +0.5 / -0.2	20.2 (Min)	102 (Nom)
W1 (inside, at hub)			16.4 (Min)		
W2 (outside, at hub)			22.4 (Max)		

Reference EIA 481

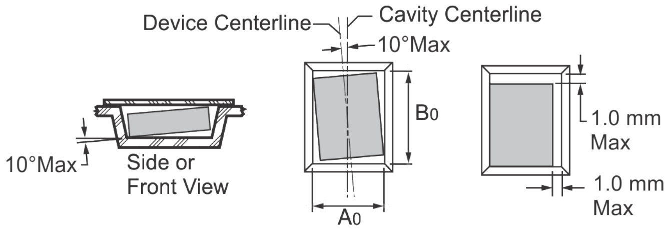


Dimensions in mm, may vary with supplier

Carrier Tape			Cover Tape
W: 16.00 ±.3 E_1: 1.75 ±.1 F: 7.50 ±.1 T: 0.50 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 12.00 ±.1 P_2: 2.00 ±.1	A_0: 4.80 B_0: 9.19 K_0: 9.50	W_C: 13.10 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

Reference EIA 481



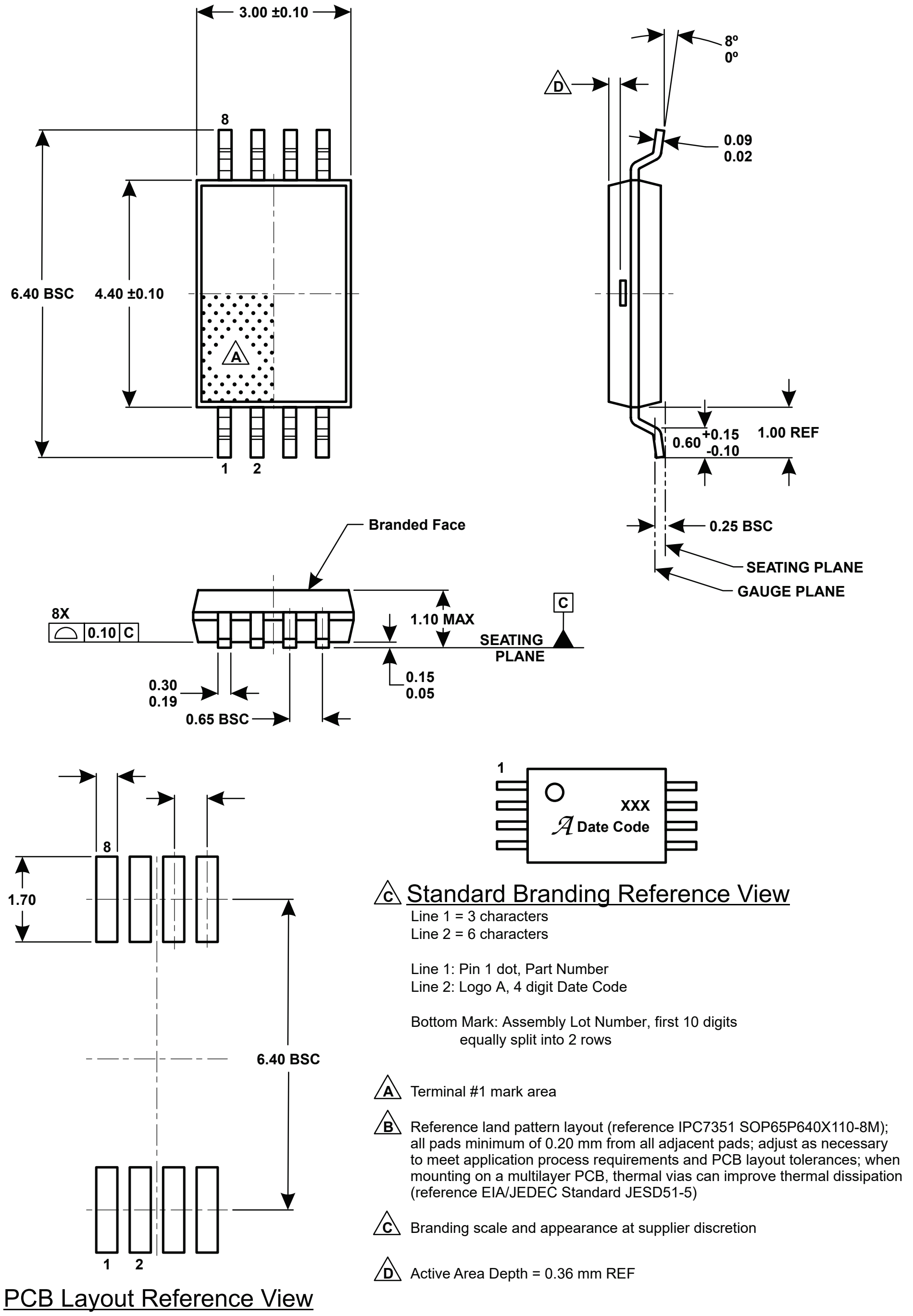
Reference EIA 481

Reference EIA 481

Figure 19: OK Package, TX Leadform, Packing Information (For Reference Only; Not For Tooling Use)

TSSOP Option

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000381, Rev. 1 and JEDED MO-153AA)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View

C Standard Branding Reference View

Line 1 = 3 characters
Line 2 = 6 characters

Line 1: Pin 1 dot, Part Number
Line 2: Logo A, 4 digit Date Code

Bottom Mark: Assembly Lot Number, first 10 digits
equally split into 2 rows

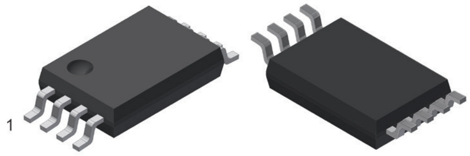
A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

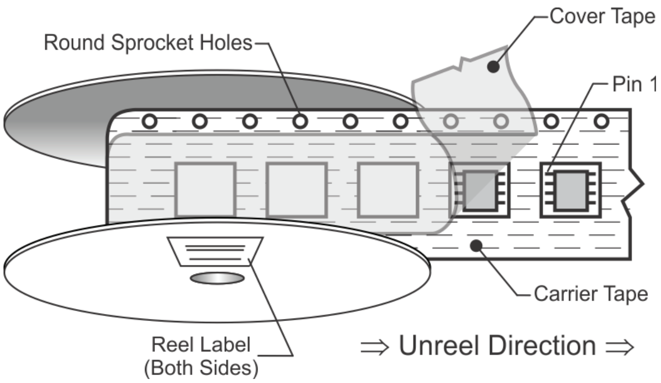
C Branding scale and appearance at supplier discretion

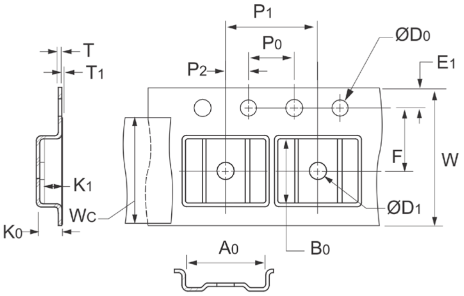
D Active Area Depth = 0.36 mm REF

Figure 20: 14-Pin TSSOP, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 8
Gull-wing
JEDEC: MO-153AA





Dimensions in mm, may vary with supplier

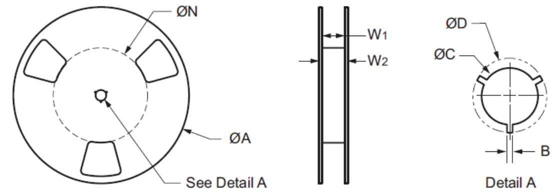
Carrier Tape			Cover Tape
W: 12.00 ±.1 E_1: 1.75 ±.1 F: 5.50 ±.05 T: 0.30 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 8.00 ±.1 P_2: 2.00 ±.05	A_0: 6.80 B_0: 3.40 K_0: 1.50 K_1: 1.15 D_1: 1.50 MIN	W_C: 9.1 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

Reference EIA 481

- Embossed tape and reel
- 4000 devices per 13 in. reel
- 50 min. trailer pockets
- 55 min. leader pockets

- Branded face outward
- Pin 1 on trailing device edge, sprocket hole side

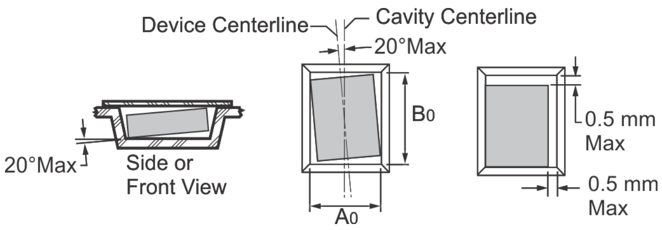


Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)		12.4 (Min)			
W_2 (outside, at Hub)		18.4 (Max)			

Reference EIA 481

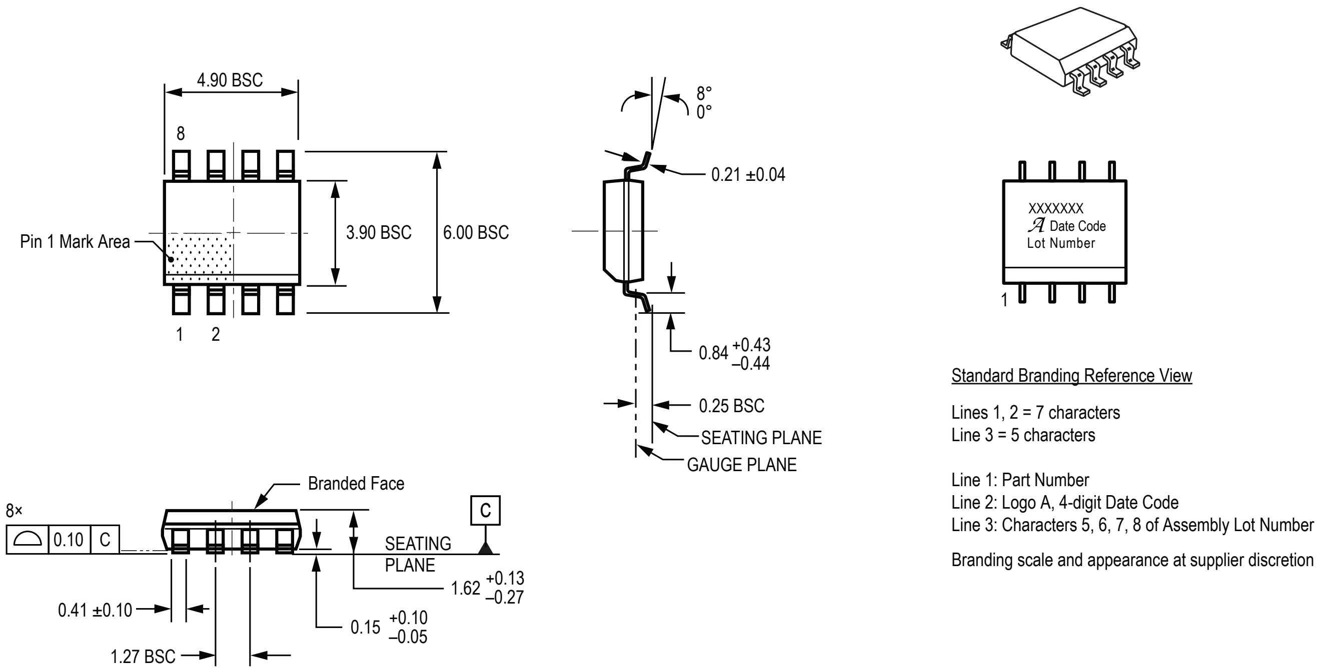


Reference EIA 481

Figure 21: LE Package, 8-Pin TSSOP, Packing Information (For Reference Only; Not For Tooling Use)

SOIC-8 Package Option

For Reference Only; not for tooling use (reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



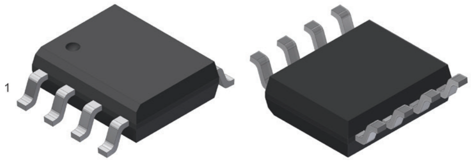
Standard Branding Reference View

Lines 1, 2 = 7 characters
Line 3 = 5 characters

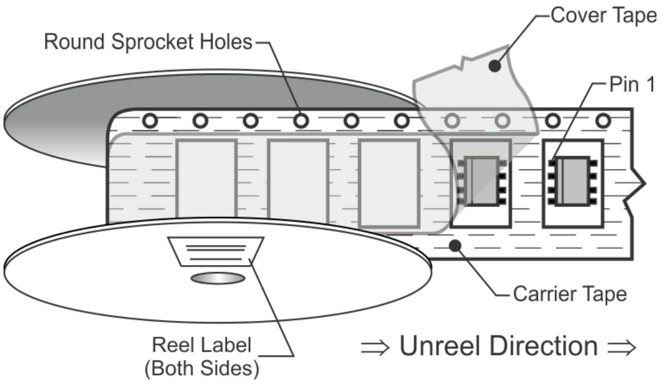
Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

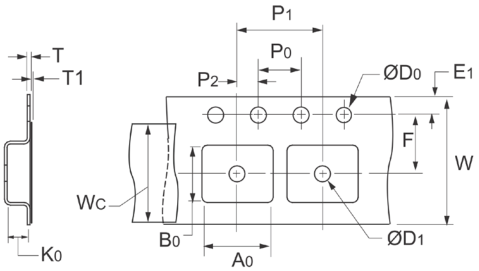
Branding scale and appearance at supplier discretion

Figure 22: OL Package, 8-Pin SOIC, Package Outline Drawing (For Reference Only; Not For Tooling Use)



Terminals: 8
Gull-wing pins
Narrow body
SOIC8
JEDEC MS-012 AA





Dimensions in mm, may vary with supplier

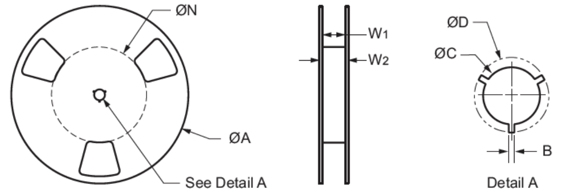
Carrier Tape			Cover Tape
W: 12.00 ±.1 E_1: 1.75 ±.1 F: 5.5 ±.05 T: 0.30 (0.6 MAX)	D_0: 1.50 +.1/-.0 P_0: 4.00 ±.1 P_1: 8.00 ±.1 P_2: 2.00 ±.05	A_0: 6.7 B_0: 5.4 K_0: 2.1 D_1: 1.5 MIN	W_C: 9.1 T_1: 0.061 (0.1 MAX)

1. Pocket centerlines to cavity center, not to pocket detection hole.
2. A_0 and B_0 measured 0.3mm above bottom of pocket.

Reference EIA 481

- Embossed tape and reel
- 3000 devices per 13 in. reel
- 25 min. trailer pockets
- 55 min. leader pockets

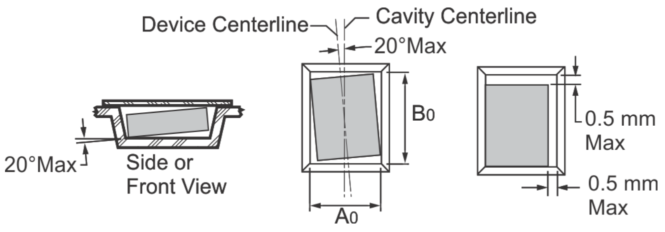
- Branded face outward
- Pin 1 on trailing device edge, sprocket hole side



Access hole and hub configuration may vary at supplier discretion within limits shown

Dimensions in mm

Type	A	B	C	D	N
Plastic 13 in.	330 (Nom)	1.5 (Min)	$13^{+0.5}_{-0.2}$	20.2 (Min)	102 (Nom)
W_1 (inside, at Hub)			12.4 (Min)		
W_2 (outside, at Hub)			18.4 (Max)		



Reference EIA 481

Reference EIA 481

Figure 23: OL Package, 8-Pin SOIC, Packing Information (For Reference Only; Not For Tooling Use)

Revision History

Number	Date	Description	Responsibility
–	March 11, 2026	Initial release to the Allegro website	F. Kulla