THE CRITICAL ROLE OF CAPACITOR DERATING IN BOOTSTRAP CIRCUITS

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ABSTRACT

This application note investigates the impact of capacitor derating on the performance and reliability of a bootstrap circuit within an automotive motor-drive systems, specifically using the Allegro AMT49100 high-voltage gate driver. While multilayer ceramic capacitors (MLCCs) are the standard choice for bootstrap components due to their low equivalent series resistance (ESR) and compact size—under DC bias, temperature extremes, and aging—their effective capacitance can decrease significantly, often by more than 70%. This reduction can compromise the floating supply voltage, leading to bootstrap undervoltage lockout (UVLO) faults, incomplete MOSFET enhancement, and system instability. This document provides a comprehensive analysis of these derating mechanisms and outlines a robust design methodology for selecting bootstrap capacitors that maintain sufficient charge reserves in all operating conditions, ensuring the safe and reliable operation of the AMT49100 in safety-critical applications.

INTRODUCTION

Modern automotive motor-control applications often use three-phase brushless DC (BLDC) motors and permanent-magnet synchronous motors (PMSMs). To drive these motors efficiently, high-voltage gate drivers like the Allegro AMT49100 are used to control external N-channel MOSFETs in a three-phase bridge configuration. [1]

The high-side N-channel MOSFETs must be fully enhanced to achieve a low on-resistance ($R_{DS(ON)}$). To achieve this, the gate voltage must be driven significantly greater than the system supply voltage (V_{BB}), effectively "floating" above the main power rail. The most common and cost-effective method to generate this floating supply is the bootstrap circuit, which consists of a bootstrap diode and a bootstrap capacitor.

The bootstrap capacitor acts as a stable energy reservoir, supplying the necessary charge to turn on the high-side MOSFET and maintain the gate-source voltage during the entire duration of the on state. Designers typically use a simple approach to select this capacitor, whereby the design ensures that this capacitance (C_{BOOT}) significantly exceeds (e.g., 10× to 20×) the MOSFET gate capacitance (C_{GATE}).

However, this simplified approach often fails to account for the nonideal characteristics of MLCCs, specifically the Class 2 dielectrics (such as X7R and X5R) commonly used in these applications. These capacitors exhibit DC bias derating, where the effective capacitance reduces drastically as the applied DC voltage increases. For a gate driver operating with a 12 V regulator supply, a nominal 100 nF capacitor might effectively provide only 20 nF to 30 nF of capacitance. This significant reduction in charge storage can lead to severe consequences for the AMT49100 gate driver, including:

- **Bootstrap undervoltage lockout (UVLO):** During the high-side on-time of the gate driver, the floating supply voltage (V_{BOOT}) might reduce to less than the UVLO threshold, causing the driver to turn off the MOSFET to protect the system.
- **Increased power dissipation:** If the gate voltage reduces but does not reach the UVLO trip point, the MOSFETs might operate in their linear region with higher ($R_{DS(ON)}$), leading to excessive thermal stress.
- **Motor operation instability:** Intermittent faults lead to gate-driver turn-off. During operation, this might result in an overcurrent event and overall control instability.

This application note details the mechanisms of capacitor derating, specifically focusing on DC bias, temperature, and aging effects. It provides a robust design methodology for selecting the appropriate bootstrap capacitor to ensure the Allegro AMT49100 operates reliably in all automotive conditions.

[1] AMT49100, 80 V Automotive Three-Phase MOSFET Driver, Allegro MicroSystems Datasheet, Rev. 6, March 31, 2025.

BOOTSTRAP CIRCUIT OPERATION [2]

The bootstrap circuit generates the floating supply voltage (V_{BOOT}) required to drive the high-side N-channel MOSFET using a simple diode-capacitor network, as shown in Figure 1. The charging and discharging operation are as follows:

- **Charging phase:** When the low-side MOSFET is in the on state, the switch node is grounded, allowing current to flow from the logic supply (V_{REG}) through the bootstrap diode (D_{BOOT}) to charge the C_{BOOT}. This stage is indicated in green in Figure 1.
- **Discharging phase:** Upon turn-on of the high-side MOSFET, the switch node rises (V_S) to the supply voltage. The diode (D_{BOOT}) becomes reverse-biased, isolating the bootstrap capacitor (C_{BOOT}), which then acts as the sole energy reservoir for the high-side gate driver. This stage is indicated in red in Figure 1.

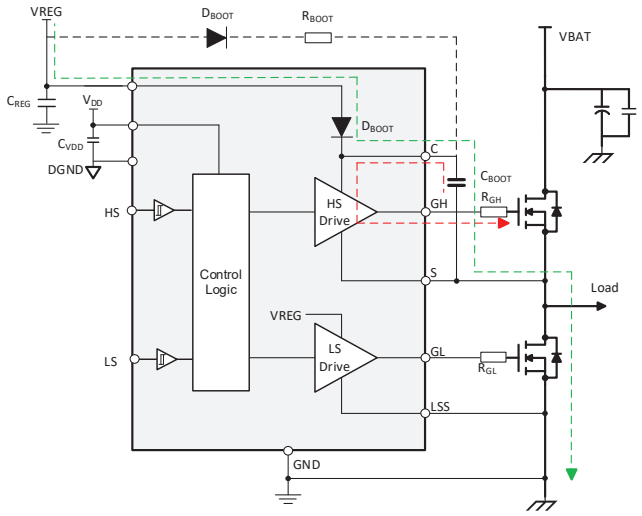

Figure 1: Typical Bootstrap Circuit for a High-Side Gate Driver

To prevent unintended UVLO faults, the bootstrap capacitor (C_{BOOT}) must be sized to supply the total required charge (Q_{Total}) without its voltage reducing to less than the UVLO threshold of the driver. The minimum effective capacitance ($C_{BOOT\,(Min.)}$) required is calculated as:

Equation 1:

$$C_{BOOT\,(Min.)} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where, Q_{Total} is calculated as:

Equation 2:

$$Q_{Total} = Q_G + (I_{LEAK} + I_{QBS} + I_R) \times t_{ON(Max)}$$

and ΔV_{BOOT} is represented as:

Equation 3:

$$\Delta V_{BOOT} = V_{REG} - V_{fBOOT} - V_{BCON}$$

where:

- Q_G is the gate charge of the MOSFET
- I_{LEAK} is the gate leakage current of the MOSFET
- I_{QBS} is the bootstrap circuit quiescent current
- $t_{on(max)}$ is the maximum turn-on time of the MOSFET
- V_{BCON} is the rising threshold of the bootstrap undervoltage
- V_{REG} is the regulator supply voltage
- V_{BOOT} is the bootstrap diode drop
- I_R is the reverse leakage current

It is critical to note that the value calculated above represents the minimum effective capacitance required at the operating DC bias point. As detailed in the sections that follow, to account for DC bias derating effects, the nominal capacitor value selected must be significantly greater.

[2] Content in this section was generated using Allegro artificial intelligence; all material was verified by the authors, March 2026.

CAPACITOR CLASSIFICATION [2]

This section presents the different types of MLCCs available on the market. The industry standard (IEC 60384) categorizes these into classes based on their dielectric materials and temperature stability:

- **Class 1 (temperature compensating)** comprises Code 0, G (C0G; also termed negative-positive-zero, NP0) MLCCs. This is the most commonly used type of capacitor. This type of capacitor uses paraelectric materials, such as titanium dioxide (TiO_2), that are extremely stable and exhibit negligible change in capacitance with voltage, time, or temperature. However, the relatively low dielectric constant (ε_r) of this type of capacitor results in low capacitance per unit volume. Therefore, this type of capacitor is predominantly used for accurate timings in radio-frequency (RF) circuits. [3] In a design, system size requirements that result from system cost goals typically limit the practical application of this type of capacitor; for a bootstrap supply, it is generally not viable.
- **Class 2 (high dielectric constant):** X7R, X5R, X7S, and X7T materials are the most used Class 2 capacitors. A capacitor of this type uses ferroelectric materials, such as barium titanate ($BaTiO_3$), which has a very high dielectric constant (ε_r). This allows for a high capacitance value in a compact package and thereby allows use of this type of capacitor in applications that require a high capacitance, such as the bootstrap capacitor. [4]

  However, Class 2 capacitors are chemically sensitive to operating conditions: They exhibit significant capacitance changes due to DC bias, temperature, and aging. Nonetheless, this type of capacitor is preferred due to its cost-effectiveness and smaller size. [4]

  Class 2 capacitors are identified by a three-character code (e.g., X7R) that defines the operating temperature range and capacitance-stability limits. The IEC temperature codes for Class 2 capacitors are summarized in Table 1.

Table 1: IEC Temperature Codes

1st Letter (Min. Temp)	2nd Letter (Max. Temp)	3rd Letter (Max. Cap. Change)
X = –55°C Y = –30°C Z = 10°C	5 = 85°C 6 = 105°C 7 = 125°C 8 = 150°C	R = ±15% S = ±22% T = +22%/–33% U = +22%/–56% V = +22%/–82%

CAPACITOR DERATING [2]

The nominal value of a Class 2 MLCC is measured in very specific conditions that are not realistic in actual application; i.e., it is typically measured at 0 V DC bias, 25°C, and with a small AC signal. As soon as the capacitor is placed in a bootstrap regulator supply, its effective capacitance begins to reduce. The primary factors that cause this degradation are discussed next.

DC Bias Derating

The capacitance of a parallel plate capacitor is governed by the fundamental equation:

Equation 4:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where:

- ε_0 is the permittivity of free space (constant).
- ε_r is the relative permittivity (i.e., dielectric constant) of the material.
- A is the overlap area of the internal electrodes.
- d is the dielectric thickness between layers.

In a Class 2 dielectric material (such as $BaTiO_3$), the relative permittivity is not constant; rather, it is a function of the applied electric field as follows:

- **At 0 V bias,** the internal dipoles are free to rotate and align with the AC signal, resulting in a very high ε_r (typically 2000 to 4000) and, thus, a high nominal capacitance, as shown in Figure 2.
- **At high DC bias,** the strong DC electric field "locks" or saturates the dipole domains in a fixed direction. Because the dipole domains are already aligned with the DC field, they cannot rotate further to store charge from the AC signal, as shown in Figure 3. This saturation causes the dielectric constant (ε_r) to reduce and effectively reduces the capacitance, as shown in Equation 4. When the component is operated near its rated voltage, it is very common for the effective dielectric constant (ε_r) to reduce by 50% to 80%. [5][6]

[3] IEC 60384-21, Fixed capacitors for use in electronic equipment – Part 21: Sectional specification: Fixed surface mount multilayer capacitors of ceramic dielectric, Class 1, IEC Standard, June 21, 2024.

[4] IEC 60384-21, Fixed capacitors for use in electronic equipment – Part 22: Sectional specification: Fixed surface mount multilayer capacitors of ceramic dielectric, Class 2, IEC Standard, June 21, 2024.

[5] SimSurfing Tool, DC Bias Characteristics of MLCCs, Online Tool, Murata Manufacturing Co., Ltd.

[6] Frank Puhane, SN011: Why does the capacitance of MLCCs change? Aging, Application Note, Würth Elektronik, Apr 29, 2024.

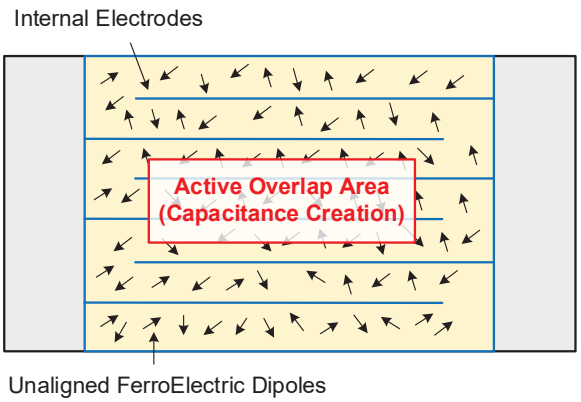

Figure 2: Basic MLCC Construction (No Bias)

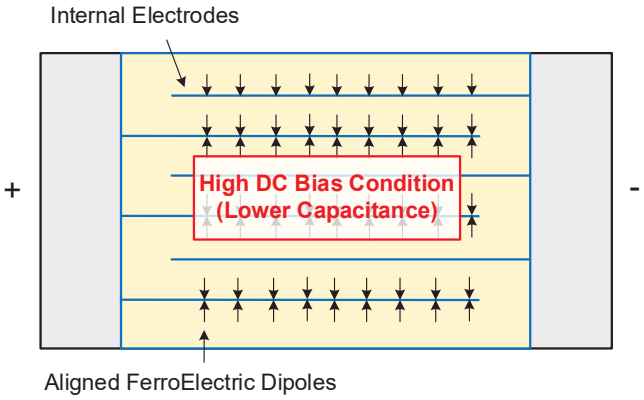

Figure 3: Dielectric Dipoles at High DC Bias

The magnitude of capacitance loss is also dependent on the specific Class 2 dielectric formulation. An X5R capacitor is designed to achieve the maximum density and therefore uses thinner dielectric layers. This type of capacitor results in greater electric field stress (V/m) and rapid dipole saturation. Conversely, an X7R capacitor is optimized for stable operation across a wider temperature range and therefore has a lower capacitance derating. As shown in Figure 4, the derating of X7R [7] is generally lower than that of the X5R [8] capacitor; however, the overall derating of both is significant when the DC bias approaches the rated voltage.

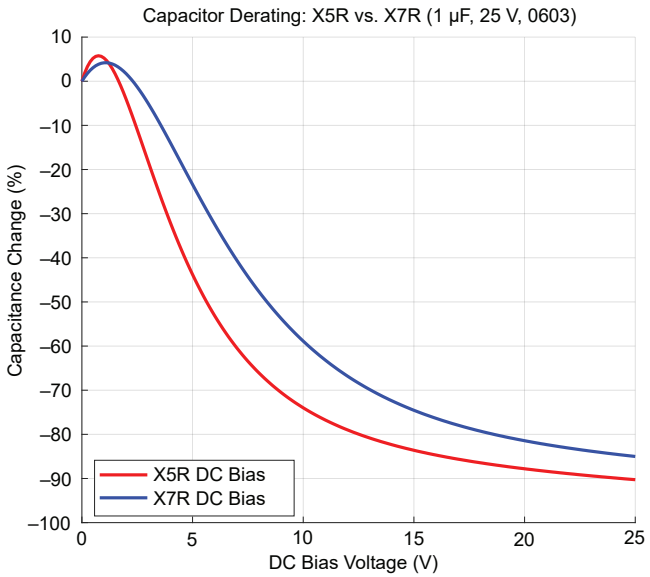

Figure 4: DC Bias Effect on X5R and X7R Capacitors [5]

[7] GRM188R71E105MA49 (X7R), Chip Monolithic Ceramic Capacitor for General, muRata Datasheet.
[8] GRM185R61E105MA12 (X5R), Chip Multilayer Ceramic Capacitors for Consumer Electronics & Industrial Equipment, muRata Datasheet.

Package Size Impact

The physical volume of the capacitor is a critical factor in DC bias performance, driven by the electric field strength ($E = V/d$). A reduced capacitor size requires thinner dielectric layers (d). This thinner barrier results in a much stronger electric field (E) for the same operating voltage (V), leading to rapid dipole saturation and a more-severe loss of capacitance. [9]

For example, as illustrated in Figure 5, for the same capacitance and voltage rating, a 1206 package [10] has a better (lower) DC bias derating characteristic than a 0805 package. [11] Moreover, the 0603 package [12] is further degraded to nearly 70% of its capacitance at 12 V. This confirms that, to mitigate bias effects, a key strategy is to increase the package volume. Therefore, the most effective strategy to achieve better bootstrap circuit performance is often to sacrifice printed circuit board (PCB) space for a larger package.

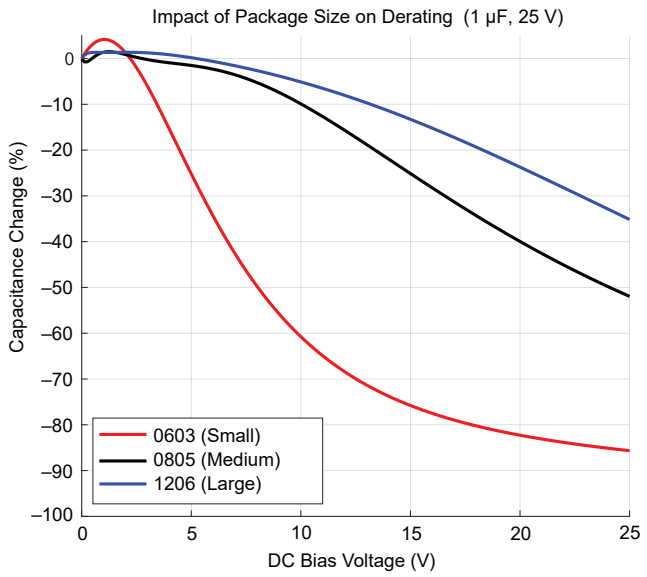

Figure 5: Capacitor Derating for Different Package Sizes [5]

Temperature Derating

The capacitance of an MLCC varies with temperature, as defined in Table 1. For example, an X7R capacitor is specified to maintain its capacitance within ±15% of the nominal value over its operating temperature range of –55°C to 125°C. The overall variation of the capacitance with temperature is not as severe as the DC bias derating; however, the design must account for this variation, especially in applications with wide operating temperature ranges. [9]

Aging (Long-Term Degradation)

The dielectric material in a Class 2 MLCC experiences a gradual, logarithmic decrease in capacitance over time. This phenomenon is known as aging. The rate of degradation is specified in percent per decade-hour (e.g., 2% to 5% per decade). This means that, after 1,000 hours, the reduction in capacitance can be a few percent; and, in subsequent logarithmic time intervals, capacitance continues to reduce. This impact is smaller, but it adds to the total capacitance loss over the lifetime of the product. [13]

By incorporating all these factors, designers can select the initial design margin before capacitors are selected.

[9] Simon Cen, DC Bias Characteristics of Ceramic Capacitors, Technical Paper, KYOCERA AVX Components Corporation, Feb 22, 2023.
[10] GRM31MR71E105 (package: 1206), Chip Multilayer Ceramic Capacitors for Consumer Electronics & Industrial Equipment, muRata Datasheet.
[11] GCJ21BR71E105 (package: 0805), Soft Termination Chip Multilayer Ceramic Capacitors for Automotive Powertrain/Safety Equipment, muRata Datasheet.
[12] GRT188R71E105 (package: 0603), AEC-Q200 Compliant Chip Multilayer Ceramic Capacitors for Infotainment, muRata Datasheet.
[13] TDK Corporation, Capacitors Part 3: Ceramic Capacitors (DC Bias Characteristics), TDK Electronics ABC, Tech Library.

EXPERIMENTAL VERIFICATION

To validate the theoretical impact of DC bias derating on system reliability, bench testing was performed using the Allegro AMT49100 high-voltage gate driver. The objective was to quantify the actual effective capacitance (C_{EFF}) of various X7R MLCCs under real-world operating conditions and to determine the specific load points where bootstrap UVLO faults occur.

The test setup consisted of an AMT49100 configured to drive a simulated high-side load. A variable resistive load was applied in parallel with the gate-source of the high-side MOSFET to simulate the total current draw ($I_{total} = I_{QBS} + I_{LEAK}$). The voltage reduction (ΔV) across the bootstrap capacitor was captured during a fixed discharge duration (t_{ON}), and the bootstrap circuit was stressed by increasing the load current until the AMT49100 triggered a V_{BS} undervoltage fault (UVLO). This test compares the robustness of capacitors with identical nominal values but different voltage ratings.

As shown in Figure 6, the 100 nF/16 V capacitor causes a system fault at only 14 mA of load current, whereas the 100 nF/50 V version supports nearly double that current (26 mA) before failing. This proves that use of a capacitor rated near the operating voltage (12 V bias on a 16 V part) results in critically low energy storage, which makes the system susceptible to nuisance bootstrap UVLO tripping.

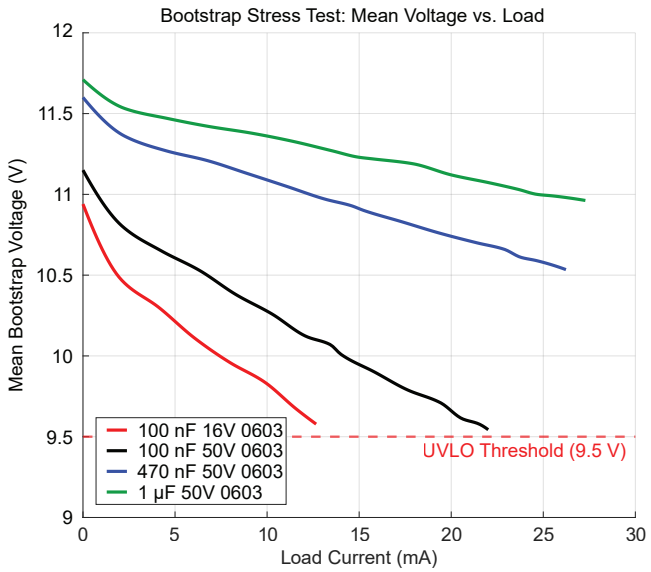

Figure 6: Maximum Load Capability Before UVLO Fault

To quantify the loss of capacitance, the voltage ripple (ΔV_{BOOT}) was measured and recorded for the process of driving only the high-side MOSFET having gate charge of 140 nC in the absence of an applied load. Measurements were recorded for varying capacitor sizes and voltage ratings. The nominal datasheet value is compared with the measured effective value at 12 V DC bias in Table 2.

Table 2: Measured Effective Capacitance vs. Package and Voltage

C (nF)	Rated VDC	Package	ΔV_{BOOT} (V)	C_{EFF} (nF)	Derating %
100	16 V	0603	2.2	63.64	36.36
100	50 V	0603	1.82	76.92	23.08
100	50 V	0805	1.86	75.27	24.73
470	50 V	0603	0.72	194.44	58.63
470	50 V	0805	0.6	233.33	50.35

Key observations based on the experimental results when the voltage rating increased from 16 V to 50 V are:

- **Voltage rating impact:** The two 100 nF/0603 capacitors recovered approximately 13 nF of capacitance (from 63.6 nF at 16 V to 76.9 nF at 50 V).
- **Capacitance vs. volume:** The most severe derating is observed in the high-value, small-package parts. The 470 nF/0603 capacitor lost more than 60% of the value reported in the datasheet (470 nF to 190 nF), whereas the 100 nF/0603 capacitor lost only 23% of the value reported in the datasheet.
- **Package size benefit:** For the 470 nF capacitor, the larger 0805 package retained significantly more capacitance (233 nF) than the smaller 0603 package (194 nF). The larger physical volume reduces the internal electric field stress for the same applied voltage.

DESIGN GUIDELINES FOR THE ROBUST BOOTSTRAP CIRCUIT [2]

To ensure robust performance, designers must mitigate the risks of the bootstrap capacitor derating. This means that designers must commit to a rigorous component selection and validation methodology, as described in the sections that follow.

Account for Entire System Demand

A robust design ensures that the bootstrap capacitor meets the peak demand of the system. The capacitor must store enough charge to fully turn on the high-side MOSFET and to supply any quiescent and leakage currents for the duration that the MOSFET is in the fully on state, without its voltage reducing to less than the undervoltage lockout (UVLO) threshold of the driver. Key parameters to consider include:

- **Total gate charge (Q_g) of the external MOSFET:** This is the primary consumer of charge from the bootstrap capacitor during each switching event.
- **PWM switching frequency:** A higher frequency results in less time for the capacitor to recharge during the duration of the on state of the low side. Thus, a higher frequency causes more stress on the bootstrap circuit.
- **Operational duty-cycle range:** The maximum high-side duty cycle is critical because it defines the minimum low-side turn-on time available for the bootstrap capacitor to be recharged through the bootstrap diode (D_{BOOT}).

Select Based on Real-World Performance

As discussed in the previous section, the bootstrap-capacitor selection must not be based on its nominal value, and the DC bias derating must be considered. The following design choices are recommended:

- **Voltage rating:** Choose a capacitor with a voltage rating that exceeds the operating bus voltage; ensure a margin of 2× to 3×. The lower internal electric field stress in the high-voltage-rated part drastically reduces the effect of the DC bias derating.
- **Package size:** For a given capacitance and voltage rating, use a physically larger package (e.g., 0805 vs. 0603). The larger package exhibits a lower percentage of capacitance loss for the same DC bias, as highlighted in previous section.
- **Dielectric material:** Consider different ceramic materials with different characteristics. While X7R is common, a material like C0G (NP0) exhibits a near-total absence of DC bias derating, albeit typically in a much smaller capacitance value.

Validate Under Real-World Conditions

Theoretical calculations provide a good starting point for capacitor requirements, but bench validation is essential to guarantee the overall system reliability. Some points to consider include:

- **Manufacturer tools:** The most critical step is to validate the effective capacitance of the chosen component in actual operating-bias-voltage conditions. Capacitor manufacturers provide powerful online tools (e.g., Murata's SimSurfing, KEMET's K-SIM) that plot the capacitance value against a DC bias voltage. These tools can provide a good derating approximation of the selected capacitor.
- **Bench measurements:** A bench measurement to confirm the bootstrap operation with the selected capacitor is essential to validate the design margin.

Implementation of these design and validation practices can ensure the bootstrap supply for the AMT49100 has sufficient energy for all operating conditions. In this way, a designer can secure the long-term safety and reliability of the entire motor-drive system.

CONCLUSION

The robustness of an automotive motor-control system, particularly one that uses a high-side gate driver like the Allegro AMT49100, is fundamentally dependent on the stability of the floating bootstrap supply. Although a bootstrap capacitor is often selected based on simple nominal calculations, this application note demonstrates that failure to account for the nonideal characteristics of Class 2 ferroelectric dielectrics can severely compromise system reliability.

Experimental verification confirms that, when subjected to typical automotive bias voltages, a standard X7R capacitor can lose a significant portion of its effective charge storage capability, often more than 60%. This substantial reduction in effective capacitance directly impacts the energy available to drive the high-side MOSFET, which thereby creates an increased risk of a bootstrap undervoltage lockout (UVLO) fault, incomplete gate enhancement, and potential thermal instability during operation.

To mitigate these risks, designers must adopt a conservative approach to component selection, beyond the datasheet nominal value. To ensure robust performance, any capacitor selected must have a voltage rating significantly greater than the operating bus voltage and a physically larger package size should be considered to minimize internal electric field stress. By validating the effective capacitance under real-world bias conditions, designers can guarantee sufficient design margin for the AMT49100 and thereby secure the long-term safety and reliability of the motor-drive system.

Revision History

Number	Date	Description	Responsibility
–	March 10, 2026	Initial release	V. Bist S. Shembekar

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