COMMON-DRAIN AND COMMON-SOURCE REVERSE-BATTERY PROTECTION SCHEMES FOR THE A89103

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ABSTRACT

In advanced automotive motor control applications—such as electric power steering (EPS), electromechanical braking, and high-power thermal management pumps—reverse battery connections pose a catastrophic threat to the three-phase inverter and sensitive control electronics. While traditional passive diodes offer basic reverse-polarity protection, their high power dissipation renders them completely unsuitable for the high-current demands of modern BLDC motor systems. An active solution—using a high-performance gate driver like the Allegro A89103 to control low-resistance N-channel MOSFETs—provides a robust, highly efficient safeguard. This application note presents a comprehensive analysis of back-to-back N-channel MOSFET topologies for implementing bidirectional blocking and reverse-battery protection with the A89103 device. The analysis focuses on both common-source and common-drain configurations, highlighting the critical addition of a protective PMOS transistor to ensure complete gate isolation during severe reverse polarity events.

INTRODUCTION

The proliferation of high-power brushless DC (BLDC) motors in automotive architectures demands highly efficient and fail-safe power management. Systems ranging from engine cooling fans to safety-critical ASIL-compliant steering and braking modules are directly connected to the main power rail of the vehicle. In these environments, simple human errors during assembly, jump-starting, or maintenance can inadvertently reverse the battery terminals.

For a standard three-phase motor inverter, a reverse-battery event is particularly disastrous. The negative voltage forward-biases the intrinsic body diodes of all six inverter MOSFETs simultaneously. Therefore, robust reverse-battery protection is a mandatory requirement to isolate the inverter from the power bus during a fault.

Traditional passive blocking diodes are entirely unsuited for these applications; at motor currents of 30 A to 100 A, the forward voltage drop of a standard diode would result in very high power loss, reducing system efficiency and requiring massive heat sinks.

To achieve high efficiency, active reverse-battery protection using low on-resistance N-channel MOSFETs is the industry standard.

The Allegro A89103 gate driver is purpose-built to manage complex motor loads and includes the necessary drive capabilities to control an active, solid-state reverse-battery protection stage. Because motor applications often require blocking current in both directions (to prevent reverse-battery damage, and to isolate a regenerative motor from overcharging the battery during a fault), a single MOSFET is insufficient. Instead, a back-to-back MOSFET configuration must be used to oppose the body diodes.

This application note provides a detailed analysis of the two ways to implement this bidirectional isolation switch using the A89103:

1. **Common-Drain (CD) Configuration:** The drain terminals of the two back-to-back MOSFETs are connected together.
2. **Common-Source (CS) Configuration:** The source terminals of the two back-to-back MOSFETs are connected together.

Both configurations use an external PMOS transistor on the gate drive line (GREV) to ensure the system remains protected and the gate driver is isolated even during extreme reverse-battery conditions.

COMMON DRAIN CONFIGURATION

The common-drain configuration uses two N-channel MOSFETs placed in series, with their drain terminals tied together at a central node. The source of the reverse FET (Q1) connects to the battery input, while the source of the bridge FET (Q2) connects to the load. This central common-drain node provides power to the A89103 by connecting directly to its VBB pin. Additionally, a protective PMOS transistor (Q6) is placed in series with the gate of the Reverse FET, as illustrated in Figure 1.

Normal Operation (CD): During standard operation, based on the schematic in Figure 1, driving the GREV pin high relative to the SREV pin causes the gate voltage of the PMOS (Q6) to drop below its source voltage. This negative gate-to-source potential

turns on Q6, establishing a path to charge the gate capacitance and fully enhance Q1. Crucially, even with this added PMOS protection circuitry, the A89103 driver maintains full, independent control over both Q1 and Q2.

The normal operation waveforms in Figure 3 demonstrate this distinct turn-on sequence, showing a smooth, controlled ramp-up of the gate-to-source voltages (V_{GS}). This independent control enables advanced system diagnostics and allows for a controlled soft-start of the capacitive DC-link to prevent massive inrush currents. Once both gates are fully enhanced, a low-impedance path is established from the battery to the load.

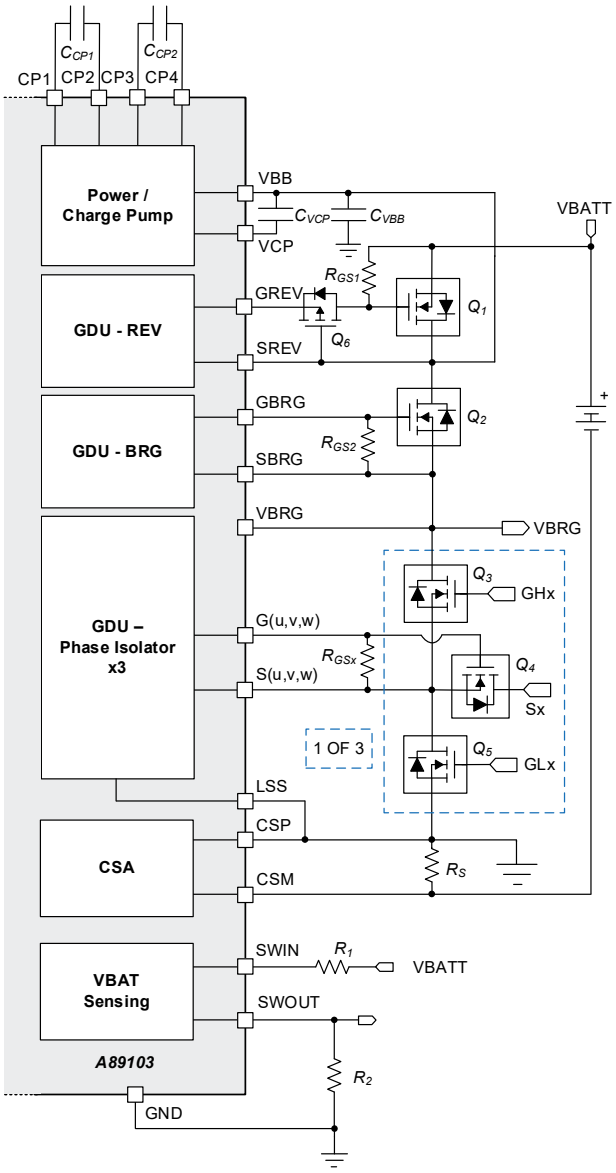

Figure 1: Schematic – Common Drain Configuration

Reverse Battery Protection Mechanism and Current Paths (CD): To fully understand this mechanism, it is critical to trace the fault currents depicted in Figure 2. During a reverse-battery event, the system ground becomes positive relative to the main supply input. The fault current attempts to flow through three distinct paths:

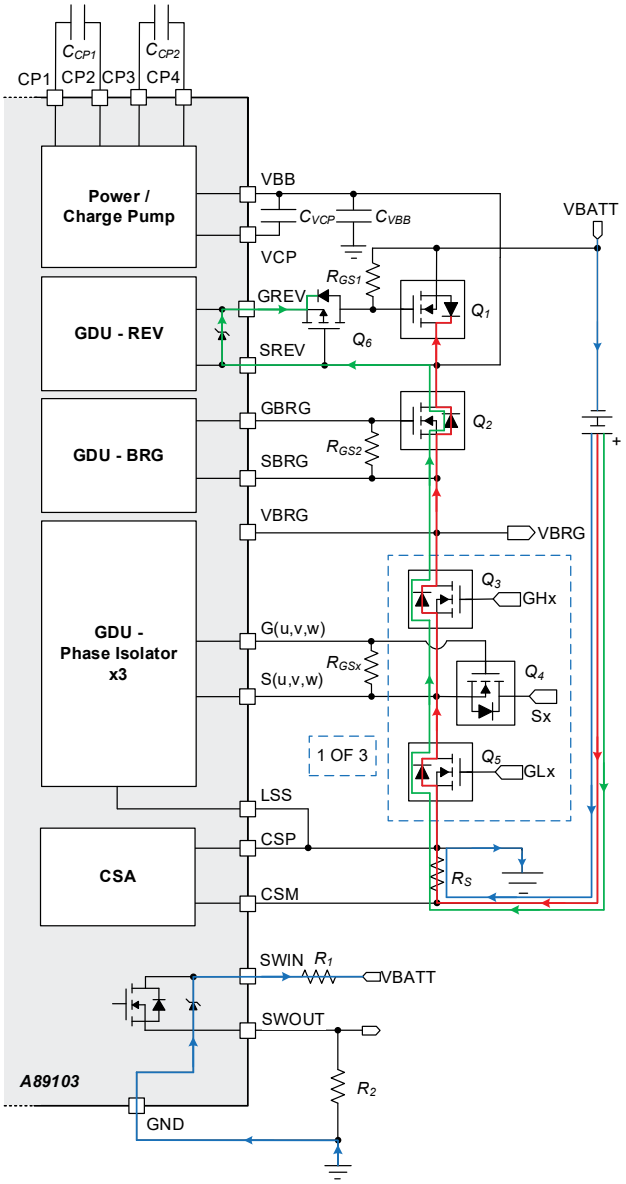

Figure 2: Schematic – Current Paths During Common Drain Reverse Battery Event

1. Blocked by the Reverse FET (Q1): As indicated by the red trace, the fault current initially flows through the downstream inverter FET diodes and passes through the forward-biased body diode of the bridge FET (Q2) to reach the common-drain

node. The current then attempts to exit toward the reversed battery terminal but is completely halted by the reverse FET (Q1). Because Q1 drain is tied to the central node and its source to the battery input, its intrinsic body diode is strongly reverse-biased against this flow, effectively isolating the inverter.

2. Internal VBAT Sensing Path (SWIN): As indicated by blue trace, a secondary fault path attempts to flow through the ground, into the A89103 internal ESD diode of the SWIN pin and out through the SWIN (switched battery input) pin. It is then connected to the negative terminal of supply through a series resistor. A properly sized series resistor at the SWIN node safely limits this reverse current.

3. Blocked by the PMOS (Q6): As indicated by the green trace, a tertiary fault path originates from the common-drain node, entering the A89103 via the SREV pin and passing through the internal gate driver ESD diode to the GREV pin. However, this path is effectively blocked by the external PMOS (Q6). This isolation prevents the reverse current from charging the gate capacitance of Q1, ensuring it does not accidentally turn on during the fault.

The effectiveness of this PMOS is captured in the fault waveforms of Figure 4, where a severe –60 V reverse transient is applied. Because the oscilloscope probe ground is referenced to the supply ground (V_{BATT}) during this test, the waveforms show all common system nodes rising with a 60 V potential relative to the negative terminal. Crucially, the gate voltage of the reverse FET (GREV_FET) is isolated by the PMOS and does not follow this rise. The gate-to-source voltage (V_{GS}) remains securely clamped below the turn-on threshold (V_{TH}). The reverse FET stays fully off, and the flat load voltage trace proves that complete reverse battery protection is achieved.

Figure 3: Waveform – Common Drain Configuration

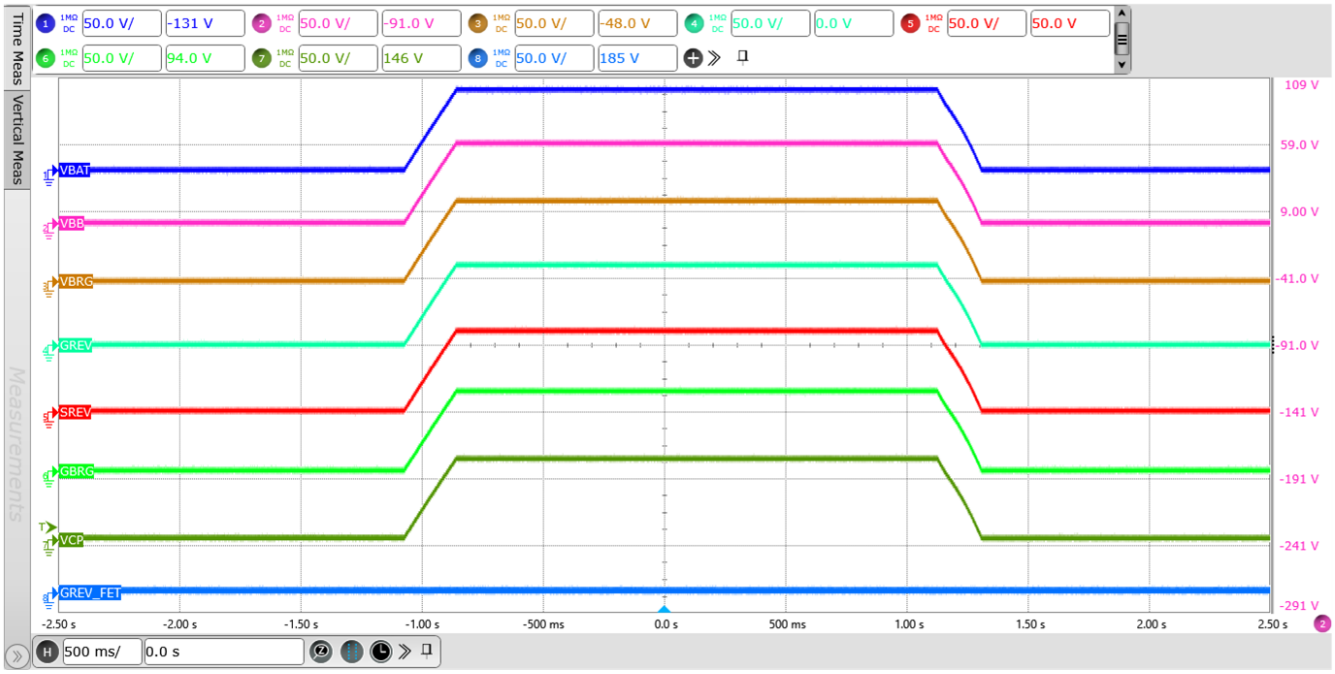

Figure 4: Waveform – Common Drain Reverse Battery Event

COMMON-SOURCE CONFIGURATION

The common-source configuration uses two N-channel MOSFETs placed in series, with their source terminals tied together at a central, floating node. In this arrangement, the drain of the Bridge FET (Q1) connects to the battery input, while the drain of the reverse FET connects to the load. This central common-source node serves as the shared reference point for the gate drive (SREV). To ensure continuous power to the A89103 IC across all operating modes, the main supply (V_{BB}) is provided by ORing the battery voltage (V_{BATT}) and the bridge voltage (V_{BRG}). Additionally, a protective PMOS transistor (Q6) is placed in series with the gate of the reverse FET, as illustrated in Figure 5.

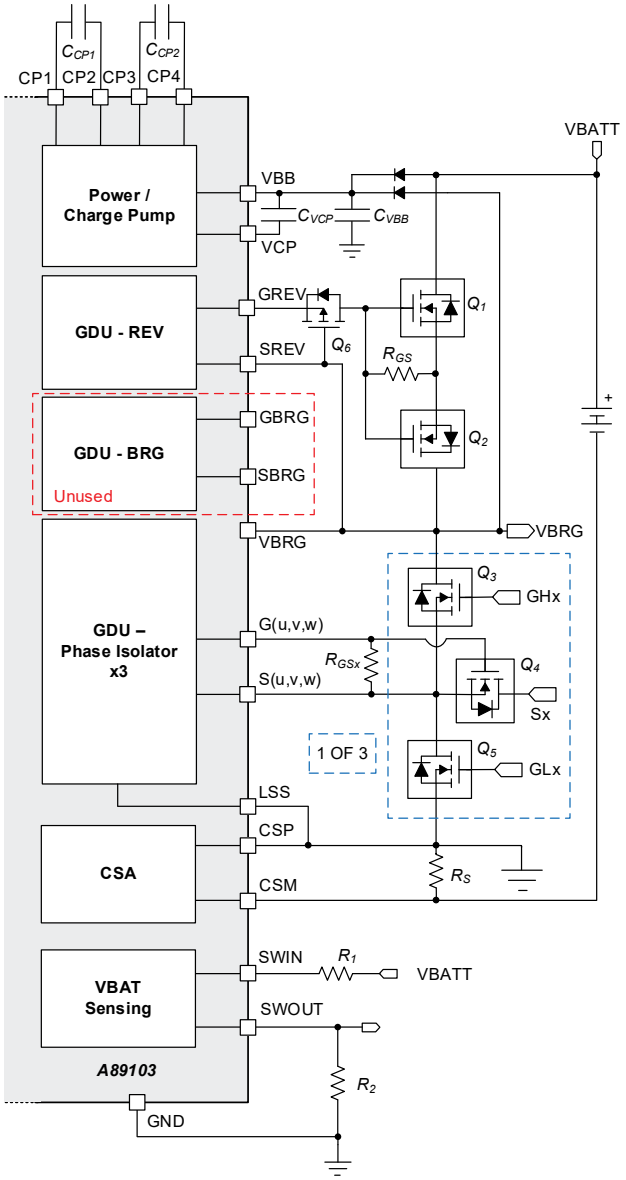

Figure 5: Schematic – Common-Source Configuration

Normal Operation (CS): The normal operation waveforms in Figure 7 demonstrate this synchronized turn-on sequence, showing a smooth, clean ramp-up of the gate-to-source voltages (V_{GS}). Unlike the independent control in the common-drain setup, the common-source configuration typically turns on both the reverse FET (Q1) and the bridge FET (Q2) simultaneously. This synchronized switching still enables a controlled soft-start of the capacitive DC-link to prevent massive inrush currents. Once both gates are fully enhanced, a highly efficient, low-impedance path is established from the battery to the load.

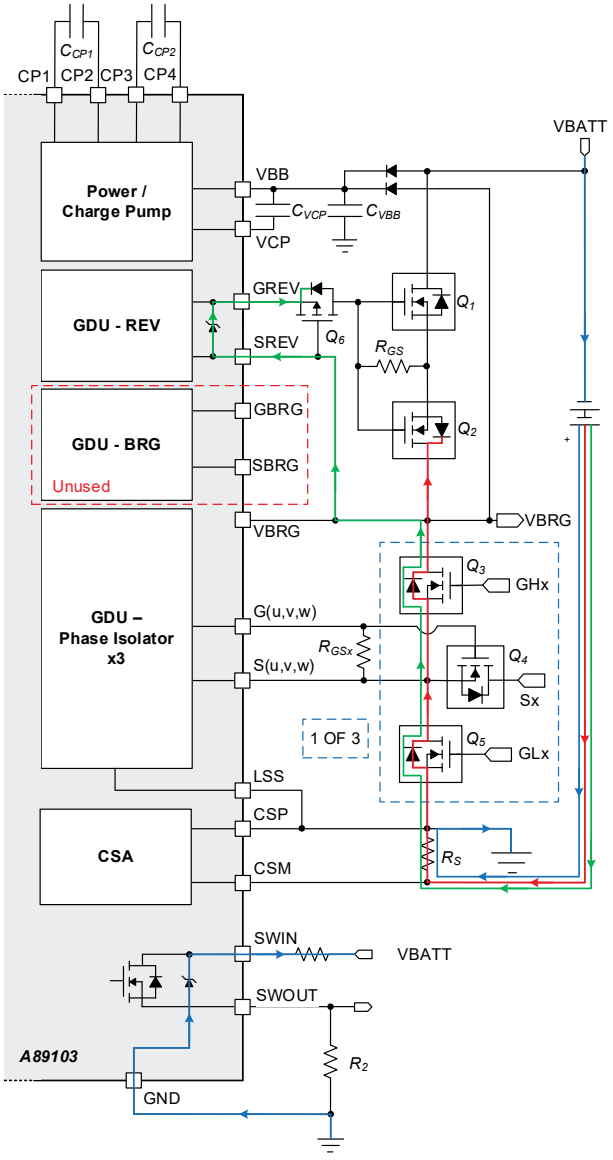

Figure 6: Schematic – Current Paths During Common-Source Reverse-Battery Event

Reverse Battery Protection Mechanism and Current Paths (CS): To fully understand this mechanism, it is critical to trace the fault currents depicted in Figure 6. During a reverse-battery event, the system ground becomes positive relative to the main supply input. The fault current attempts to flow through three distinct paths:

1. Blocked by the Reverse FET (Q1): As indicated by the red trace, the primary reverse current initially flows from the ground through the downstream inverter FET diodes and attempts to enter the drain of the reverse FET. However, it is completely halted here. Because the reverse FET drain is connected to the load and its source is tied to the central node, its intrinsic body diode is strongly reverse-biased against this flow, effectively isolating the central node and the battery from the inverter.

2. Internal Sensing Path (SWIN): As indicated by the blue trace, a secondary fault path attempts to flow through the ground, into the A89103 internal ESD diode of the SWIN pin and out through the SWIN (switched battery input) pin. It is then connected to the negative terminal of supply through a series resistor. A properly sized series resistor at the SWIN node safely limits this reverse current.

3. Blocked by the PMOS (Q6): As indicated by the green trace, a tertiary fault path originates from the common-source node, entering the A89103 via the SREV pin and passing through the internal gate driver ESD diode to the GREV pin. However, this path is effectively blocked by the external PMOS (Q6). This isolation prevents the reverse current from charging the gate capacitance of the reverse FET, ensuring it does not accidentally turn on during the fault.

The effectiveness of this PMOS is captured in the fault waveforms of Figure 8, where a severe –60 V reverse battery is applied. Because the oscilloscope probe ground is referenced to the supply ground (V_{BATT}) during this test, the waveforms show all common system nodes rising with a 60 V potential relative to the negative terminal. Crucially, the gate voltage of the reverse FET (GREV_FET) is isolated by the PMOS and does not follow this rise. The gate-to-source voltage (V_{GS}) remains securely clamped below the turn-on threshold (V_{TH}). This proves that reverse-battery voltage protection is achieved.

Figure 7: Waveform – Common-Source Configuration

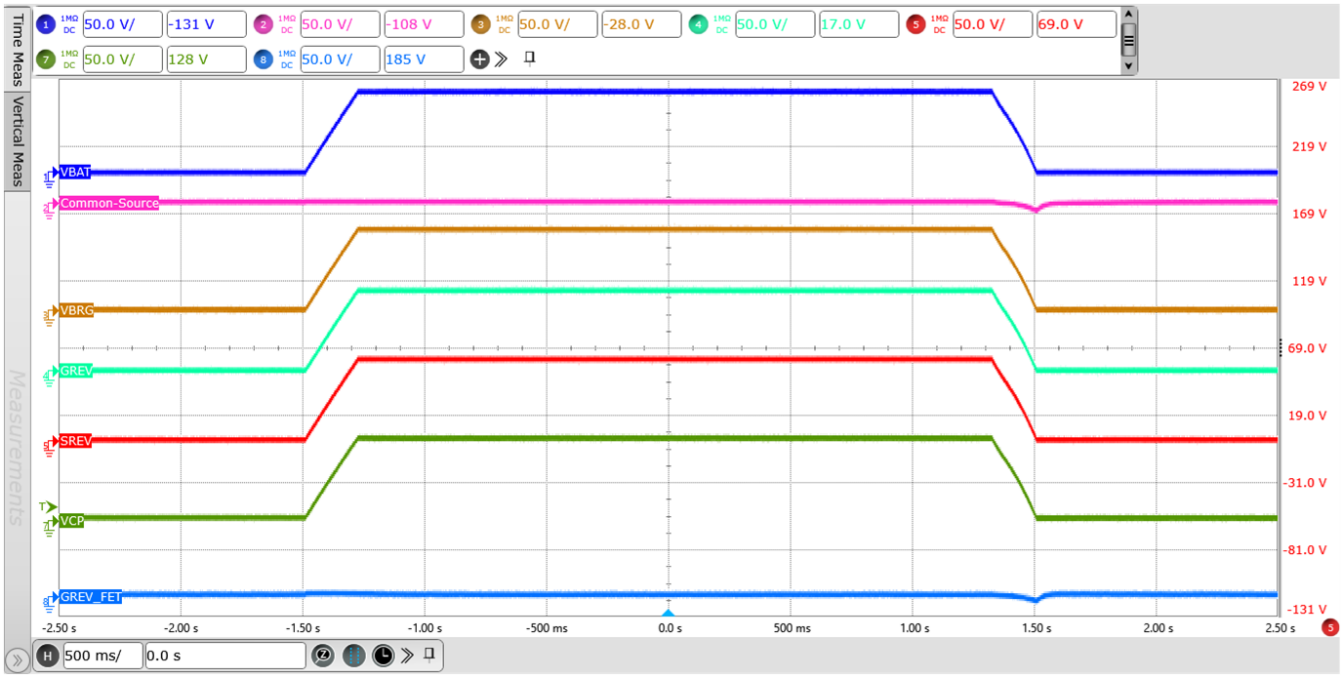

Figure 8: Waveform – Common-Source Reverse-Battery Event

CONFIGURATIONS COMPARISON

Both the common-drain and common-source configurations provide highly effective reverse-battery protection when paired with the A89103 and an external PMOS isolating transistor. The choice between the two often comes down to system-level control requirements:

Control Flexibility: The common-drain configuration allows for the independent control of the reverse FET and the bridge FET. This is highly advantageous in complex power distribution networks where the reverse FET might need to be modulated independently of the load-side bridge FET.

Simplicity of Drive: The common-source configuration is often preferred for its simplicity in simultaneous driving, as both MOSFETs share a common reference point (their sources). This allows the A89103 to turn both the reverse and bridge FETs on simultaneously with ease during normal operation.

Voltage Withstand: Both configurations, when augmented with the PMOS on the GREV line, successfully withstand reverse-battery conditions, making them suitable for both robust 12 V automotive systems and demanding 48 V applications.

CONCLUSION

This application note highlights the transition from passive diode protection to high-efficiency, active MOSFET reverse-battery protection using the A89103. For modern automotive systems, particularly those exposed to potential 48 V transients and –60 V reverse conditions, specialized configurations are required to prevent damage to the gate driver and the load.

By using either a common-drain or common-source topology, and introducing a simple PMOS transistor on the gate drive line, engineers can achieve robust, active reverse battery protection. The common-drain setup offers the distinct advantage of independent FET control, while the common-source setup excels in simultaneous switching applications. Both architectures leverage the A89103 to ensure maximum system efficiency, minimal heat dissipation, and complete protection against catastrophic reverse-polarity events.

REFERENCES

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[2] K. Tshiloz, A. Foletto and M. Kurihara, Reverse Battery Protection Scheme for Automotive Applications, https://www.allegromicro.com/-/media/files/application-notes/an296275-reverse-battery-protection.pdf, Allegro MicroSystems Application Notes, AN296275, Nov. 2022.

Revision History

Number	Date	Description
–	June 16, 2026	Initial release

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