MOSFET SLEW-RATE CONTROL WITH AN ALLEGRO SMART GATE DRIVER

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ABSTRACT

This application note presents practical strategies for the optimization of MOSFET switching dynamics of a three-phase Allegro smart gate driver (ASGD), such as the A89199 or the A4916. Unlike conventional gate drivers that rely on fixed gate resistance—where switching speed and slew rate are inherently coupled and lossy—the ASGD employs a high-resolution, programmable multistage current-source architecture. The gate current in the A89199 is adjustable from ±5 mA to ±75 mA in 5 mA increments, with timing resolution of 50 ns, enabling fine-grained control of both turn-on and turn-off switching trajectories.

By leveraging the gate-charge characteristics of the external MOSFET—specifically the gate-to-source charge (Q_{GS1}) and the gate-to-drain charge (Q_{GD})—the designer can independently control the dead time and adjust the current-rise time and voltage-slew (dV/dt) phases of each switching transition.

This application note introduces three distinct slew-rate control modes: 1) constant gate current; 2) two-step gate current with fixed first-stage parameters (I_1, t_{S1}) and variable second-stage current (I_2); and 3) two-step gate current with variable first-stage parameters and fixed second-stage current. Each mode offers a different tradeoff between simplicity of tuning and control of granularity.

A practical tuning methodology is presented using double-pulse test (DPT) measurements to experimentally characterize Q_{GS1} and Q_{GD} at the target operating conditions. The two-step current-source approach enables a fast-to-plateau strategy: the first stage ($I_1 \times t_{S1}$) rapidly charges Q_{GS1} to minimize dead-time distortion and propagation delay, while the second stage (I_2) provides controlled charging of Q_{GD} to achieve a target dV/dt that suppresses electromagnetic interference (EMI) and switching-node ringing. Detailed calculations, experimental waveforms, and step-by-step tuning procedures are provided to help engineers achieve optimal switching performance while meeting stringent automotive electromagnetic compatibility (EMC) requirements. The techniques are demonstrated on a 12 V automotive motor-drive system and are directly applicable to applications including steering, pumps, HVAC blowers, windshield wiper motors, etc.

Applicable Allegro Products

This application note uses the A89199 as an example. The slew-rate control methodology described in this application note is applicable to the A89199, A4918, A4916, A4911, and AMD89111 Allegro motor drivers.

INTRODUCTION

MOSFETs are the dominant switching devices in both low-voltage and high-voltage power stages across automotive and industrial applications. In the automotive domain, systems such as coolant pumps, HVAC blowers, and windshield-wiper motors commonly employ three-phase inverter topologies, where six MOSFETs are driven by a dedicated gate-driver unit. ASGDs, such as the A89199, provide a highly integrated, reliable solution for these motor-drive systems, combining gate drive, protection, and diagnostic functions in a single device.

A key requirement in these applications is precise control of the MOSFET switching performance. The rate of change of the switching-node voltage—commonly referred to as the slew rate, *dV/dt*—directly affects EMC, voltage stress on the power stage, and long-term reliability of downstream components such as motor winding insulation. An excessively high slew rate generates broadband EMI and can excite parasitic resonances that produce voltage overshoots and ringing. Conversely, an unnecessarily slow slew rate increases switching losses and dead-time distortion, degrading overall system efficiency.

In conventional gate-driver designs, the switching speed is governed by an external gate resistor. While straightforward to implement, this approach has fundamental limitations. The gate resistor sets a fixed resistor-capacitor (RC) time constant with the MOSFET input capacitance, coupling the current-rise phase (d$\mathbf{I}$/dt) and the voltage-slew phase (dV/dt) together. The designer cannot independently optimize one without affecting the other. Furthermore, the energy dissipated in the gate resistor during every switching cycle represents a direct power loss that scales with switching frequency.

A current-source gate driver overcomes these limitations through active regulation of the gate current rather than reliance on a passive voltage-divider relationship. By control of the magnitude of the gate current during different phases of the switching transition, the designer gains independent control of dV/dt and d$\mathbf{I}$/dt. The Allegro A89199 ASGD implements this capability through a programmable, multi-stage current-source architecture. The gate current is adjustable, typically from ±5 mA to ±75 mA in 5 mA increments, with each stage programmable in 50 ns (typical) time steps via the serial peripheral interface (SPI). This level of granularity enables fine-tuned shaping of both the turn-on and turn-off switching trajectories to meet specific application requirements.

The voltage slew rate of the MOSFET is fundamentally governed by the flow of gate current during the Miller-plateau region, where the gate-drain charge (Q_{GD}) is delivered (during turn-on) or removed (during turn-off). The relationship is expressed by the slew-rate equation (Equation 1) as:

Equation 1:

$$dV_{DS}/dt = I_G/C_{GD}$$

where dV_{DS}/dt is the rate of change of the drain-source voltage, $\mathbf{I}_G$ is the gate current, and C_{GD} is the gate-drain capacitance.

By adjusting the gate current during this critical interval, the ASGD provides direct, predictable control of the switching-node slew rate. However, effective slew-rate control requires accurate knowledge of the MOSFET gate-charge characteristics—specifically, the charge required to reach the Miller plateau (Q_{GS1}) and the charge required to traverse it (Q_{GD}). While MOSFET datasheets provide nominal gate-charge values, these are typically specified at a single test condition. The actual charge requirements vary with drain-source voltage (V_{DS}), drain current ($\mathbf{I}_D$), and junction temperature (T_J). This application note addresses this gap by presenting a practical measurement methodology based on double-pulse testing (DPT) to experimentally characterize Q_{GS1} and the gate-drain charge (Q_{GD}) at the target operating conditions of the application.

This application note presents three distinct slew-rate control strategies using the A89199 ASGD:

1. Constant gate current—a single-stage approach where a fixed gate current controls the entire switching transition.
2. Two-step gate current with fixed $\mathbf{I}_1/t_{S1}$ and variable $\mathbf{I}_2$—the first stage is calibrated to deliver Q_{GS1}, and the second-stage current is varied to adjust the slew rate by controlling Q_{GD}.
3. Two-step gate current with variable $\mathbf{I}_1/t_{S1}$ and fixed $\mathbf{I}_2$—the first-stage parameters are adjusted by controlling the Q_{GS1} while holding the slew-rate-controlling second-stage constant.

For each mode, detailed calculations, experimental waveforms, and step-by-step tuning procedures are provided. The techniques are demonstrated on a 12 V automotive motor-drive system using the A89199 evaluation board (APEK89199), and are directly applicable to applications including pumps, HVAC blowers, windshield-wiper motors, etc.

MOSFET SWITCHING CHARACTERISTICS UNDER CURRENT-SOURCE GATE DRIVE

Understanding the switching behavior of a MOSFET under current-source gate drive is essential for effective slew-rate control. Unlike a voltage-source (resistive) gate driver—where the gate current decays exponentially as V_{GS} rises—a current-source gate driver delivers a controlled, approximately constant current throughout the switching transition. This constant-current drive simplifies the relationship between gate charge and switching time, making it possible to precisely control the rate of change of drain-source voltage (dV_{DS}/dt) by adjusting the gate current magnitude.

This section describes the MOSFET turn-on and turn-off switching characteristics under constant current-source gate drive, identifies the key gate-charge regions, and establishes the fundamental relationship between gate current and slew rate that underpins the three control modes presented in this application note.

Turn-On Characteristics

The turn-on switching characteristics of a MOSFET under constant current-source gate drive are illustrated in Figure 1. The gate driver injects a constant-current $\mathbf{I}_G$ into the gate-source terminals of the MOSFET, progressively charging the gate capacitances until the device is fully enhanced (i.e., the device is in the fully on state). The total gate charge (Q_G) required for the complete turn-on of the MOSFET is the product of the gate current and the total switching time:

Equation 2:

$$Q_G = I_G \times t_{ON}$$

The turn-on transition can be divided into four distinct charge regions, each corresponding to a specific phase of the switching event, described next.

Region 1—Threshold Charge (Q_{TH}) from t_0 to t_1

At the beginning of the switching cycle, the MOSFET is off and $V_{GS} = 0$. The gate driver begins to inject current ($\mathbf{I}_G$), which charges the gate-source capacitance (C_{GS}). Because $\mathbf{I}_G$ is constant, V_{GS} rises linearly with time. During this interval, the drain-source voltage (V_{DS}) remains at the bus voltage V_{BB}, and drain current does not flow. This region ends when V_{GS} reaches the threshold voltage ($V_{GS(TH)}$) of the MOSFET. The charge delivered during this interval is:

Equation 3:

$$Q_{TH} = I_G \times (t_1 - t_0)$$

Region 2—Current-Rise Charge (Q_I) from t_1 to t_2

Once V_{GS} exceeds $V_{GS(TH)}$, a conduction channel forms and the drain current $\mathbf{I}_D$ begins to rise. The gate current continues to charge C_{GS}, and V_{GS} continues to increase linearly. The increasing V_{GS} increases the channel conductivity, allowing $\mathbf{I}_D$ to ramp up toward the load current ($\mathbf{I}_{LOAD}$). During this interval, V_{DS} remains at approximately V_{BB} because MOSFET operation is in the saturation region. This region ends when $\mathbf{I}_D$ reaches $\mathbf{I}_{LOAD}$ and V_{GS} reaches the Miller plateau voltage (V_{P1}). The charge delivered during this interval is:

Equation 4:

$$Q_I = I_G \times (t_2 - t_1)$$

The combined charge required to bring V_{GS} from zero to the Miller plateau V_{P1} is defined as:

Equation 5:

$$Q_{GS1} = Q_{TH} + Q_I = I_G \times (t_2 - t_0)$$

Q_{GS1} is a critical parameter for slew-rate control because it determines how much charge the gate driver must deliver before the voltage transition begins. Accurate knowledge of the Q_{GS1} value at the target operating conditions (V_{BB}, $\mathbf{I}_D$) is essential for proper configuration of the gate-driver timing.

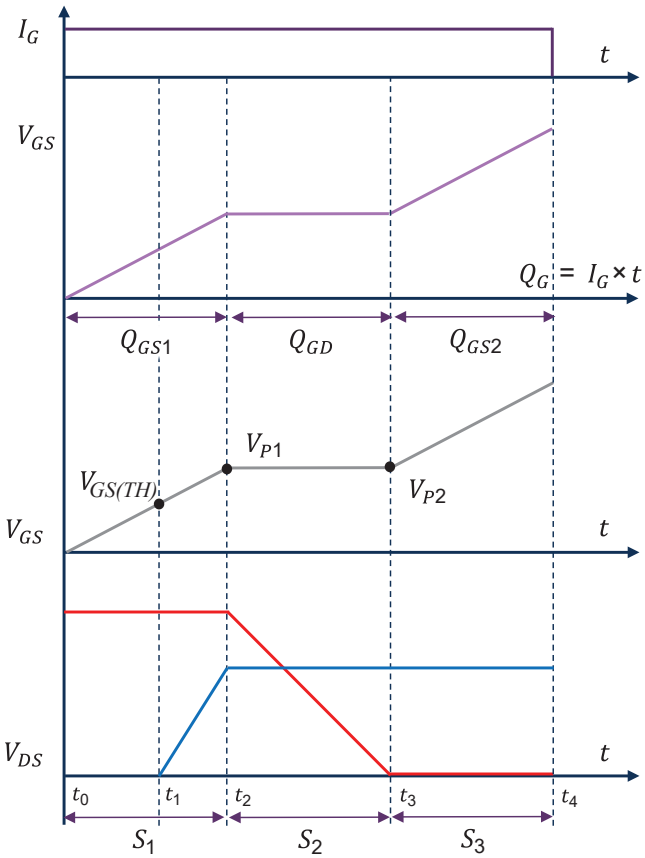


Figure 1: Typical MOSFET Turn-On Characteristics

Region 3—Miller Plateau Charge (Q_{GD}) from t_2 to t_3

Region 3 is the Miller plateau, which is the most critical region for slew-rate control. During this interval, V_{GS} remains essentially constant at V_{P1} while the gate current (I_G) charges the gate-drain capacitance ($C_{GD,}$ also referred to as the Miller capacitance). This charging causes V_{DS} to reduce from V_{BB} toward $V_{DS(ON)}$. The rate at which V_{DS} reduces—the slew rate (dV_{DS}/dt—is directly governed by the gate current and the value of C_{GD} as calculated in the slew-rate equation (Equation 1).

The drain current I_D ideally remains constant at I_{LOAD} throughout this region. The charge required to complete the V_{DS} transition (S_2) is:

Equation 6:

$$Q_{GD} = I_G \times (t_3 - t_2) = I_G \times S_2$$

where Q_{GD} represents the charge that directly controls the switching-node voltage transition. As per Equation 6, for a higher value of I_G, the duration of the V_{DS} transition (i.e., S_2) is reduced, which causes a faster dV_{DS}/dt.

For example, for a known MOSFET, if Q_{GD} is 5 nC and $V_{BB} = V_{DS} = 13.5$ V, dV_{DS}/dt (0 to 100%) is as shown in Table 1.

The slew rate during this region is the primary parameter that the gate driver must manage to balance switching losses, EMI, and voltage overshoot.

Table 1: Example of MOSFET dV_{DS}/dt with Varying Gate Current

I_G (mA)	Q_{GD} (nC)	V_{DS} (V)	S_2 (nS)	dV_{DS}/dt (V/µs)
20	10	13.5	500	27
30	10	13.5	333.3	40.5
40	10	13.5	250	54
60	10	13.5	166.7	81

Region 4—Remaining Gate-Source Charge (Q_{GS2}) from t_3 to t_4

After the Miller plateau, V_{DS} is settled at its on-state value, $V_{DS(ON)} = I_D \times R_{DS(ON)}$, and C_{GD} is fully charged. The gate current resumes charging C_{GS}, and V_{GS} increases from V_{P2} toward the applied gate-drive voltage $V_{GS(max)}$. This final charge region further reduces $R_{DS(ON)}$ and ensures the MOSFET is fully enhanced. The charge delivered during this interval is:

Equation 7:

$$Q_{GS2} = I_G \times (t_4 - t_3)$$

The total gate charge during turn-on is therefore:

Equation 8:

$$Q_G = Q_{GS1} + Q_{GD} + Q_{GS2}$$

The V_{REG} supplies the required current for the low-side driver, and the bootstrap circuit generates the floating supply voltage for the high-side driver.

Turn-Off Characteristics

The turn-off switching characteristics of a MOSFET under constant current-source gate drive are illustrated in Figure 2. The turn-off process is essentially the reverse of the turn-on process: the gate driver sinks a constant current (I_G) from the gate-source terminals and progressively discharges the gate capacitances until the device is in the fully off state. The four charge regions of the turn-on process occur in reverse order.

Region 1—Discharge of Q_{GS2} from t_5 to t_6

At the start of the turn-off process, the MOSFET is fully enhanced with $V_{GS} = V_{GS(max)}$. The gate driver begins to sink current I_G and to discharge C_{GS}. The gate-source voltage (V_{GS}) decreases linearly from $V_{GS(max)}$ toward the Miller plateau voltage (V_{P2}). During this interval, V_{DS} remains at $V_{DS(ON)}$ and I_D continues to flow at I_{LOAD}. The MOSFET remains fully enhanced and operates in the ohmic region. This region ends when V_{GS} reaches the Miller plateau voltage (V_{P2}). The charge delivered during this interval is:

Equation 9:

$$Q_{GS2} = I_G \times (t_6 - t_5)$$

Region 2—Miller Plateau Discharge (Q_{GD}) from t_6 to t_7

When V_{GS} reaches V_{P2}, the Miller plateau region begins. The gate current (I_G) now discharges the gate-drain capacitance (C_{GD}), which causes V_{DS} to rise from $V_{DS(ON)}$ toward V_{BB}. The gate-source voltage (V_{GS}) remains nearly constant at V_P, and I_D remains at I_{LOAD}. The rate of V_{DS} increase—the turn-off slew rate—is again governed by the slew-rate equation (Equation 1).

This region is the critical phase for turn-off slew-rate control. The charge required to complete the V_{DS} transition (S_2) is:

Equation 10:

$$Q_{GD} = -I_G \times (t_8 - t_7) = -I_G \times S_2$$

The charge removed during this interval equals Q_{GD}.

Region 3—Current Reduction (Q_I) from t_7 to t_8

After V_{DS} reaches V_{BB}, the Miller plateau ends. V_{GS} resumes its linear decrease to less than V_{P1}, and the MOSFET transitions from saturation into cutoff. The channel conductivity decreases, which causes I_D to reduce rapidly from I_{LOAD} toward zero. This region produces the dI_D/dt during the turn-off process.

Region 4—Final Discharge (Q_{TH}) from t_8 to t_9

V_{GS} continues to reduce to less than $V_{GS(TH)}$, the channel closes completely, and I_D reaches zero. V_{DS} remains at V_{BB}, and the MOSFET is in the fully off state.

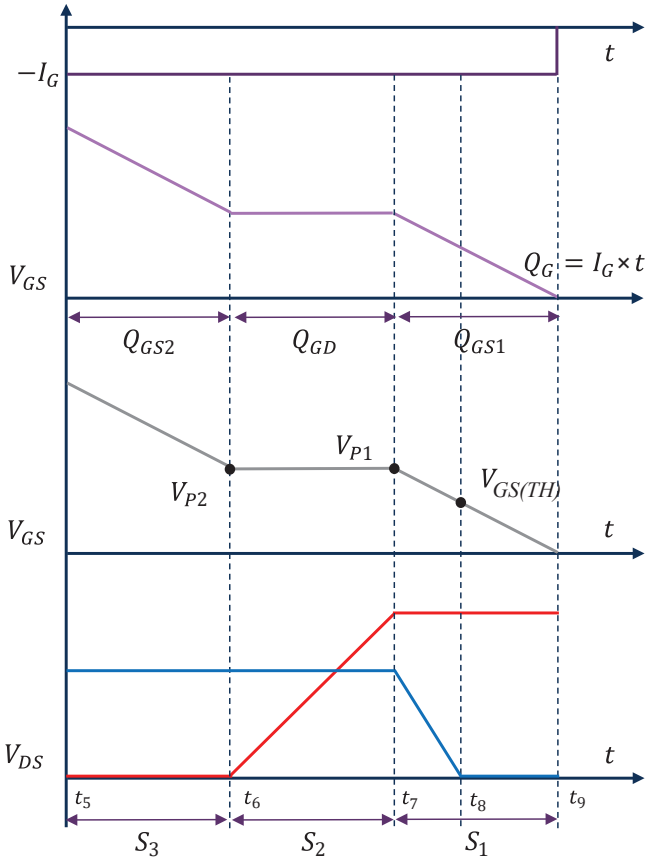


Figure 2: Typical MOSFET Turn-Off Characteristics

SLEW-RATE CONTROL MODES

The turn-on and turn-off analysis presented in the Turn-On Characteristics and Turn-Off Characteristics sections reveals a fundamental relationship: The slew rate of the drain-source voltage is directly proportional to the gate current during the Miller plateau region and inversely proportional to the gate-drain capacitance. This relationship is derived from the slew-rate equation (Equation 1), where $\mathbf{I}_G$ is the gate current during the Miller plateau and C_{GD} is the gate-drain capacitance at the instantaneous V_{DS}. This relation has three important implications for gate-driver design:

1. The gate current during the Miller plateau directly controls the slew rate.

   For a given MOSFET (with known C_{GD}), when gate current doubles during the Miller plateau, the slew rate approximately doubles. In terms of slew-rate control, this linear relationship makes a current-source gate drive fundamentally superior to a resistive gate drive—The designer has a direct, programmable interface to adjust $(dV_{DS})/dt$.

2. The gate current before the Miller plateau does not affect the slew rate—It only affects the delay time.

   The charge Q_{GS1} must be delivered before V_{DS} begins to transition. The current used to deliver Q_{GS1} determines how quickly the MOSFET reaches the Miller plateau (i.e., the turn-on delay), but it does not influence the V_{DS} transition rate itself. This decoupling of delay time and slew rate is a key advantage of the two-step current-source gate-drive approach.

3. The nonlinearity of C_{GD} with V_{DS} causes the slew rate to vary during the transition.

   Because C_{GD} is not constant—it is low at high V_{DS}, and it is high at low V_{DS}—the instantaneous slew-rate changes throughout the Miller plateau, even under constant gate current. At the beginning of the turn-on transition (high V_{DS}, low C_{GD}), the slew rate is highest; as V_{DS} reduces and C_{GD} increases, the slew rate decreases. This nonlinear behavior must be considered when selecting the gate current to ensure that the peak slew rate (not just the average) remains within the system limits.

These implications lead to three distinct approaches for control of the MOSFET slew rate using a current-source gate driver. Each mode offers a different tradeoff between simplicity, flexibility, and independent control of delay time versus slew rate. In the sections that follow, each mode is described and theoretical switching waveforms are presented.

Mode 1: Constant Gate Current

In this mode, a single gate-current level (I_G) is applied throughout the entire switching event, as shown in Figure 3 (turn-on) and Figure 4 (turn-off). The same current charges Q_{GS1} (which sets the delay time) and Q_{GD} (which sets the slew rate). Consequently, both the delay time and the slew rate scale together—An increase to I_G reduces the delay but also increases dV_{DS}/dt, and vice versa.

This mode is the simplest to configure and is suitable for applications where the delay time and slew rate do not need to be independently optimized. However, because I_G simultaneously governs both parameters, any adjustment to the slew rate necessarily changes the delay time.

As shown in Figure 3, during turn-on, the constant current I_G first charges Q_{GS1} to reach the Miller plateau; afterward, the same current I_G charges Q_{GD} and drives the V_{DS} transition. The turn-off behavior in Figure 4 is the mirror image: I_G first discharges Q_{GS2}, then discharges Q_{GD} during the Miller plateau to ramp V_{DS} back to V_{BB}.

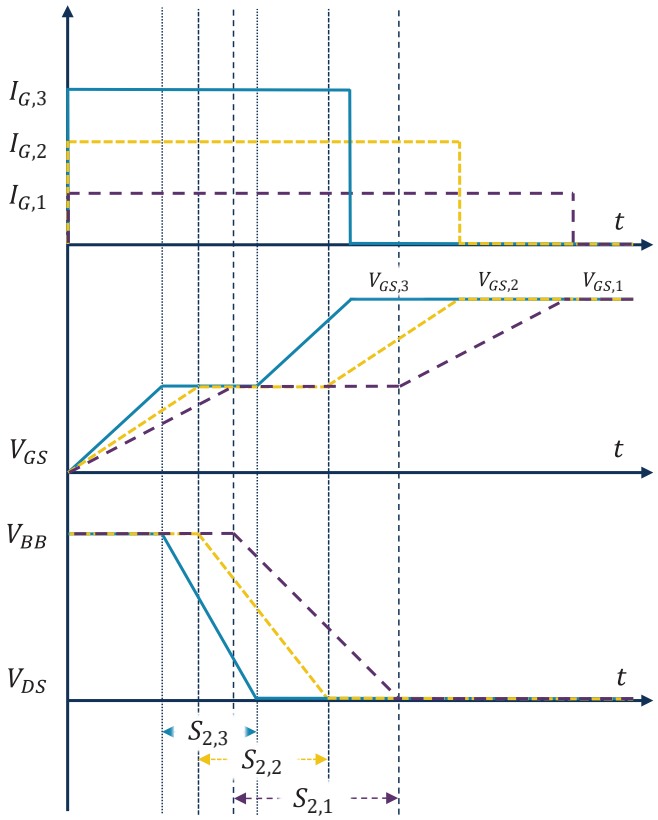


Figure 3: Typical Turn-On Characteristics of MOSFET in Mode 1

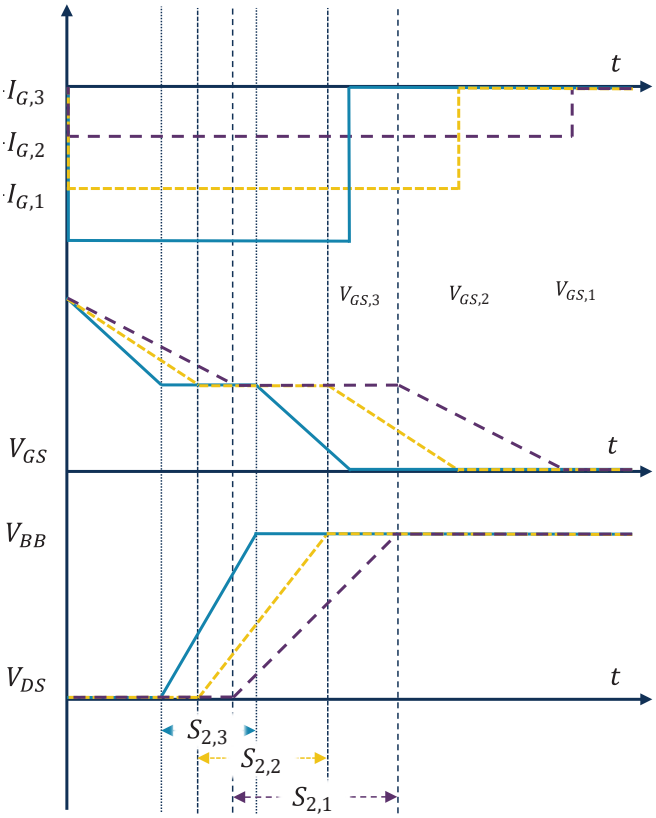


Figure 4: Typical Turn-Off Characteristics of MOSFET in Mode 1

Mode 2: Two-Step Gate Current—Fixed I_1/t_{S1}, Variable I_2

In this mode, the gate current is delivered in two steps. The first step applies current I_1 for fixed duration t_{S1}, calibrated to deliver the charge Q_{GS1} required to reach the Miller plateau. At the end of t_{S1}, the gate driver transitions to a second current level I_2, which controls the V_{DS} slew rate during the Miller plateau. The turn-on and turn-off waveforms for this mode are shown in Figure 5 and Figure 6, respectively.

This mode decouples the delay time from the slew rate. By holding I_1 and t_{S1} constant (such that $I_1 \times t_{S1} \approx Q_{GS1}$), the delay time remains fixed regardless of the selected slew rate. The slew rate is then independently adjusted by varying I_2 alone in the slew-rate equation (Equation 1).

As illustrated in Figure 5, during turn-on, the first step (I_1, t_{S1}) delivers Q_{GS1} to bring V_{GS} to the Miller plateau, after which the second step (I_2) takes over and governs the rate of the V_{DS} reduction. In Figure 6, the turn-off mirror image shows I_2 control of the V_{DS} rise during the Miller plateau, followed by I_1 completing the V_{GS} discharge.

This mode is recommended when the designer needs to sweep the slew rate across multiple operating points while maintaining a consistent switching delay—a common requirement in EMI optimization and compliance testing.

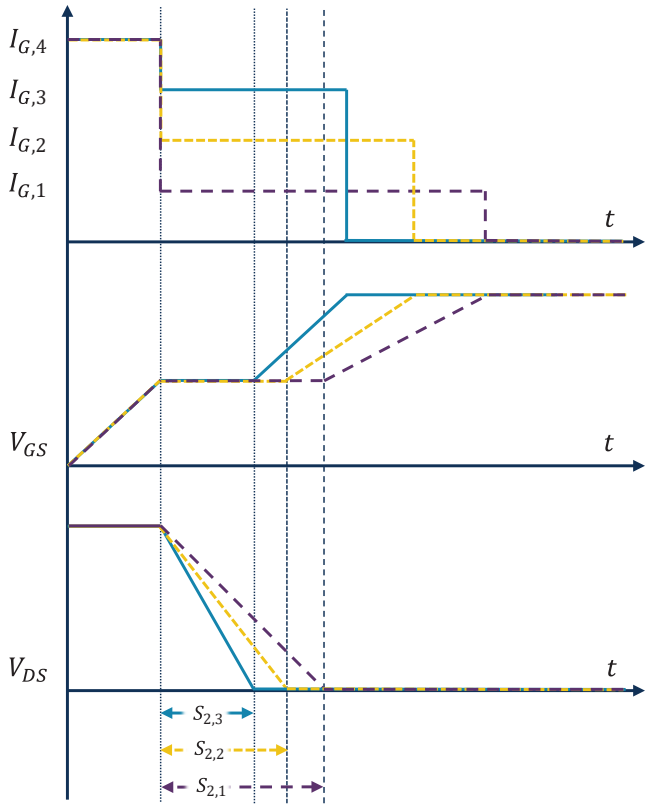


Figure 5: Typical Turn-On Characteristics of MOSFET in Mode 2

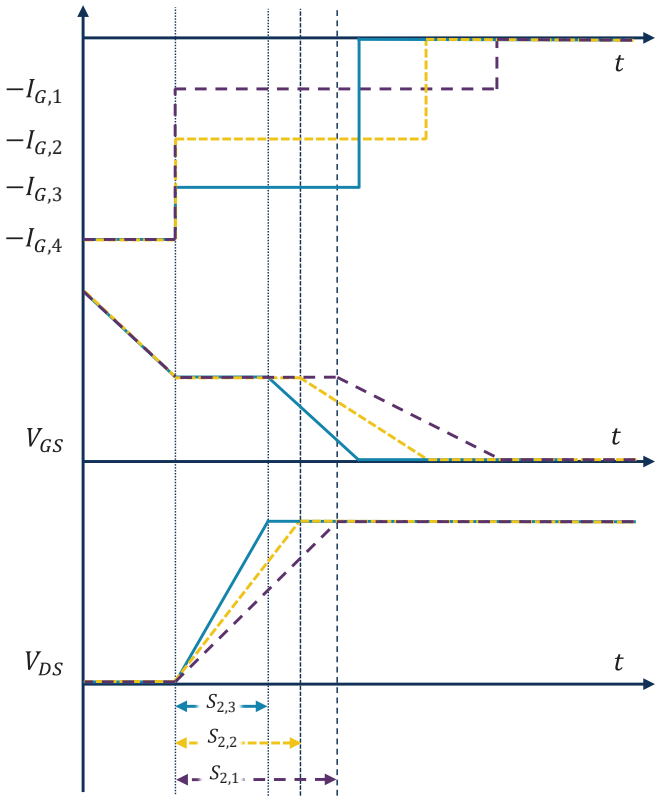


Figure 6: Typical Turn-Off Characteristics of MOSFET in Mode 2

Mode 3: Two-Step Gate Current—Variable I_1/t_{S1}, Fixed I_2

In this mode, the second step current (I_2) is held constant to maintain a fixed slew rate, while the first step parameters (I_1 and t_{S1}) are varied to adjust the delay time. The turn-on and turn-off waveforms for this mode are shown in Figure 7 and Figure 8, respectively.

Because I_2 is fixed, the V_{DS} slew rate remains the same regardless of how the delay time is adjusted:

Equation 11:

$$(dV_{DS})/dt = I_2/C_{GD} = constant$$

As shown in Figure 7, during turn-on, the first step (I_1, t_{S1}) delivers Q_{GS1}, and adjustment to I_1 or t_{S1} changes only how quickly the Miller plateau is reached. Once the Miller plateau begins, I_2 takes over and produces the same V_{DS} transition rate regardless of the I_1/t_{S1} configuration. The turn-off behavior in Figure 8 follows the same principle in reverse.

This mode is recommended when the application requires a fixed, certified slew rate (e.g., to stay within a validated EMI envelope) while allowing the designer to adjust the delay time for dead-time optimization or system-level timing requirements.

Summary

The Allegro A89199 ASGD provides SPI-programmable gate current, typically from ±5 mA to ±75 mA in 5 mA steps, with a time duration (t_{S1}) configurable in 50 ns (typically) increments, which enables the designer to implement any of the three modes. Each mode is presented in detail in this section (Slew-Rate Control Modes) and the performance is validated through double-pulse test (DPT) measurements presented in the Experimental Results section.

The three implications presented at the start of this section (Slew-Rate Control Modes) motivate the three slew-rate control modes shown in Table 2.

Table 2: Summary of Slew-Rate Control Modes

Control Mode	Gate Current Profile	Delay Time	Slew Rate	Figures
Mode 1: Constant I_G	Single current level throughout	Coupled to I_G	Coupled to I_G	Figure 3 Figure 4
Mode 2: Fixed I_1/t_{S1}, Variable I_2	Two-step; I_1, t_{S1} fixed; I_2 varied	Fixed	Adjustable via I_G	Figure 5 Figure 6
Mode 3: Variable I_1/t_{S1}, Fixed I_2	Two-step; I_1, t_{S1} varied; I_2 fixed	Adjustable via I_1/t_{S1}	Fixed I_G	Figure 7 Figure 8

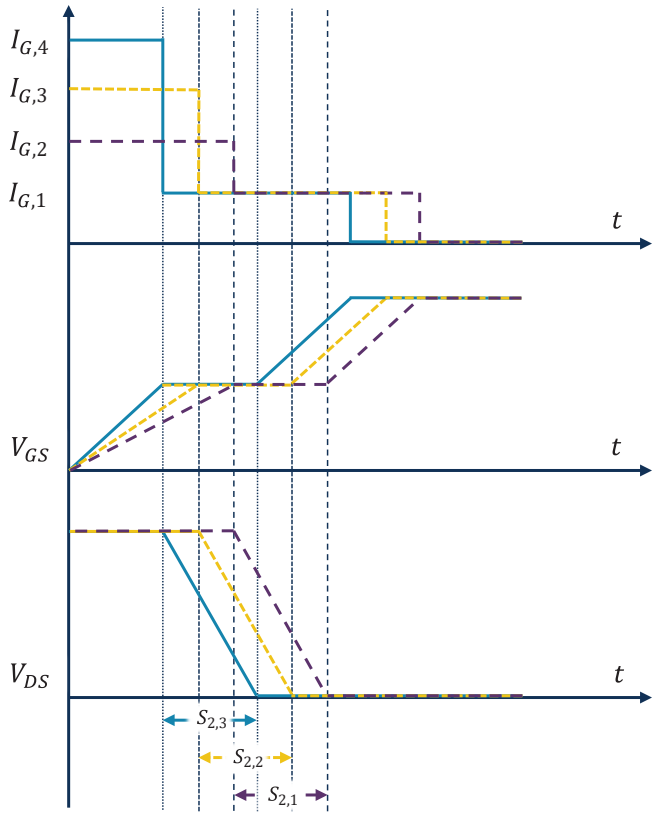


Figure 7: Typical Turn-On Characteristics of MOSFET in Mode 3

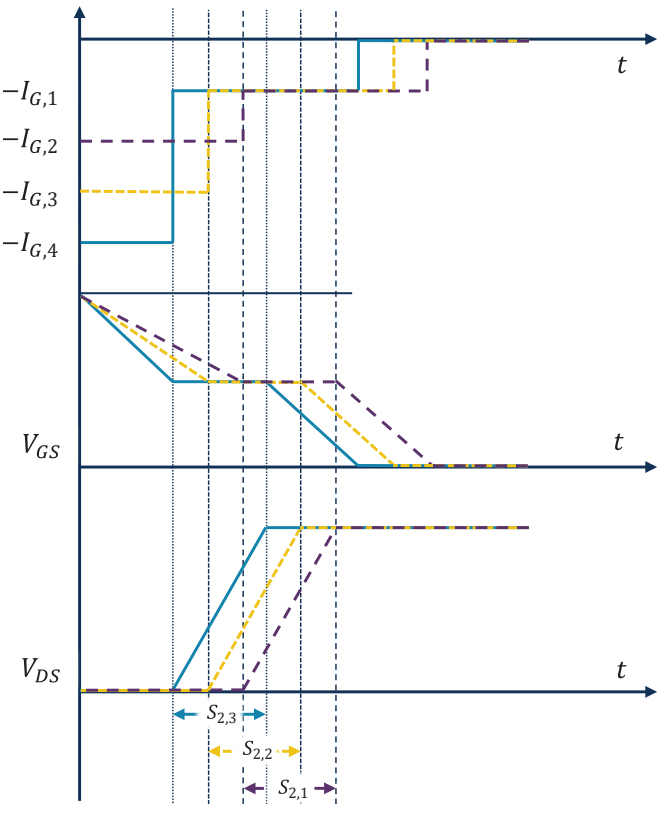


Figure 8: Typical Turn-Off Characteristics of MOSFET in Mode 3

EXPERIMENTAL SETUP

To validate the slew-rate control methodologies discussed in the Slew-Rate Control Modes section, a comprehensive hardware evaluation was performed. This section details the test circuit, the equipment configuration, and the baseline characterization procedure required to extract the specific gate-charge parameters of the MOSFET under the target operating conditions.

Double-Pulse Test Circuit

The dynamic switching characteristics of the MOSFETs were evaluated using a standard double-pulse test (DPT) methodology. The DPT is the industry-standard approach for characterization of the hard-switching behavior of power semiconductor devices because it allows for precise control of the voltage and current commutation without subjecting the power stage to the thermal stress of continuous operation.

Operating Principle: The DPT circuit (see Figure 9) typically consists of a half-bridge configuration with an inductive load connected in parallel with the high-side device, while the low-side device acts as the device under test (DUT). The test sequence consists of two distinct pulses (see Figure 10) applied to the gate of the DUT:

- ***First Pulse:*** The DUT is turned on for a calculated duration to build up the desired load current (I_D) through the inductor. At the end of this pulse, the DUT is turned off. This turn-off event is captured to analyze the turn-off switching characteristics and slew rate. During the off-time, the inductor current freewheels through the body diode of the complementary high-side MOSFET (or an external Schottky diode).
- ***Second Pulse:*** The DUT is turned on again for a shorter duration. Because the inductor is already carrying the full load current, this turn-on event represents a hard-switching commutation. This transition is captured to analyze the turn-on switching characteristics, reverse recovery effects, and turn-on slew rate.

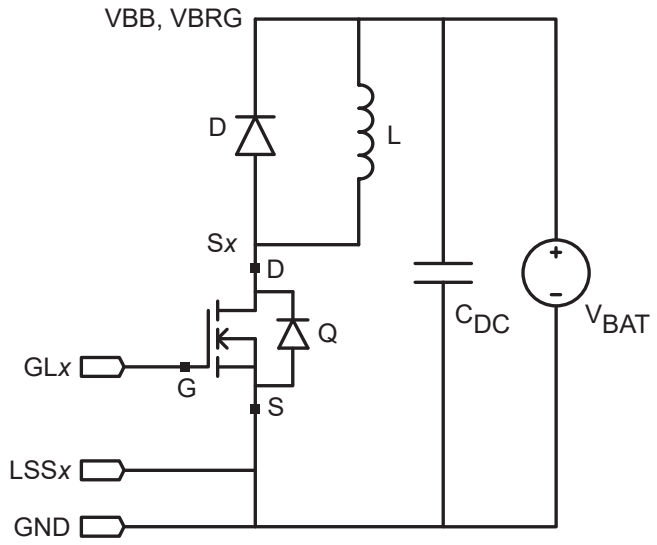


Figure 9: DPT Circuit

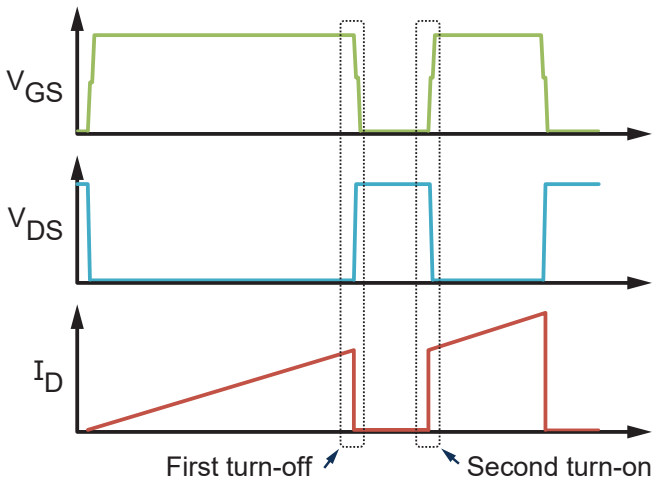


Figure 10: DPT Waveform

Test Equipment and Configuration

The experimental validation was conducted using the Allegro A89199 evaluation board (APEK89199), which features the A89199 ASGD. The test bench was configured to replicate a typical 12 V automotive motor-drive environment. See Figure 11.

Equipment Configuration

- Gate Driver Board: Allegro A89199 evaluation board (APEK89199) populated with the A89199 and the target automotive MOSFETs.
- Control Interface: A PC running the A89199 graphical user interface (GUI). The GUI communicates with the evaluation board via SPI, allowing real-time, fine-grained adjustment of the multistage gate current parameters (I_1, t_{S1}, and I_2).
- Signal Generation: A precision PWM generator used to supply the double-pulse logic signals to the A89199 input pins.
- Power Supply: A high-current DC power supply set to a nominal battery voltage of V_{BB} = 13.5 V.
- Measurement Probes:
  - Gate-Source Voltage (V_{GS}): Measured using optically isolated probes (e.g., Tektronix IsoVu). Isolated probes are critical for high-side measurements to reject high dV/dt common-mode noise and accurately capture the Miller plateau voltage.
  - Drain-Source Voltage (V_{DS}): Measured using high-bandwidth differential voltage probes to capture the switching-node slew rate.

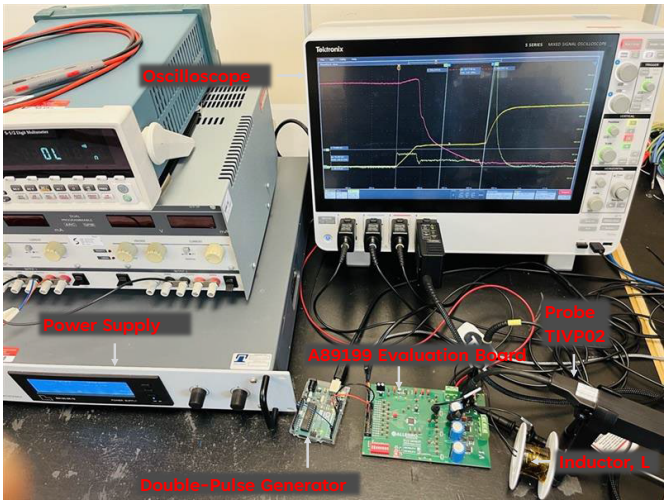


Figure 11: Bench Test Setup

Gate-Charge Characterization

While MOSFET datasheets provide nominal gate-charge values, these are typically specified under static test conditions that might not reflect the actual application. To accurately program the A89199 two-step current drive, the pre-plateau charge (Q_{GS1}) and the Miller plateau charge (Q_{GD}) must be characterized at the target operating point. A constant current source can be used to drive the gate during testing to easily extract these gate charge characteristics.

Characterization Procedure:

1. Set Operating Conditions: The DPT power supply is set to V_{BB} = 13.5 V, and the first pulse width is calibrated to achieve a target load current of I_D = 10 A.
2. Configure Constant Current Drive: A constant current source is used to drive the MOSFET gate. A fixed, known gate current (e.g., I_G = 40 mA) is applied for the entire switching transition to allow for clear observation of the charge regions.
3. Capture Waveforms: The DPT is executed, and the oscilloscope captures V_{GS}, V_{DS}, and I_G.
4. Extract Parameters:
   - Q_{GS1} Measurement: Observe the V_{GS} waveform to identify the time interval ($t_2 - t_0$) from the start of the gate pulse until V_{GS} reaches the Miller plateau and V_{DS} begins to reduce. The pre-plateau charge is calculated as: $Q_{GS1} = I_G \times S_1$
   - Q_{GD} Measurement: Identify the time interval ($t_3 - t_2$) during which V_{GS} is flat (the Miller plateau) and V_{DS} transitions from V_{BB} to nearly zero. The Miller charge is calculated as: $Q_{GD} = I_G \times S_2$

By experimentally determining Q_{GS1} and Q_{GD} at 13.5 V and 10 A, the designer can accurately calculate the required first-stage current (I_1) and time (t_{S1}) to rapidly traverse the turn-on delay; the designer can subsequently tune the second-stage current (I_2) of the smart gate driver to achieve the desired dV/dt slew rate.

EXPERIMENTAL RESULTS

This section presents the empirical data captured using the setup described in the Experimental Setup section. Each control mode was tested at V_{BB} = 13.5 V and I_D = 10 A to evaluate its effectiveness in managing the dV/dt slew rate while minimizing unnecessary switching delays.

Constant Gate Current (Mode 1)

In Mode 1, the A89199 provides a single, constant gate current (I_G) throughout the entire turn-on and turn-off transition. This mode serves as the baseline for comparison.

Analysis: Increasing the gate current (I_G) directly increases the slew rate (dV/dt) during the switching process, which reduces switching losses, as shown in the waveforms in Figure 12 and Figure 13. However, because I_G is constant, the time required to charge the pre-plateau region (Q_{GS1} during turn-on and Q_{GS2} during turn-off) is also tied to the same current level.

- Low I_G (e.g., 20 mA): Results in a very soft slew rate but introduces a significant turn-on and turn-off delay (t_d) as the driver slowly charges the gate to the Miller plateau.
- High I_G (e.g., 60 mA): Minimizes delay, but the resulting high dV/dt can lead to increased EMI and voltage ringing on the phase node.

The fundamental tradeoff in constant gate current mode (mode 1) is that the designer cannot optimize the dead time/delay and the slew rate independently.

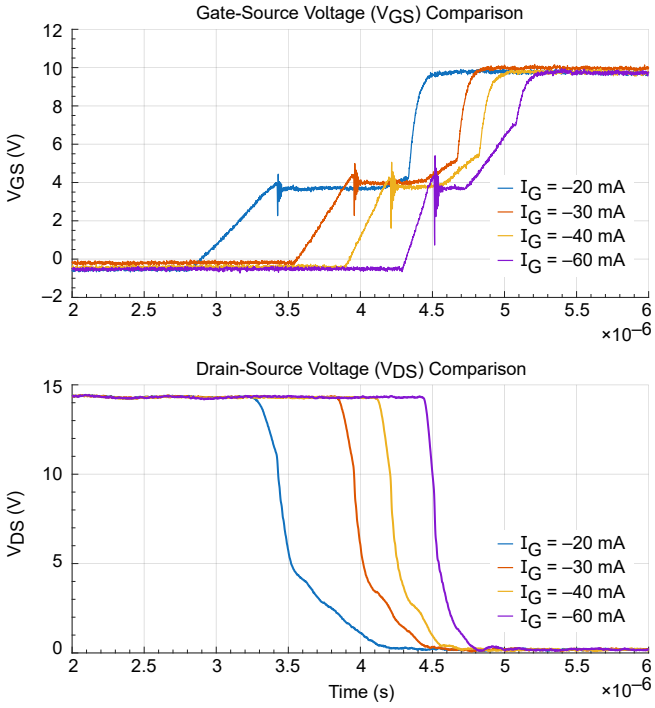


Figure 12: Experimental Waveforms from Turn-On in Mode 1

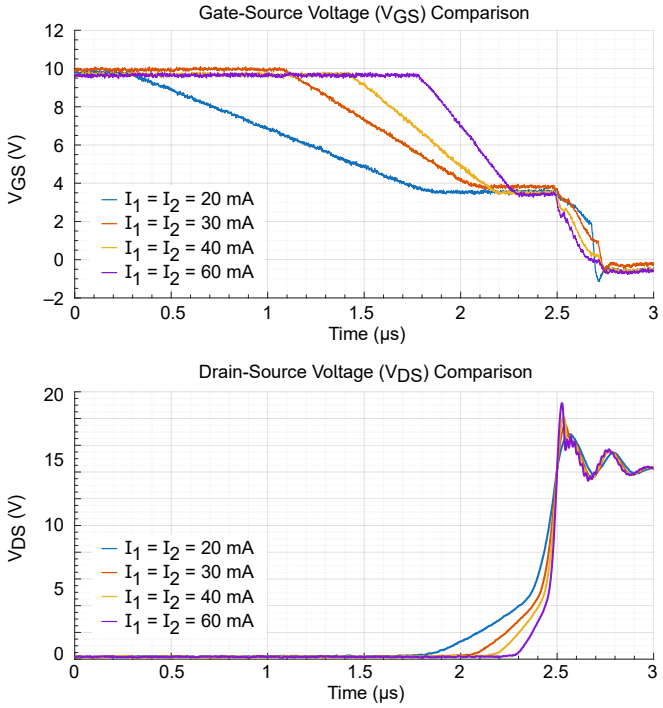


Figure 13: Experimental Waveforms from Turn-Off in Mode 1

Two-Step Gate Current: Fixed I_1/t_{S1}, Variable I_2 (Mode 2)

Mode 2 uses the ASGD ability to provide a high-current boost (I_1) for a fixed duration (t_{S1}) to rapidly reach the Miller plateau during turn-on and turn-off, followed by a variable current (I_2) to control the slew rate.

Analysis: In Figure 14 and Figure 15, by setting I_1 to a high value of 70 mA and t_{S1} to match the pre-plateau charge (Q_{GS1} during turn-on and Q_{GS2} during turn-off), the turn-on delay is drastically reduced compared to Mode 1. Once the Miller plateau is reached, I_2 is varied to tune the dV/dt.

- Performance: The results demonstrate that the slew rate can be adjusted from approximately 23 V/µs to 75 V/µs by varying I_2 (as in Table 3 and Table 4), all while maintaining a consistent, minimized turn-on delay.
- Benefit: This mode is ideal for applications where the load current is relatively stable, allowing the designer to set the I_1/t_{S1} phase once, then focus purely on EMI tuning via I_2.

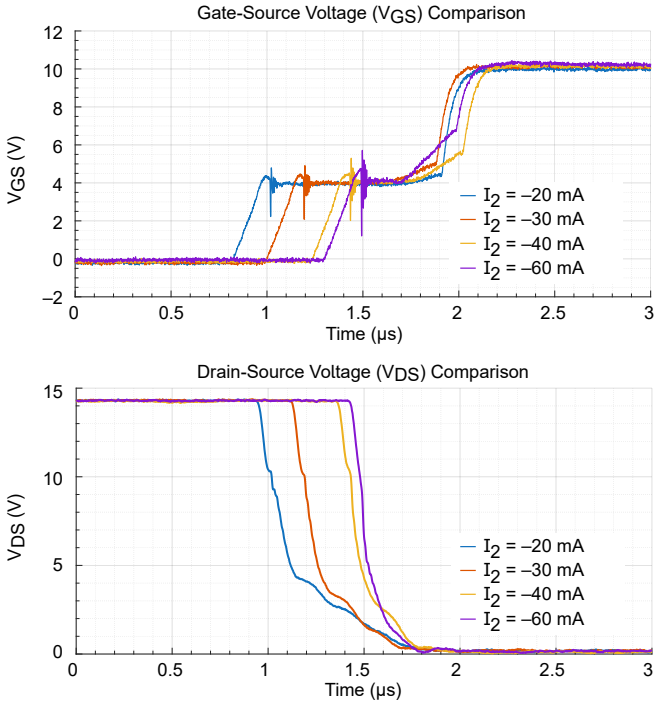


Figure 14: Experimental Waveforms from Turn-On in Mode 2

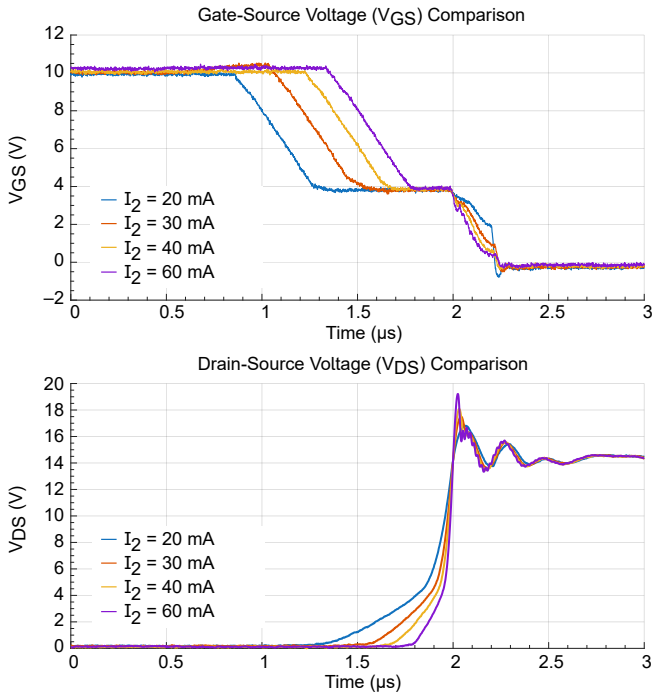


Figure 15: Experimental Waveforms from Turn-Off in Mode 2

Table 3: Slew Rate Results for Turn-On

I_G	Δt (80% to 20%)	ΔV	Slew Rate
–20 mA	0.365 µs	8.87 V	24.30 V/µs
–30 mA	0.276 µs	8.95 V	32.46 V/µs
–40 mA	0.186 µs	9.01 V	48.34 V/µs
–60 mA	0.129 µs	8.86 V	68.80 V/µs

Table 4: Slew Rate Results for Turn-Off

I_G	Δt (20% to 80%)	ΔV	Slew Rate
20 mA	0.375 µs	8.83 V	23.53 V/µs
30 mA	0.244 µs	8.85 V	36.29 V/µs
40 mA	0.180 µs	8.92 V	49.51 V/µs
60 mA	0.118 µs	8.77 V	74.19 V/µs

Two-Step Gate Current: Variable I_1/t_{S1}, Fixed I_2 (Mode 3)

In Mode 3, the second-stage current (I_2) is held fixed to maintain a constant slew rate of nearly 24 kV/µs, while the first-stage parameters (I_1 and t_{S1}) are adjusted to achieve the desired delay time, as shown in Figure 16 and Figure 17.

Analysis: This mode is particularly useful for characterizing the sensitivity of the system to the dead time and the timing of the current transition.

- Observation: The effect of adjustments to t_{S1} and I_1 before reaching the Miller plateau to minimize (or adjust) the delay time in the system is shown in The waveforms in Figure 16 and Figure 17. If t_{S1} is too short, the driver switches to the lower I_2 current before reaching the plateau, which unnecessarily increases the delay. If t_{S1} is too long, I_1 bleeds into the Miller plateau, causing a difficult-to-control spike in the slew rate. Thus, the t_{S1} and I_1 parameter selection is crucial for the optimal operation.
- Benefit: Mode 3 allows designers to precisely align the I_1-to-I_2 transition with the start of the Miller plateau across different MOSFET types, ensuring that the target slew rate defined by I_2 is perfectly maintained without transition artifacts.

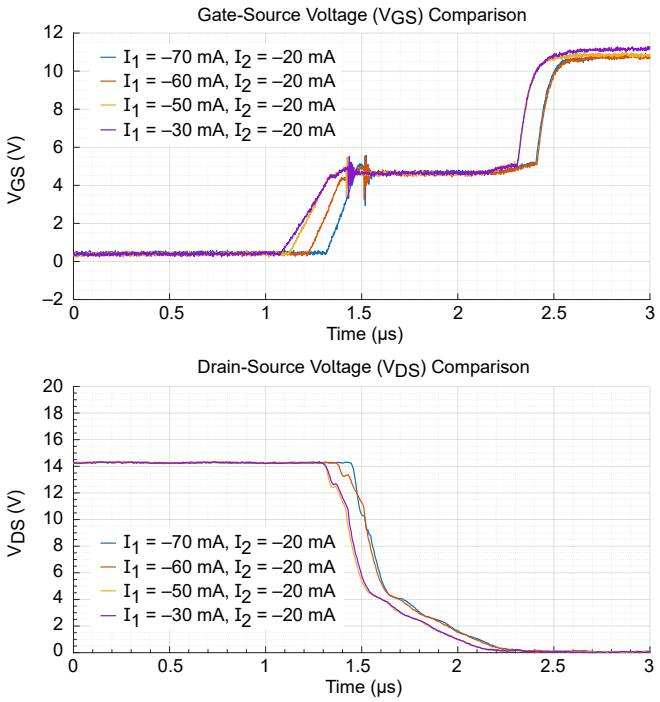


Figure 16: Experimental Waveforms from Turn-On in Mode 3

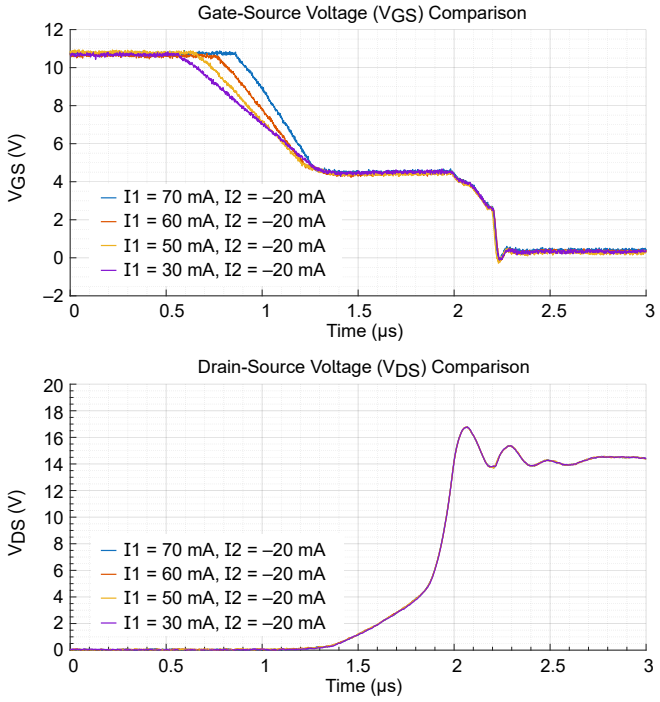


Figure 17: Experimental Waveforms from Turn-Off in Mode 3

Summary of Experimental Results

The measured performance across the three modes is summarized in Table 5, which highlights the primary advantage of the A89199 two-step drive: decoupling of the turn-on delay from the slew-rate control.

Table 5: Measured Performance of Modes 1 – 3

Control Mode	Slew-Rate Control	Delay Optimization	Primary Application
Mode 1	Dependent on I_G	Linked to I_G	Basic/low-speed switching
Mode 2	Highly adjustable (I_2)	Optimized (fixed I_1/t_{S1})	Standard EMI tuning
Mode 3	Fixed (I_2)	Adjustable (I_1/t_{S1})	Precision timing/ High-efficiency

Benefit: Combining mode 2 and mode 3 allows designers to precisely align the I_1-to-I_2 transition with the start of the Miller plateau across different MOSFET types, ensuring that the target slew rate defined by I_2 is perfectly maintained without transition artifacts.

CONCLUSION

An Allegro smart gate driver provides a sophisticated multi-stage gate-drive architecture that overcomes the fundamental limitations of a traditional driver using gate resistance and constant-current drivers. By decoupling the charge phases of the MOSFET switching transition, designers can achieve optimized switching performance without compromising EMI and efficiency.

Summary of Slew-Rate Control Steps

To achieve precise slew-rate control in a practical design, the following workflow is recommended:

1. ***Characterization:*** Use a double-pulse test (DPT) with a constant current source to experimentally measure the pre-plateau charge (Q_{GS1}) and the Miller plateau charge (Q_{GD}) at the target V_{BB} and I_D conditions.
2. ***Delay Optimization:*** Configure the first stage (I_1, t_{S1}) of the ASGD to provide a high current boost that rapidly delivers Q_{GS1} during the turn-on process and Q_{GS2} during the turn-off process. This minimizes the delay during the turn-on and turn-off processes. This also allows for reduced-duration dead-time settings in the controller.
3. ***Slew-Rate Tuning:*** Adjust the second stage current (I_2) to deliver Q_{GD} at the specific rate required to meet dV/dt targets. This ensures that EMI and voltage ringing are managed specifically during the Miller plateau phase.
4. ***Verification:*** Validate the transition point between I_1 and I_2 using high-bandwidth isolated probes to ensure the current step aligns correctly with the start of the Miller plateau.

Final Takeaway

The primary advantage of the A89199 architecture is the ability to independently control the gate current levels for different portions of the switching cycle. This independence allows the designer simultaneously to minimize dead time (for improved efficiency and duty cycle range) and to control the slew rate precisely (for EMI compliance). By following the methodologies outlined in this note, engineers can transition from a trial-and-error approach to a systematic, data-driven optimization of power-stage switching performance.

APPENDIX: SLEW-MODE TO SWITCH-MODE TRANSITION

Overview

During each MOSFET switching event, the A89199 operates in slew mode (gate current-control mode) to precisely shape the dV/dt, as described in this application note. Once the MOSFET has reached its fully on or fully off state, the driver transitions to switch mode (gate voltage-control mode), which efficiently holds the MOSFET in its static on or off state.

This appendix describes the criteria that govern the slew-mode-to-switch-mode transition and how these modes relate to the programmable V_{DS} thresholds.

Transition Criteria

The A89199 monitors the drain-source voltage (V_{DS}) across the relevant sense pair at the end of each switching event. The transition from slew mode to switch mode occurs once V_{DS} reduces to less than a programmable threshold, confirming that the MOSFET has completed its switching transition. The four conditions specified in the datasheet are:

- High-Side (HS) MOSFET turn-on:
$$V_{(DS-HS)} = (V_{BRG} - V_{Sx}) < V_{DSTH}$$
- High-Side (HS) MOSFET turn-off:
$$V_{(DS-HS)} = (V_{Sx} - V_{LSSx}) < V_{DSTL}$$
- Low-Side (LS) MOSFET turn-on:
$$V_{(DS-LS)} = (V_{Sx} - V_{LSSx}) < V_{DSTL}$$
- Low-Side (LS) MOSFET turn-off:
$$V_{(DS-LS)} = (V_{BRG} - V_{Sx}) < V_{DSTH}$$

Threshold Programming

The drain-source voltage high and low thresholds (V_{DSTH} and V_{DSTL}, respectively) are generated by internal digital-to-analog converters (DACs) and are configured by the VTH [5:0] and VTL [5:0] register bits, respectively. This allows the designer to independently tune the slew-to-switch transition point for the high-side and low-side sense nodes based on the MOSFET $R_{DS(on)}$ and the expected load current.

Transition Timing

Once the applicable V_{DS} threshold condition is satisfied, the gate control transitions from slew mode to switch mode within the time specified in Table 6. After this transition, the GHx/GLx output switches from current-source drive to voltage-source drive, holding the MOSFET in its fully on (or fully off) state.

Table 6: Transition Time Specification—Slew Mode to Switch Mode.

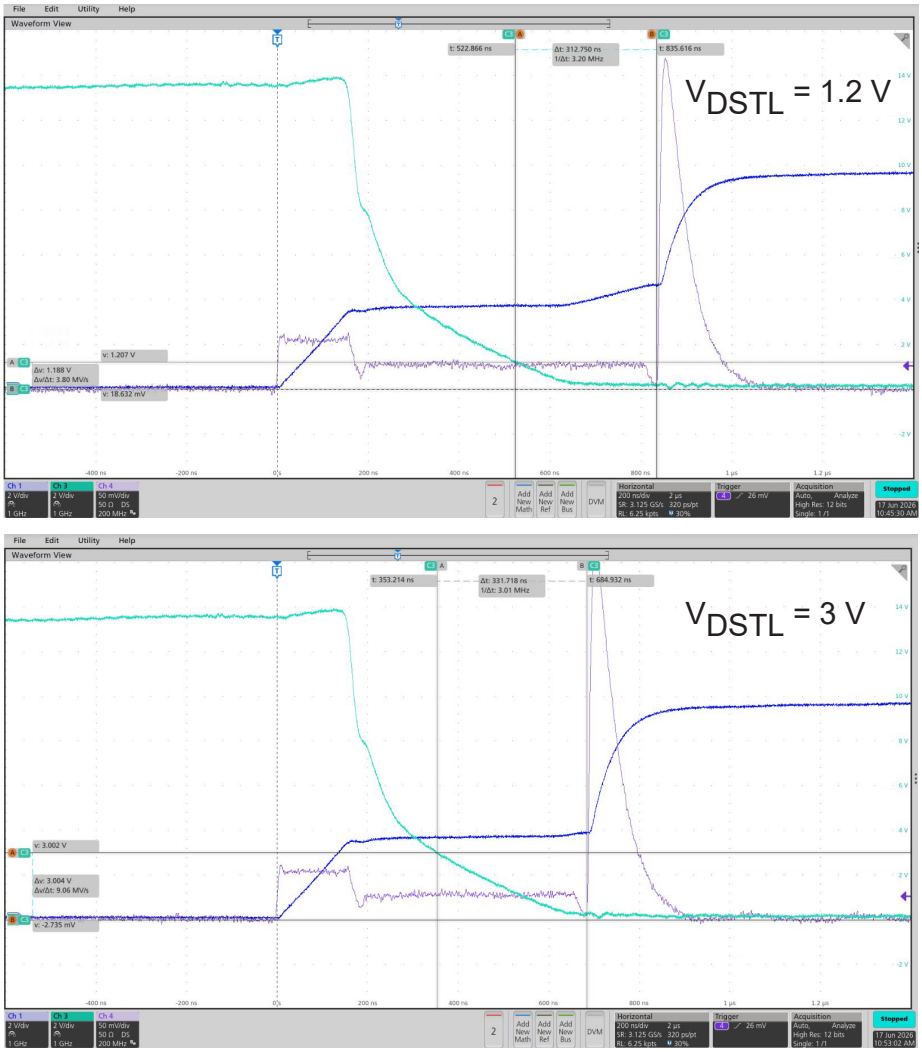
Minimum	Typical	Maximum	Unit
160	426	692	ns

Importance for Dead-Time Configuration

For gate-drive control to be operational, the dead-time register DT [5:0] must be set to a nonzero value. The dead time must be large enough to ensure that, during turn-off of any MOSFET, the device has fully transitioned to the off state (i.e., has reached the slew-to-switch transition) before the start of turn-on of the complementary MOSFET in the same phase. Failure to allow sufficient dead time might result in shoot-through current and excessive power dissipation.

Experimental Validation of Slew-to-Switch Transition

An experimental capture of a low-side MOSFET turn-on transition is shown in Figure 18 illustrating the slew-to-switch mode transition. The waveforms show the measured V_{DS}, V_{GS}, and I_G. The threshold V_{DSTL} is programmed to 1.2 V and 3 V in Figure 18. As turn-on of the low-side MOSFET occurs, V_{DS} reduces under the control of the programmed gate current I_2 (slew mode). Once V_{DS} reduces to less than the V_{DSTL} = 1.2 V and 3 V threshold, the driver transitions from slew mode to switch mode after approximately 320 ns, visible as the sharp rise in V_{GS} to the full gate-drive rail voltage in CH1 and the corresponding current spike on gate current in CH4. The measured delay is within the specification range given in Table 6.



V_{DSTL} = 1.2 V (top) and 3 V (bottom), CH1 is gate voltage, CH2 is drain-source voltage V_{DS}, and CH4 is gate current I_G.

Figure 18: Experimental Waveforms Showing Slew-to-Switch Mode Transition of Low-Side MOSFET

Revision History

Number	Date	Description	Responsibility
–	June 30, 2026	Initial release to Allegro website	M. Kumar

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