



DESIGNING ROBUST SOLID-STATE CIRCUIT BREAKERS WITH ALLEGRO AHV85311 ISOLATED GATE DRIVER OR AHV85003 AND AHV85043 CHIPSET

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ABSTRACT

In modern DC distribution grids, data centers, and electric-vehicle (EV) charging systems, the fast-fault interruption and arc-free operation of the solid-state circuit breaker (SSCB) is becoming essential. This application note provides design guidelines to implement an SSCB using the Allegro AHV85311 isolated gate driver or the Allegro AHV85003 and AHV85043 isolated gate driver chipset. Both solutions feature the Allegro Power-Thru technology. The document focuses on how to drive large parallel silicon-carbide (SiC) MOSFET arrays and how to optimize gate resistor selection to maintain system stability under heavy gate charge (Q_G) loads.

INTRODUCTION

An SSCB leverages power semiconductors to interrupt DC lines. In complex power-supply architectures, the SSCB delivers several advantages; however, it also introduces requirements: Unlike a mechanical breaker, an SSCB requires a high-side gate driver with an isolated power supply on the secondary side. Allegro solutions that can meet these SSCB requirements include the Allegro-patented Power-Thru technology, which greatly simplifies system design.

These solutions include:

- The Allegro AHV85003 and AHV85043 isolated SiC FET driver chipset combined with an external transformer. For information about this product, refer to the AHV85003 and AHV85043 chipset product page on the Allegro website.
- The AHV85311 isolated SiC FET driver, which integrates the primary-side and secondary-side circuitry as well as the transformer within the same package (NK or NL variant). For more information about this product, refer to the AHV85311 product page on Allegro website.

In both AHV85311 driver and the AHV85003 and AHV85043 driver chipset, the isolated secondary-side bias supply is integrated. This allows the capability to achieve higher reliability with significantly fewer external components than discrete floating supply solutions.

This application note details how to implement the AHV85311 circuit or the AHV85003 and AHV85043 chipset circuit for an SSCB application. The AHV85311 isolated gate driver is used as the example, but the information presented is also relevant for the AHV85003 and AHV85043 chipset, unless noted otherwise. Key points are presented to ensure operational stability under very-high- Q_G load conditions. To validate the proposed application, measurements of the capacitive load and the real-world SiC MOSFET application are also presented.

SYSTEM OVERVIEW

A high-performance SSCB is conceptually a high-speed DC switch managed by an intelligent controller. The system is required to monitor line conditions and provide galvanic isolation between the low-voltage control logic and the high-voltage power rail.

The SSCB architecture consists of four primary stages:

- **Power Switch Matrix:** One or more power semiconductors that carry the continuous load current and the interrupt-fault conditions.
- **Isolated Gate Driver:** The AHV85311 acts as the critical bridge that translates logic signals into gate-drive pulses and simultaneously provides isolation.
- **Power-Thru Supply:** Embedded in the gate driver, instead of using an external DC-DC converter, the AHV85311 generates its own secondary-side floating rails (e.g., +18 V/–3V) directly from the primary-side supply (V_{DRV}).
- **Control and Sensing:** A local microcontroller unit (MCU) or field-programmable array (FPGA) monitors the current—e.g., via the Allegro tunneling magnetoresistance (TMR) sensor—and commands the AHV85311 to trip if a fault is detected (using fast comparators).

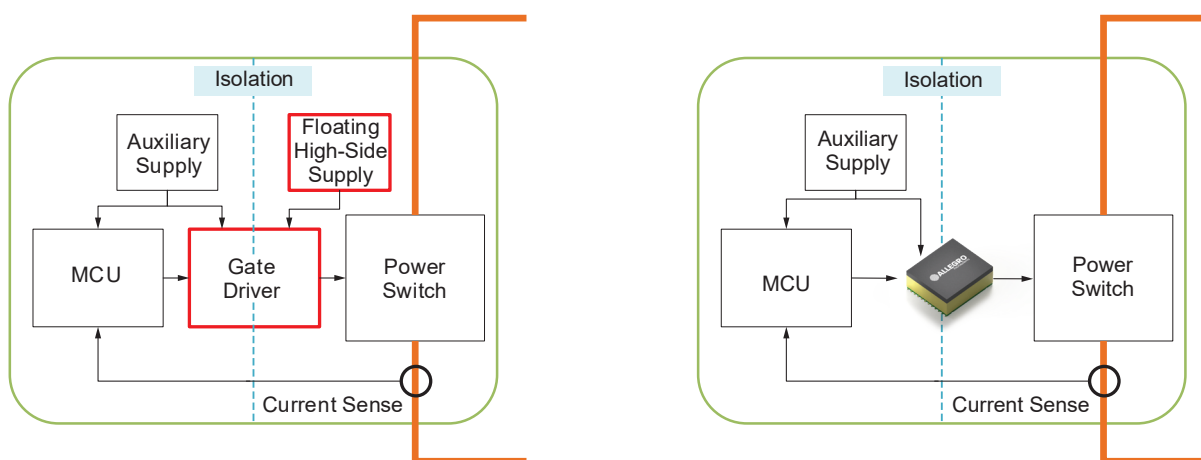


Figure 1: Typical Application Block Diagram without Allegro-Proposed Technology (left) and with the Allegro AHV85311 NK Package (right)

SELECTION OF POWER SEMICONDUCTORS

In the SSCB application, the most commonly selected power-switch technologies are the SiC MOSFET, silicon super-junction MOSFET, insulated gate bipolar transistor (IGBT), and SiC junction field-effect transistor (JFET).

The AHV85311 is designed as a MOSFET isolated gate driver with:

- a regulated positive rail with configurable voltage of 15 V, 18 V, or 20 V, as determined by the selected Allegro part number.
- a negative rail (0 to 5 V), with configurable voltage, as determined by external resistors.

The focus of this application note is the power-switch technology that is typically in the off state, such as a SiC MOSFET or a silicon MOSFET that matches the 15 V, 18 V, or 20 V driving voltage for the on state.

Because an IGBT has the same gate structure, an IGBT can be driven if it can accept a 15 V driving voltage.

Tests show that, for very high Q_G , the Allegro solution successfully drives several power switches in parallel, to achieve a very low value of the on-state drain-to-source resistance ($R_{DS(ON)}$).

OPERATIONS

Turn-On Optimization and UVLO Prevention

To drive the very-high Q_G that results from a MOSFET with extremely low $R_{DS(ON)}$ or a parallel stack of MOSFETs used in this application, during the very-high- Q_G switching, a clearly visible transient voltage reduction occurs on the secondary positive rail (V_{SECP}).

To charge the necessary Q_G in the gate-source capacitance (C_{GS}) when the AHV85311 receives a turn-on command, the AHV85311 is required to transfer energy from the storage capacitor on the secondary-side supply (C_{SEC}) to the gates of the MOSFET array.

The V_{SECP} voltage reduction on C_{SEC} follows the simple charge balance between two capacitors:

Equation 1:

$$\Delta V = (V_{SECP} \times C_{GS}) / (C_{GS} + C_{SEC})$$

where the equivalent series resistance (ESR) and the equivalent series inductance (ESL) contributions are negligible when real-world application values are considered.

Equation 1 is valid until the power transfer from the primary

side feeds the charges of the capacitors, which helps the voltage to increase again toward the correct regulation. After approximately tens of microseconds, additional power from the primary side begins to increase the voltage.

If the driven Q_G is very high (and consequently C_{GS} is very high), to avoid the internal undervoltage-lockout (UVLO) trigger, a limit to the voltage reduction is required.

If V_{SECP} reduces to less than 80% of its setpoint, UVLO becomes triggered.

The V_{SECP} limit (referenced to source) is indicated in the datasheet as:

Equation 2:

$$V_{SECP(UVF)} = 80\% \text{ set point}$$

For example, in the case of the 15 V option:

$$V_{SECP(UVF)} = 0.8 \times 15 = 12 \text{ V}$$

Therefore, the maximum allowed voltage change (ΔV) is 20% of the nominal V_{SECP} .

The easiest solution to avoid a UVLO trigger is to increase the storage capacitance (C_{SEC}) according to the inversion of Equation 1 as follows:

Equation 3:

$$C_{SEC} > [(V_{SECP}/\Delta V) - 1] \times C_{GS}$$

The, from Equation 2 and Equation 3, the following rule is derived:

Equation 4:

$$C_{SEC} > 4 \times C_{GS}$$

The effective capacitance requirement for the secondary storage—considering the multilayer ceramic capacitor (MLCC) derating for DC bias, temperature, and worst-case tolerance—is at least four times the gate capacitance of the power switches. This is the numerical limit that achieves a voltage reduction of 20%.

To ensure safe operation, addition of a sufficient margin to the Equation 4 result is recommended. To maintain a margin that sufficiently exceeds the UVLO threshold, the suggestion is:

Equation 5:

$$C_{SEC} > 6 \times C_{GS}$$

Simultaneous consideration of the maximum limit for C_{SEC} is required. This limit relates to linear regulation stability. In the datasheet, the maximum recommended capacitor value is 1 μF .

For an X7R MLCC, 1 μF , 10%, 50 V capacitor (e.g., Murata GCM21BR71H105KA03K), the effective capacitance

required for the worst case, considering derating and tolerance, is approximately 600 nF.

(Consideration of the same value is required for the capacitors between V_{SECP} , V_{SECN} , and the source pins).

To increase stability, an additional 2.2 nF feed-forward capacitor is required on the negative bias regulator, between the source pin and the VFB pin (see the Application Schematic—Layout Recommendation section).

According to Equation 5:

If $C_{GS} < 100$ nF and C_{SEC} is an X7R, 1 μ F, 10%, 50 V MLCC capacitor: Selection of $R_{gate(ON)}$ is according to system requirements, without additional constraints.

If $C_{GS} > 100$ nF and C_{SEC} is an X7R, 1 μ F, 10%, 50 V MLCC capacitor: Selection of $R_{gate(ON)}$ is according to system requirements plus an additional requirement for a longer turn-on time constant. The longer time constant slows the transient to allow the power transfer from the primary side to sustain the output voltage. Experimentally, the time needed to recover the voltage regulation depends on the output load and is some tens of microseconds. It can be considered a time constant of at least 10 μ s:

$$R_{gate(ON)} > (10 \mu s) / C_{GS}$$

The C_{GS} value can be derived from the power-switch data-sheet.

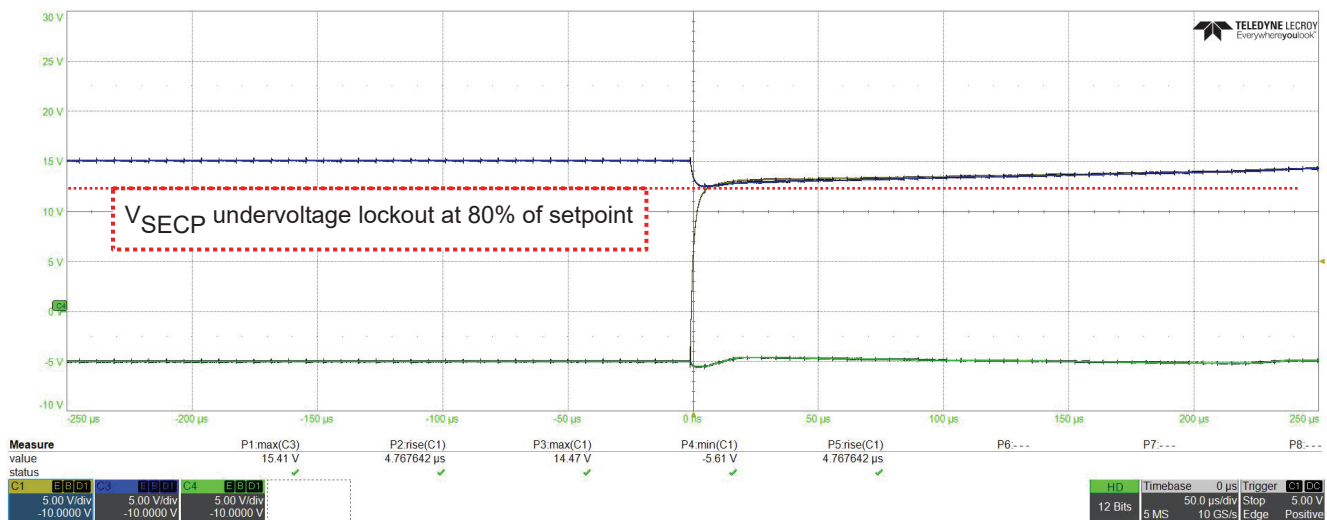
In this application, the turn-on speed is not a critical requirement. Therefore, an increased $R_{gate(ON)}$ is allowable.

The AHV85311 has split outputs, which enables a separation of the $R_{gate(ON)}$ and $R_{gate(OFF)}$ outputs and a longer turn-on transition. This feature does not affect turn-off speed, a critical requirement.

The dimensioning guidelines provided in this section use simple formulas. Experimental tests to fine-tune the component values for the specific application is always strongly recommended.

For example: In an additional test performed with a real-world SiC MOSFET application (implemented with a 1200 V, 9 m Ω Wolfspeed C4MS009120QT) and C_{SEC} (implemented with an X7R, 1 μ F, 10%, 50 V MLCC), the MOSFET gate-source capacitance is:

$$C_{GS} = 8.5 \text{ nF and } Q_{G(TOT)} = 340 \text{ nC (typical)}$$



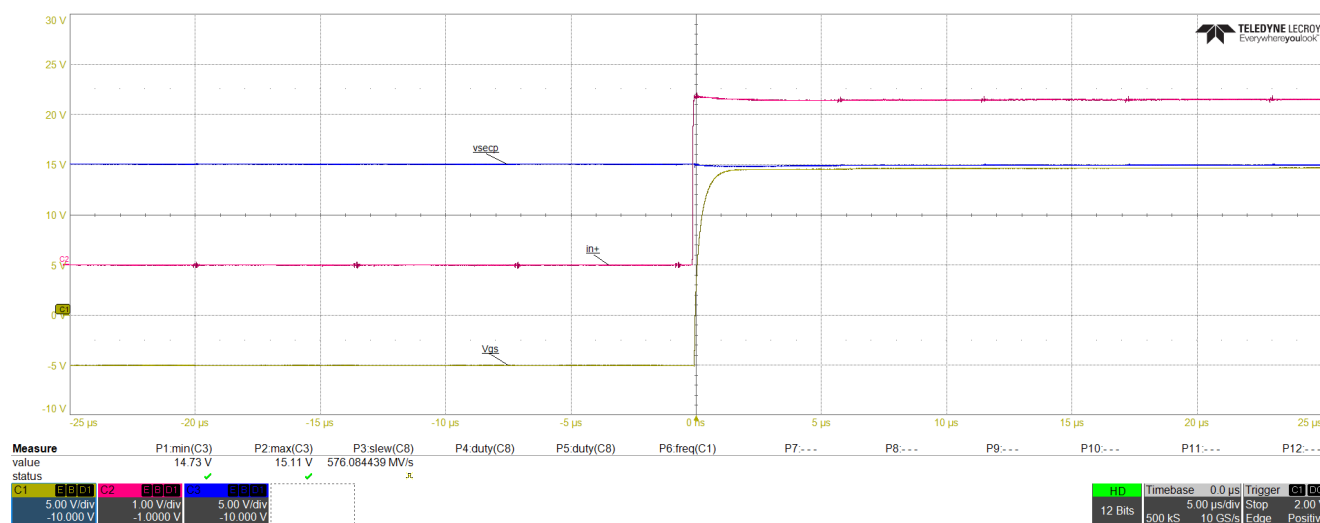
CH1: Gate-to-source voltage

CH3: Positive secondary-side voltage referenced to V_{SECP} source

CH4: Negative secondary-side voltage referenced to V_{SECN} source

Turn-on transient with effective $C_{SEC} = \sim 400$ nF, $C_{GS} = 100$ nF, equivalent to $Q_G = \sim 1800$ nC and $R_{gate(ON)} = 10 \Omega$. C_{SEC} touches the safe limit of UVLO. In this case, UVLO is not triggered, but a UVLO condition must be avoided.

Figure 2: Turn-On Transient At Limit of UVLO Area



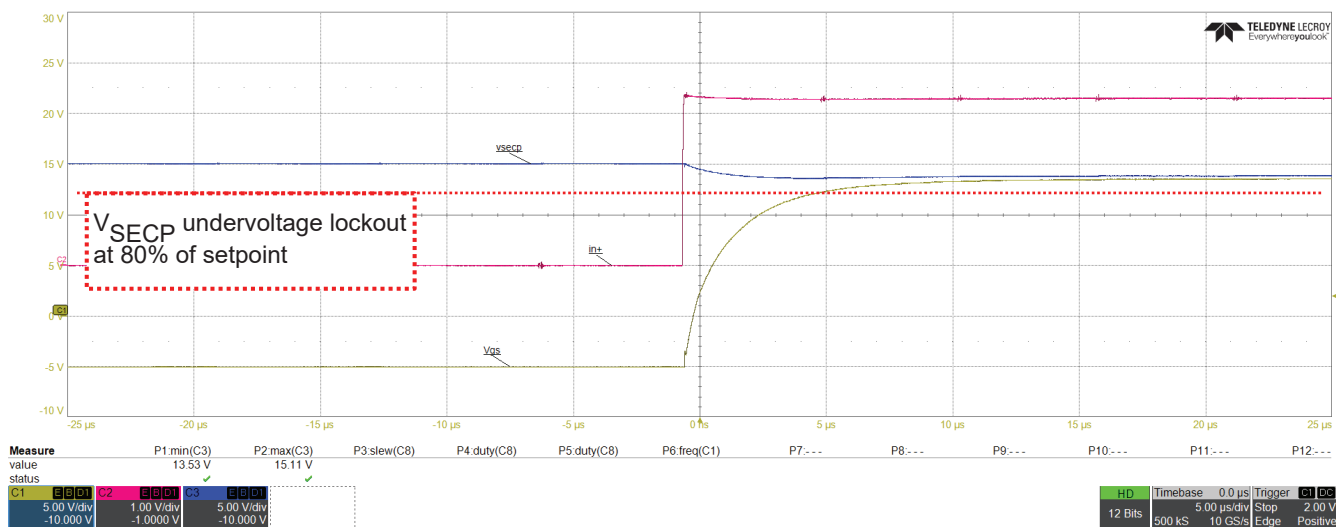
CH1: Gate-to-source voltage

CH2: Logic input signal IN+

CH3: Positive secondary-side voltage referenced to source V_{SECP}

Turn-on transient with 1× Wolfspeed C4MS009120QT ($C_{GS} = 8.5$ nF) and $R_{gate(ON)} = 10$ Ω. C_{SEC} is X7R, 1 μF, 10%, 50 V MLCC (achieving effective $C_{SEC} = \sim 600$ nF). V_{SECP} reduction is limited and far from UVLO area.

Figure 3: Turn-On Transient with Real-World MOSFET Application (1× Wolfspeed C4MS009120QT)



CH1: Gate-to-source voltage

CH2: Logic input signal IN+

CH3: Positive secondary-side voltage referenced to source V_{SECP}

Turn-on transient with 8× Wolfspeed C4MS009120QT ($C_{GS} = 68$ nF) and $R_{gate(ON)} = 10$ Ω. C_{SEC} is X7R, 1 μF, 10%, 50 V MLCC (achieving effective $C_{SEC} = \sim 600$ nF). Equation 5 is respected, and V_{SECP} reduction is limited and is far from the UVLO area.

Figure 4: Turn-On Transient with Real-World MOSFET Application (8× Wolfspeed C4MS009120QT)

ON STEADY-STATE OPERATION

During steady-state operation, with current carried on the closed power switch, the voltage supply at the gate is constant and is equal to the setpoint. The Allegro Power-Thru technology regulates this voltage to ensure it remains at this level. To ensure power transmission across the isolation barrier, the primary side has an internal isolated power supply that sends **refresh pulses**. In this application, the voltage ripple on the gate-to-source voltage can be considered negligible.

Turn-Off Speed and Negative Bias

The turn-off speed of an SSCB application is a critical requirement.

The split output of the AHV85311 allows use of a very low off-state gate resistance ($R_{\text{gate(OFF)}}$) without affecting the turn-on constraints: It is even possible to use a $0\ \Omega$ resistor for $R_{\text{gate(OFF)}}$ and to rely on the internal $1\ \Omega$ of AHV85311.

When the IN+ input is used for turn-on and turn-off of the power MOSFET, the typical propagation delay of the AHV85311 is 85 ns, as specified in the datasheet, with very good part-to-part variation of 10 ns.

During a turn-off transient, V_{SECP} increases; however, unlike the period during a turn-on transient with UVLO, the overvolt-

age threshold is not critical. This is because the discharge path of the main gate primarily occurs through the negative bias regulator and only partially occurs through the positive bias supply.

During turn-off, the AHV85311 supplies the gate with a negative bias. This ensures the robust switch-off of the power MOSFET. With an external resistor divider, this negative bias is configurable between 0 and $-5\ \text{V}$.

The linear regulator that ensures the negative bias voltage with its output capacitance is on the main discharge path of the gate. As a result, during a turn-off transient, the constraint of concern is regulation of the negative bias voltage: Verification of this constraint is required. During the transient, the negative bias voltage increases and can affect the real-world negative voltage witnessed by the gate.

Tests with a real-world SiC MOSFET application (Wolfspeed C4MS009120QT, 1200 V 9 m Ω), with eight devices in parallel, demonstrate this behavior. The recommendation to achieve a proper negative gate voltage during the turn-off transient is to maintain the negative-voltage setpoint in the steady state at $-5\ \text{V}$.

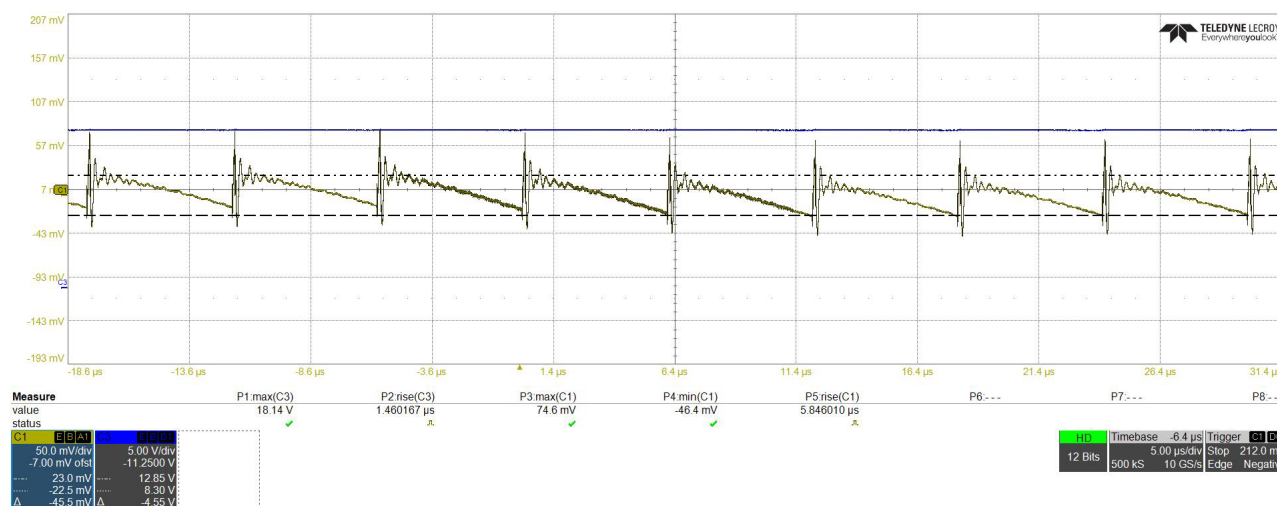
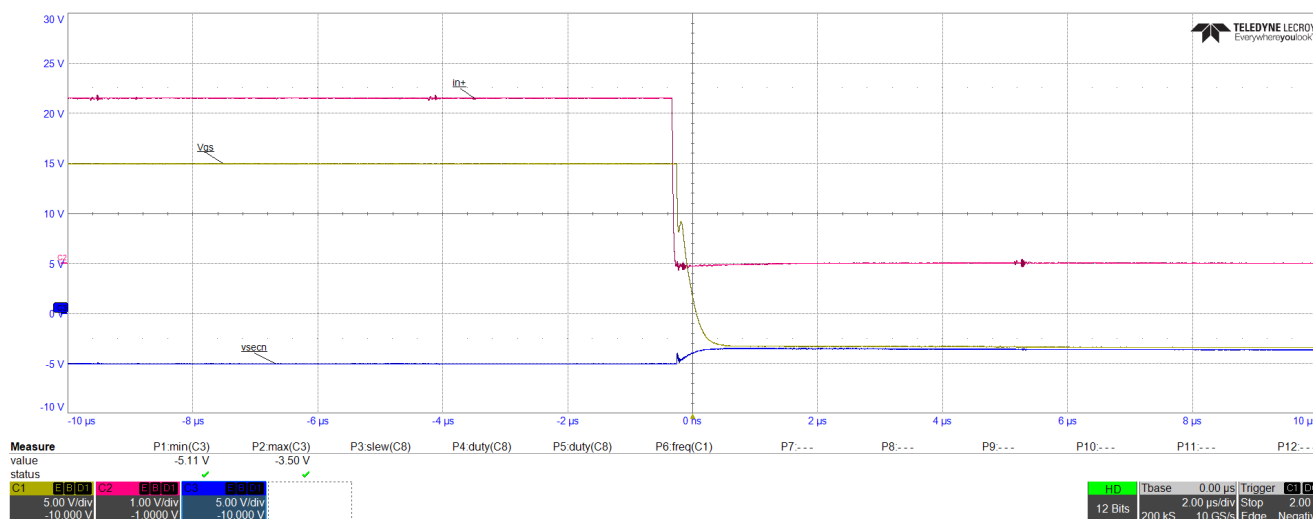


Figure 5: Gate-to-Source Voltage during On Steady-State Operation



CH1: Gate to Source voltage

CH2: Logic input signal IN+

CH3: Negative secondary side voltage referenced to source VSECN

Turn-off transient with 8× Wolfspeed C4MS009120QT for: $R_{gate(OFF)} = 0 \Omega$. C_{SEC} is X7R, 1 μ F, 10%, 50 V MLCC V_{SECN} effective voltage during transient -3.5 V.

Figure 6: Turn-Off Transient at -5 V with Real Application MOSFET (8× Wolfspeed C4MS009120QT)

Thermal Behavior

During steady-state operations, Q_G does not switch, so it does not have an impact. Therefore, the internal power dissipation is limited to the losses of the internal power supply. Temperature increase is minimal, which allows operation at very high ambient temperature.

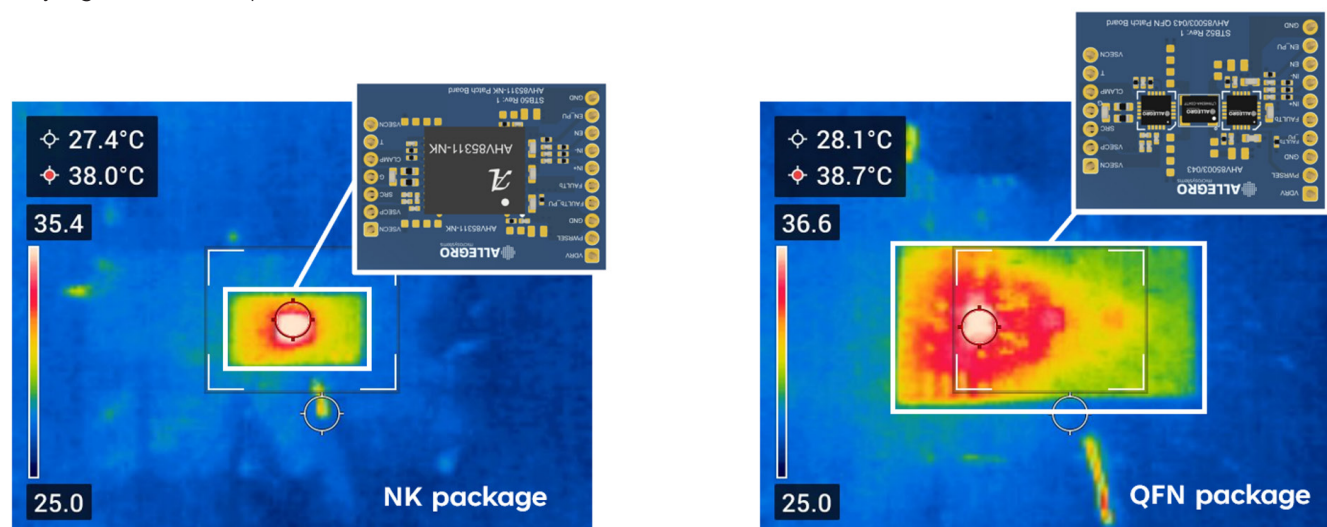


Figure 7: Thermal Map at Ambient Temperature during On Steady State Operation for AHV85311 (NK Package, Left) and AHV85003 and AHV85043 Chipset (QFN Package, Right)

APPLICATION SCHEMATIC—LAYOUT RECOMMENDATION

Proper operation in the SSCB application requires the following (with reference to the application schematic available in the datasheet, shown in Figure 8 and Figure 9):

- Use IN+ for the driving signal, not EN. EN is the enable pin for the secondary power supply, and use of EN for fast transients is not recommended.
- Tie IN- to GND.
- Select the value of any gate resistor according to the system requirements, especially requirements for timing constraints and for V_{SECP} UVLO, as described in this application note.
- Increase the limits of C_{VSN} , C_{VSP} , and C_{VNS} such that they ensure stability and minimize (as much as practicable) the voltage transient that occurs during a very-high- Q_G turn-off or turn-on operation.
 - The suggested capacitor is an X7R, 1 μ F, 10%, 50 V MLCC (e.g., Murata GCM21BR71H105KA03K).
 - The suggested negative bias resistor divider:
 - ◆ Implements $R_{NT} = 40.2 \text{ k}\Omega$ and $R_{NB} = 10 \text{ k}\Omega$ to ensure a setpoint of -5 V , to achieve the proper negative voltage during fast turn-off transient.
 - ◆ Includes a required additional 2.2 nF capacitor, added in parallel to R_{NT} to increase stability.
- Strictly adhere to the layout guidelines. Do not implement a solution that does not adhere to these guidelines.

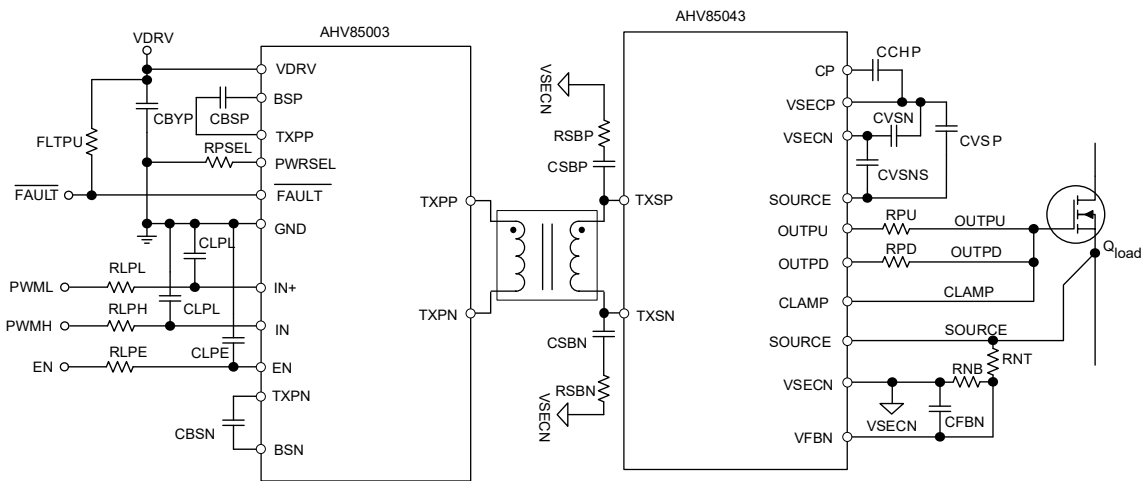


Figure 8: AHV85003 and AHV85043 Chipset, Application Schematic

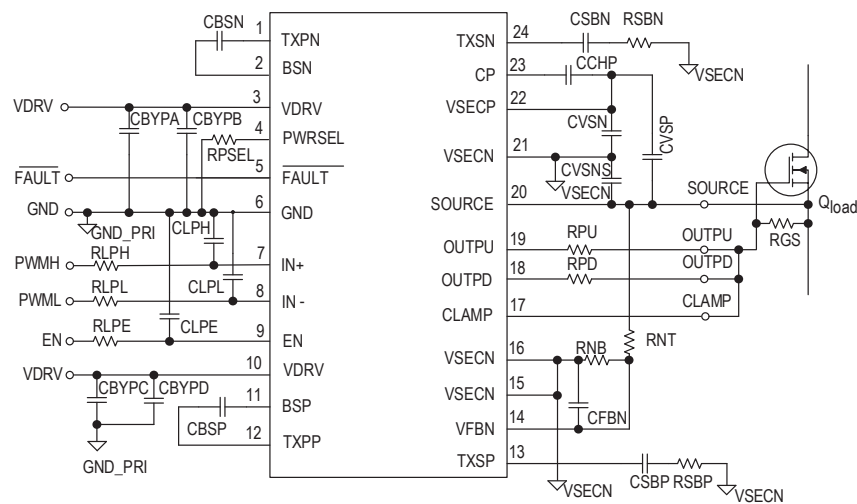


Figure 9: AHV85311 Application Schematic

ISOLATION REQUIREMENTS (AHV85311 ONLY)

In either the NK or NL package, the AHV85311 is a reinforced isolation device: The isolation transformer is embedded in the package. With minimum creepage of 8 mm and 1200 Vrms working voltage, the AHV85311 can fulfil stringent isolation requirements.

AHV85003 and AHV85043 chipset is used in combination with an external transformer; therefore, the design of the external transformer can be used to manage the isolation rating. Allegro suggests the use of already validated transformers, available in basic and functional isolation variants.

HOW TO USE EVALUATION BOARD (EVB) TO TEST SSCB APPLICATION

Allegro evaluation boards (EVBs) are available for test and evaluation of an Allegro device in the SSCB application. Currently available Allegro EVBs are shown in Table 1.

Table 1: Currently Available Allegro EVBs for AHV85311 Driver or AHV85003 and AHV85043 Chipset Driver

Allegro EVB Part Number	Gate Driver	Package	Voltage (V)
APEK85311K15NL-08-T	AHV85311	NL	15
APEK85311K18NL-08-T	AHV85311	NL	18
APEK85311K20NL-08-T	AHV85311	NL	20
APEK85311K15NK-08-T	AHV85311	NK	15
APEK85311K18NK-08-T	AHV85311	NK	18
APEK85311K20NK-08-T	AHV85311	NK	20
APEK85003K15ES-08-T	AHV85003	ES	15
APEK85003K18ES-08-T	AHV85003	ES	18
APEK85003K20ES-08-T	AHV85003	ES	20

To use an Allegro EVB shown in Table 1 for the SSCB application specifically:

1. The EVB default gate-resistance values are:

$$R_{\text{gate(ON)}} = 10 \, \Omega \text{ and } R_{\text{gate(OFF)}} = 1 \, \Omega$$

To drive $C_{\text{GS}} > 100 \, \text{nF}$, increase $R_{\text{gate(ON)}}$ as described in the Turn-On Optimization and UVLO Prevention section of this document.

2. Provide an external connection from the selected power switch to the gate and source pins. The EVB includes only the single driver circuit.

For additional information, refer to the part-specific user guide.

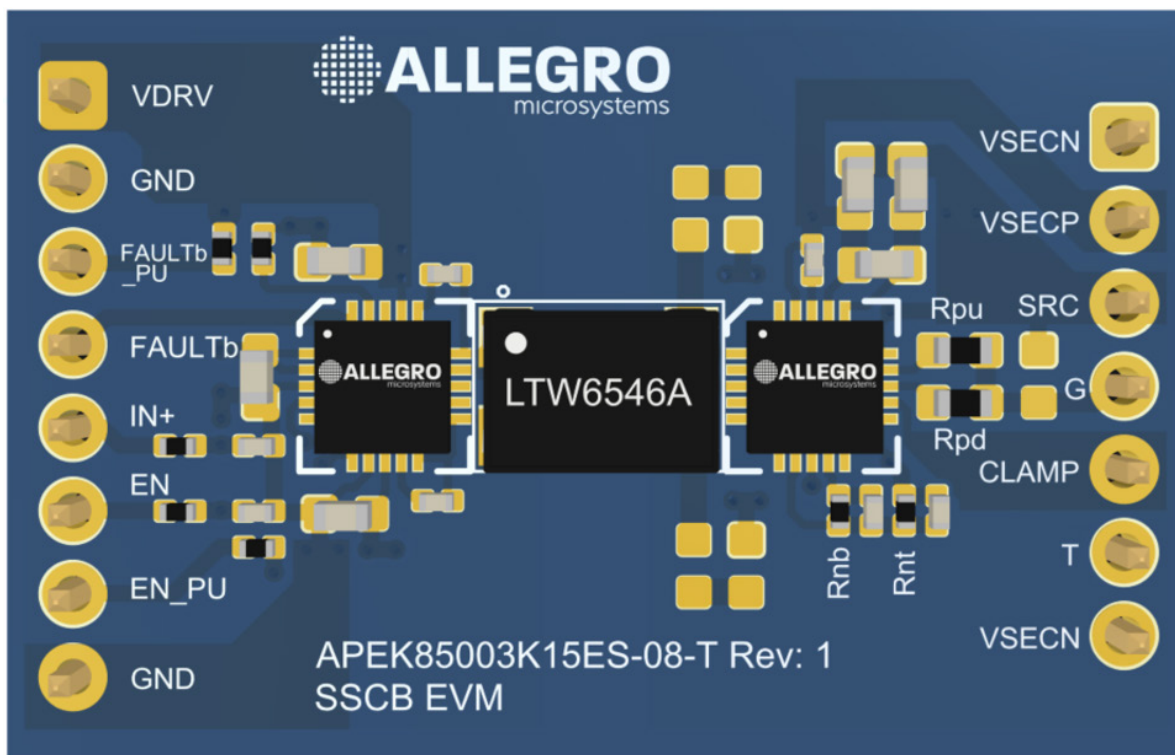


Figure 10: AHV85003 and AHV85043 Chipset (QFN Package) with External Transformer Single Channel EVB, Available in 15 V, 18 V, and 20 V Variants

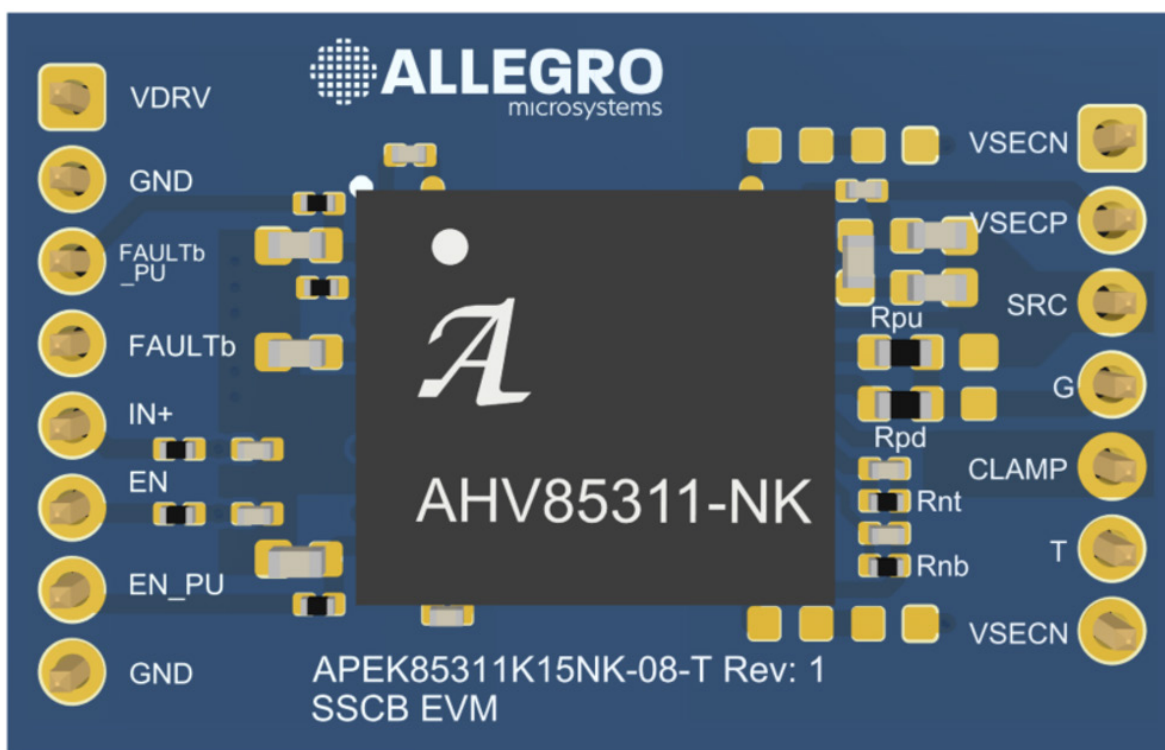


Figure 11: AHV85311 (NK Package) Single Channel EVB, Available in 15 V, 18 V, and 20 V Variants

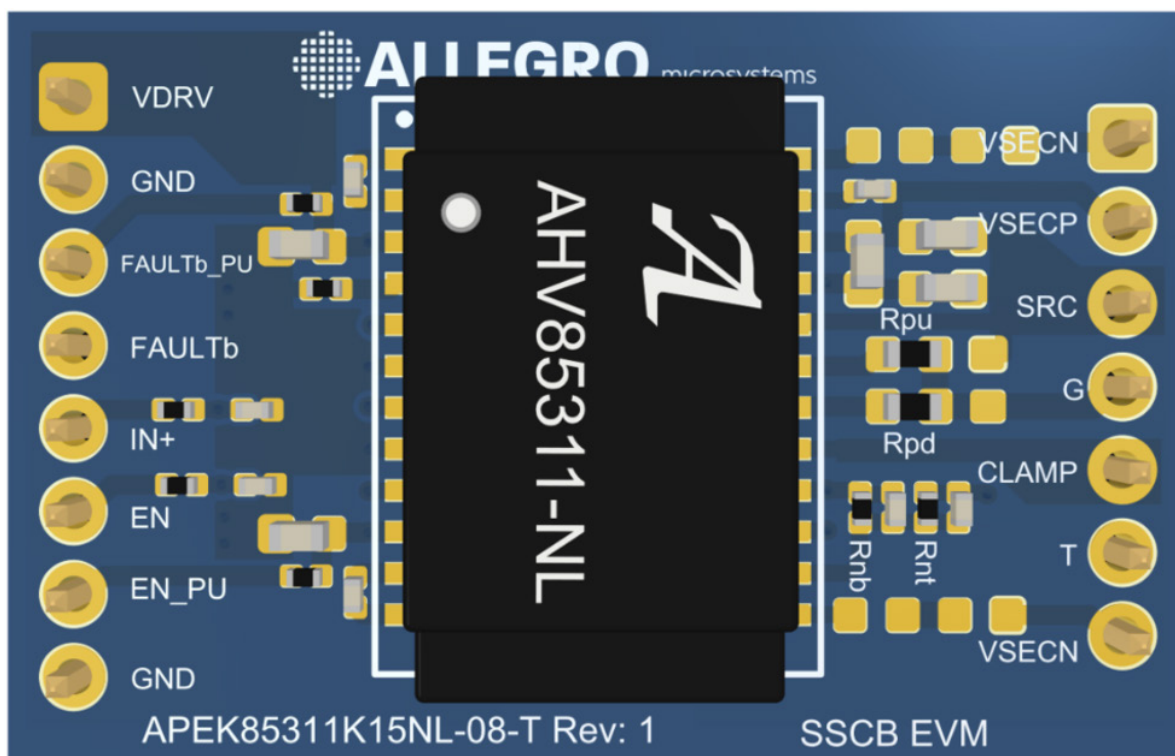


Figure 12: AHV85311 (NL Package) Single Channel EVB, Available in 15 V, 18 V, and 20 V Variants

CONCLUSION

The Allegro integrated Power-Thru gate drivers AHV85311 and AHV85003 and AHV85043 chipset are suitable for solid-state circuit-breaker application, enabled by the isolation feature and internal power supply for the secondary floating supply. These devices can simplify system design, reducing the component count.

Revision History

Number	Date	Description	Responsibility
–	September 3, 2026	Initial release	Davide Cairoli

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