



# AHV85311 SELF-POWERED ISOLATED SiC GATE DRIVER WITH BIPOLAR OUTPUT AND SECONDARY SIDE SNUBBERS FOR IMPROVED CMTI PERFORMANCE

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## ABSTRACT

The AHV85311 gate driver is optimized for driving discrete SiC FETs in applications such as Solid-State Circuit Breakers, data center PSUs, automotive On-Board-Chargers (OBC), solar inverters, and industrial robotics. With its integrated isolation transformer, it provides a self-powered isolated gate drive solution that is ideal for multiple applications and topologies.

All components with an isolation barrier have an inherent primary-to-secondary capacitance ( $C_{PS}$ ). This parasitic capacitance plays a crucial role in the common-mode transient immunity (CMTI) and EMC performance of the final application system.

## INTRODUCTION

The AHV85311 isolated SiC FET driver uses Allegro MicroSystems' patented PowerThru™ technology combined with an integrated isolation transformer.

In a typical SiC FET based converter, very high-voltage, fast-occurring transitions ( $dV/dt$ ), are generated which result in a common-mode current flowing in  $C_{PS}$ , which creates unwanted noise and power losses which must be managed within the system design.

Furthermore, these common-mode transients can disrupt a gate drivers' operation or signal integrity.

$C_{PS}$  is a parasitic component generally related to the physical construction of the component or components spanning the isolation boundary. This not only includes the isolated gate driver but also includes the PCB and any other components spanning the boundary.

Elimination of  $C_{PS}$  is not possible, but minimization of it results in minimization of the effects of common-mode transients. The integrated transformer of the AHV85311 forms the isolation barrier, and the  $C_{PS}$  is less than 4.2 pF, which is 10 to 20 times less than that of a typical external DC-DC converter module used with some gate driver solutions.

A feature of the AHV85311 is the ability to improve the CMTI performance with the inclusion of a snubber pair on the secondary side.

This application note details how to select the snubber components and the impact these components have on the overall system.

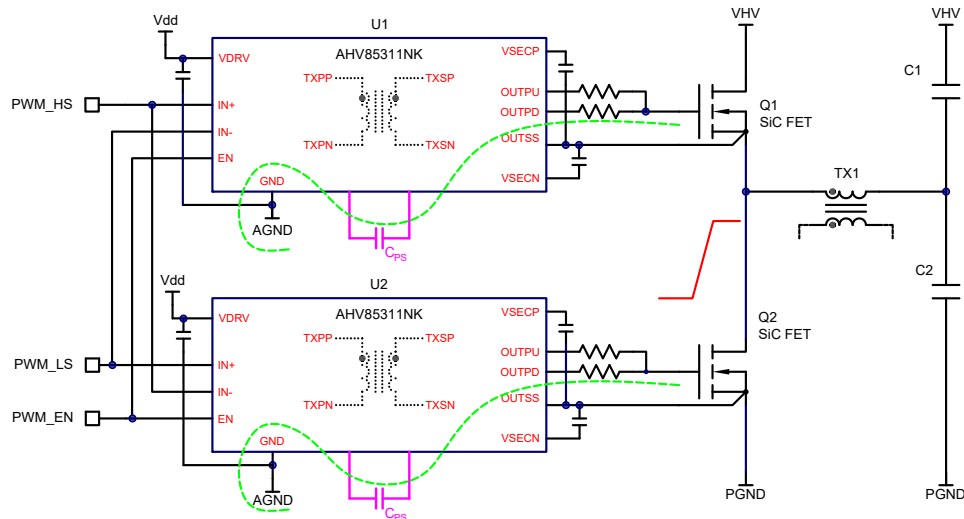


Figure 1: AHV85311 Typical Application Block Diagram

Figure 1 shows a typical application block diagram using the AHV85311 gate driver.

Shown here is the parasitic common mode capacitance,  $C_{ps}$ , of each isolated gate driver. It is important to note that this is not the only common mode capacitance that spans the isolation boundary.

In operation, the voltage at the switch node transitions from PGND to VHV or VHV to PGND as the power FETs are switched. This transition can happen very fast; of the order of nano seconds.

The resulting  $dV/dt$  results in a current in CPS of:

Equation 1:

$$i(t) = C_{ps} \frac{dV}{dt}$$

It is important to note that the same  $dV/dt$  event can be generated in a number of ways. Figure 2 shows a 100 V/ns  $dV/dt$  event generated from three different voltage levels (100 V, 500 V and 1000 V). It is important to note here that while the resulting capacitor current has the same amplitude in all cases, since the  $dV/dt$  is constant, the duration of the current pulse is different in each case.

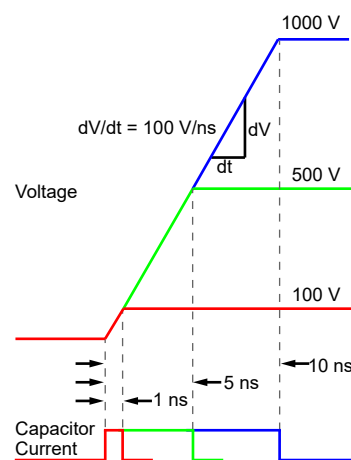


Figure 2:  $dV/dt$  events

## COMMON MODE TRANSIENT IMMUNITY TEST

A full explanation of CMTI testing is beyond the scope of this application note. There is no single standard for CMTI. For magnetic isolated couplers IEC 60747-17 section 6.7 defines the methods to measure the common-mode transient immunity (CMTI) of a coupler in both static and dynamic operation, under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse ( $dV_{CM}/dt$ ).

IEC 60747-17 section 6.7.3 also specifies precautions to be observed to obtain accurate CMTI test results.

Figure 3 below shows a typical CMTI test circuit applied to a typical AHV85311 application.

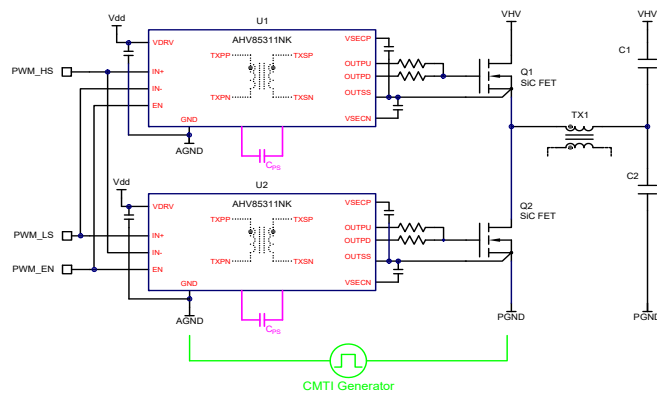


Figure 3: Typical CMTI Test Set Up

## IMPROVING THE CMTI PERFORMANCE OF THE AHV85311

The AHV85311 is specified for CMTI > 150 V/ns with secondary side snubbers ( $C_{SBP} = C_{SBN} = 470 \text{ pF}$ ,  $R_{SBP} = R_{SBN} = 36 \Omega$ ) fitted on TXSP and TXSN.

However, if the system does not achieve the desired CMTI performance because of increased primary to secondary isolation capacitance, this performance can be improved with the inclusion of two simple snubbers on the secondary side, as shown in Figure 4.

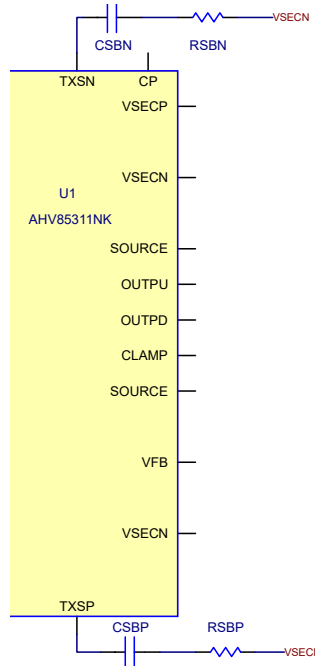


Figure 4: Secondary side snubbers

The calculation of the required snubber component values requires a measurement of the total primary-to-secondary isolation capacitance,  $C_{IO}$ , of the system. The measurement method for determining this capacitance is described in IEC 60747-17 section 6.2.

This capacitance is distributed over the number of isolated drivers used in the system, and the  $C_{PS}$  of each driver can be determined as:

Equation 2:

$$C_{PS} = \frac{C_{IO}}{\text{Number of isolated drivers}}$$

Knowing the values:

$C_{PS}$ , primary-to-secondary capacitance

$V_{CM}$ , magnitude of common mode voltage

$dV_{CM}/dt$ , the slew rate of the common mode pulse

the required snubber values can be determined from:

Equation 3:

$$R_{SN} = \text{Min of} \left[ \frac{12}{\frac{1}{2} C_{PS} \frac{dV_{CM}}{dt} - 12e^{-3}} \right] \text{ or } 1 \text{ k}\Omega$$

$$C_{SN} = \text{Max of} \left[ \frac{2 V_{CM}}{R_{SN} \frac{dV_{CM}}{dt}} \right] \text{ or } 50 \text{ pF}$$

The capacitor chosen should be a good quality ceramic capacitor with an X7R or better dielectric and a minimum voltage rating of  $(V_{SECP} - |V_{SECN}|)$  plus a recommended margin of at least 30%.

The resistor chosen should have a minimum power rating that can be determined from:

Equation 4:

$$P_R = \text{max of} ((V_{SECP} - V_{SECN})^2 C_{SN} F_{sw})$$

or

$$((V_{SECP} - V_{SECN})^2 C_{SN} 150k)$$

In the system application, the snubbers should be located close to the AHV85311 TXSP and TXSN pins with a low impedance path to the VSECN pins. For full details of PCB layout considerations for the AHV85311 see the "[AHV85311NK PCB Layout Guide](#)"

## EFFECT OF ADDING SNUBBER FOR CMTI CONCLUSION

Adding these snubbers does introduce increased power dissipation in the circuit. Because these snubbers are on the secondary side that receives its energy from the PowerThru mechanism, this uses energy that otherwise would be available to drive the FET Qg. For this reason, the snubber size should be designed to be the minimum value (minimum  $C_{SN}$ , maximum  $R_{SN}$ ) to achieve the required CMTI performance.

Refer to the AHV85311 datasheet to determine reduction in energy available to drive the load FET.

It should be noted that the AHV85311 gate driver solution is specified to deliver up to 130 nC of gate charge. Through use of the PWRSEL function, three power-level settings, low, medium and high. For full details see the AHV85311 datasheet.

Common-Mode Transient Immunity, CMTI, is an important test for isolated gate drivers to ensure reliable and safe operation in high frequency power switching environments.

The overall CMTI performance of a system is largely dependent on the total parasitic capacitance across the isolation boundary.

The AHV85311 can achieve CMTI performance in excess of 150 V/ns.

This performance can be further refined by dimensioning the two resistor-capacitor (RC) snubbers on the secondary side.

*Revision History*

| Number | Date             | Description                        | Responsibility |
|--------|------------------|------------------------------------|----------------|
| –      | October 21, 2026 | Initial release to Allegro website | Dermot Dobbyn  |

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