OPERATION OF A89110 THREE-PHASE INTEGRATED MOSFET DRIVER AT HIGH PWM FREQUENCY IN ROBOTIC ACTUATORS

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ABSTRACT

This application note describes how the A89110 three-phase integrated MOSFET driver performs when the pulse-width-modulation (PWM) frequency (f_{PWM}) greatly exceeds the typical 24 kHz.

To demonstrate device performance, tests were performed at 100 and 200 kHz, at room temperature and at 85°C ambient temperature, for a total of four tests. In these tests, the device drives a three-phase RL load (3.3 Ω + 20 µH per phase) with the respective sinusoidal PWM frequency and operating temperature. The supply (V_{BB}) is 24 V, and phase current is 1.18 to 1.30 A RMS.

All four tests display operation without faults. The charge pump is shown to maintain a differential between the charge-pump output voltage and the supply voltage ($V_{CP} – V_{BB}$) in the range of 5.89 V to 6 V, which is within the range specified in the datasheet. An estimated loss comparison at each PWM frequency shows how switching losses and dead-time losses grow with frequency.

These tests provide information that helps a designer determine a PWM frequency that is within the thermal limits of the device.

INTRODUCTION

The A89110 is a three-phase N-channel power-MOSFET driver with integrated MOSFETs, charge-pump regulator, integrated dead time, and gate drive with serial-port-interface (SPI) programmable slew rate. It operates from 4.5 V to 40 V. The A89110 datasheet [1] provides a typical motor PWM frequency (f_{PWM}) of 24 kHz. However, the datasheet does not specify an absolute maximum. This is because the practical limit to the PWM frequency depends on device timing (i.e., propagation delay, dead time rising/falling, and slew time) and thermal dissipation.

Many robotic actuators—such as those in dexterous hands, finger joints, and compact servo drives, which commonly use small, low-inductance brushless DC (BLDC) motors on 12 V or 24 V buses—benefit from higher f_{PWM} because:

- Current ripple is reduced. Ripple scales with $1/f_{PWM}$. Therefore, when a system switches from a PWM frequency of 100 kHz to 200 kHz, the ripple reduces by roughly half. This reduces torque ripple and motor copper loss.
- More current-loop bandwidth is available for finer position and force control.
- Audible noise is not created.
- Filter parts are smaller or are able to be eliminated.

This application note answers two questions:

- Can the A89110 charge pump and gate drive continue to operate from 100 kHz to 200 kHz, at room temperature and when hot?
- How do the device losses scale with switching frequency?

[1] A89110, Automotive, Three-Phase Integrated MOSFET Driver, Allegro MicroSystems Datasheet, Rev. 3, March 20, 2026. https://www.allegromicro.com/-/media/files/datasheets/a89110-datasheet.pdf

TEST SETUP

Tests performed to determine if the device continues to operate at a PWM frequency that greatly exceeds the typical 24 kHz are set up as described here. All tests use a single A89110 device on the Allegro A89110 evaluation board, connected as a three-phase bridge. The test conditions selected create conditions similar to a real robotic actuator drive and allow repeatable measurements. The test conditions are summarized in Table 1, and the bench setup is shown in Figure 1.

Power Stage and Load

In the test setup, the board runs from a 24 V bench supply. This supply matches the 24 V bus used in many robotic systems. The evaluation board has two 22 µF ceramic capacitors from VBB to GND. These capacitors provide local decoupling. Each phase drives a star-connected resistive load (RL) of 3.3 Ω in series with 20 µH. The low inductance is typical of the small BLDC motors used in robotics for dexterous hands and compact servo joints. At this inductance, the phase current ripple depends greatly on the PWM frequency, so the benefit of operation at a higher PWM frequency is apparent. With this load and modulation index (M_A = 0.62 to 0.65), the RMS phase current (I_{RMS}) is in the range of 1.18 to 1.30 A.

Control and Modulation

An STM32 microcontroller (NUCLEO-F446RE) generates the PWM signals. This MCU drives all six control inputs (HA/LA, HB/LB, HC/LC) in independent-control mode, which is the default setting (CTL = 0) of the A89110. At PWM frequencies of 100 kHz and 200 kHz, the MCU produces a sinusoidal PWM with a 1 kHz fundamental and a modulation index of 0.62 to 0.65. The MCU does not add dead time. The integrated dead time of the A89110 provides cross-conduction protection.

Gate-Drive Configuration

Configuration of the A89110 is performed over SPI using the A89110 graphical user interface (GUI) on a PC. All tests use the fastest slew setting, TSR/TSF = 0, which provides a typical output transition time (rise time, t_r, and fall time, t_f) of 50 ns. In each short PWM period, the fast edges maintain low switching losses and provide the longest usable on-time. The slew setting also sets the integrated dead time. At TSR/TSF = 0, the typical dead time on the rising edge is 500 ns and the typical dead time on the falling edge is 410 ns.

Temperature

Tests are performed at room temperature (≈25°C) and at 85°C ambient, with the evaluation board inside an environmental chamber. At the frequencies under test, the wiring between the controller and the A89110 is required to be short, so the controller board is placed close to the evaluation board. This limits the hot test to 85°C, which is less than the 105°C maximum operating ambient temperature of the device.

Measurements

A 1 GHz oscilloscope captures the three phase output voltages (OUTA, OUTB, OUTC), the OUTA phase current, and the charge-pump voltage, $V_{CP} – V_{BB}$ (measured differentially). Because the charge pump supplies the high-side gate drivers and the charge-pump load increases with switching frequency, the primary measurement of these tests is $V_{CP} – V_{BB}$: If $V_{CP} – V_{BB}$ reduces to less than the undervoltage threshold ($V_{CP(OFF)}$, 3.1 V, typical, falling), the gate drive becomes disabled. In comparison to the 6.05 V measured without a load and without PWM, this data set indicates how much margin remains at high frequency.

Table 1: Test Conditions

Parameter	Value
Device	A89110 on the Allegro A89110 evaluation board
Supply	V_{BB} = 24 V
Load	RL load, 3.3 Ω + 20 µH per phase
Controller (MCU)	STM32 (NUCLEO-F446RE)
Modulation	Sinusoidal PWM, 1 kHz fundamental
PWM Frequency (f_{PWM})	100 kHz and 200 kHz
Slew	TSR/TSF = 0, the fastest setting (50 ns typical)
Dead Time	Internal to the A89110, set by the slew setting
Ambient	≈25°C (room) and 85°C
Instruments	1 GHz oscilloscope, V_{BB} power supply, PC running the A89110 GUI
Measured Signals	OUTA, OUTB, OUTC voltage, OUTA phase current, $V_{CP} – V_{BB}$ (differential)

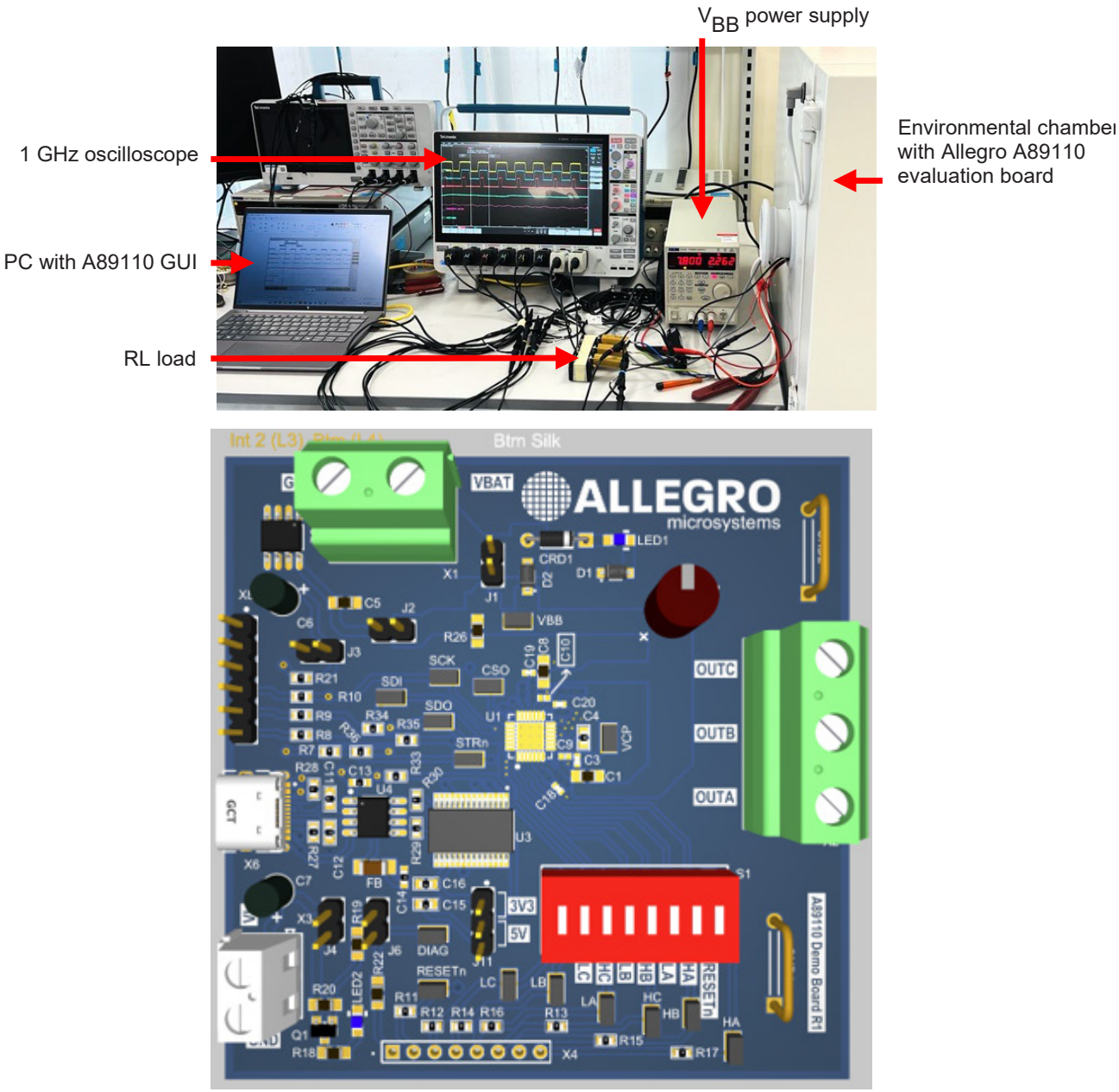


Figure 1: Test Setup and A89110 Evaluation Board

MEASURED RESULTS

Four tests covered the two PWM frequencies (100 kHz and 200 kHz) at the two ambient temperatures ($T_A \approx 25°C$ and 85°C). Tests 1.1 and 1.2 are at room temperature, and Tests 2.1 and 2.2 repeat the same frequencies at 85°C. All tests use the setup described in the Test Setup section: V_{BB} is 24 V, the fastest slew setting is selected (TSR/TSF = 0), and the per-phase RL is 3.3 Ω + 20 µH. The modulation index is 0.65 in every test except Test 2.2, which is 0.62. This provides phase currents of 1.18 to 1.30 A RMS.

Criteria used to judge device performance in each test are:

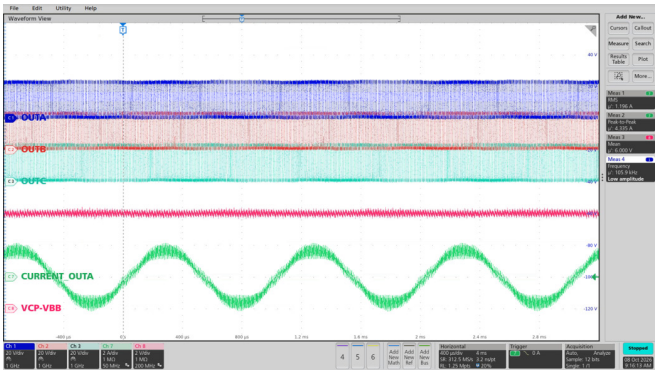
- ***Uninterrupted, fault-free operation:*** Continuous switching is required without the occurrence of a bridge-disabling fault (V_{CP} undervoltage [VCP], V_{DS} overvoltage [DSO], or overtemperature shutdown [OT]) during the test.
- ***Charge-pump margin:*** $V_{CP} – V_{BB}$ is required to remain at a voltage that is much greater than the undervoltage threshold ($V_{CP(OFF)}$ = 3.1 V typical, falling) and within the 5.4 to 6.6 V range specified for $V_{BB} > 7$ V.
- ***Clean switching:*** All three phase outputs are required to switch cleanly, and the phase current is required to follow the 1 kHz sinusoidal reference.

The results are summarized in Table 2. The waveforms captured at 400 µs/div for each test are shown in Figure 2. Each capture shows several cycles of the 1 kHz fundamental, displaying the three phase voltages OUTA, OUTB, and OUTC (20 V/div), the OUTA phase current (2 A/div), and the differential charge-pump voltage $V_{CP} – V_{BB}$ (2 V/div).

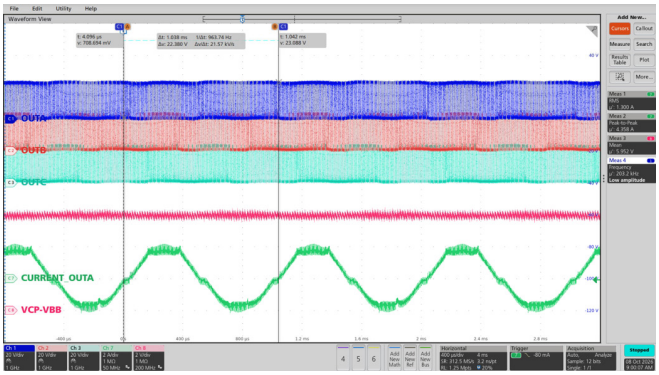
OBSERVATIONS

- ***Clean switching.*** All three phases switch cleanly at both frequencies and both temperatures. The OUTA current follows the 1 kHz sinusoidal reference. Each test produces a fault-free operation.
- ***The charge pump has margin.*** When a load is not present and PWM is not used, $V_{CP} – V_{BB}$ is 6.05 V. When switching occurs, $V_{CP} – V_{BB}$ reduces by 0.05 to 0.16 V. The worst case observed is 5.89 V at 200 kHz and 85°C, which is within the range (5.4 to 6.6 V) presented in the datasheet for $V_{BB} > 7$ V.
- ***Temperature has little effect.*** At either frequency, when temperature increases from 25°C to 85°C, $V_{CP} – V_{BB}$ shows minimal reduction (approximately 60 to 80 mV).
- ***Higher frequency reduces ripple.*** The high-frequency ripple on the phase current is visibly smaller at 200 kHz than at 100 kHz.

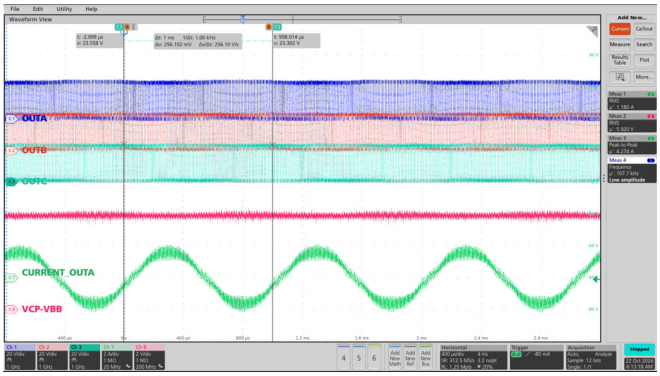
Test 1.1, 100 kHz, ≈25°C: OUTA/B/C, OUTA current, $V_{CP} – V_{BB}$



Test 1.2, 200 kHz, ≈25°C: OUTA/B/C, OUTA current, $V_{CP} – V_{BB}$



Test 2.1, 100 kHz, 85°C: OUTA/B/C, OUTA current, $V_{CP} – V_{BB}$



Test 2.2, 200 kHz, 85°C: OUTA/B/C, OUTA current, $V_{CP} – V_{BB}$

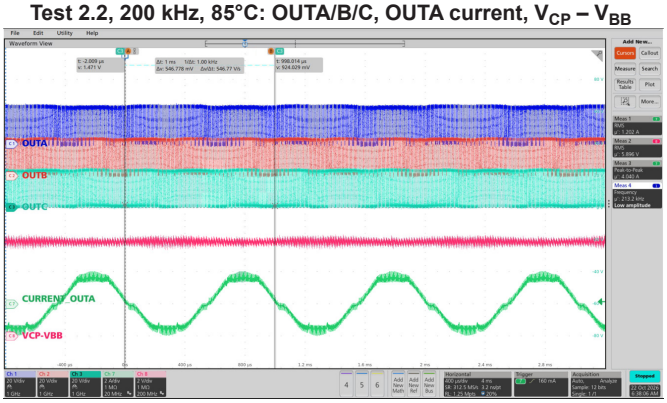


Figure 2: Test Results

Table 2: Summary of Measured Results (V_{BB} = 24 V, TSR/TSF = 0, RL = 3.3 Ω + 20 µH)

Test	f_{PWM}	Ambient	M_A	I_{RMS}	$V_{CP} – V_{BB}$
1.1	100 kHz	25°C	0.65	1.19 A	6 V
1.2	200 kHz	25°C	0.65	1.30 A	5.95 V
2.1	100 kHz	85°C	0.65	1.18 A	5.92 V
2.2	200 kHz	85°C	0.62	1.20 A	5.89 V

ESTIMATED SWITCHING-LOSS COMPARISON

The datasheet [1] provides a typical PWM frequency of 24 kHz. However, the datasheet does not provide a maximum. In practice, because switching and dead-time losses rise in proportion to f_{PWM}, the maximum f_{PWM} is determined by device dissipation.

This section estimates the losses of the A89110 at the measured operating conditions in two ways: 1) operations are compared at varied PWM frequencies (20, 50, 100 and 200 kHz) with a fixed phase current RMS (I_{RMS}) of 1.2 A, which is representative of the tests; and 2) same model is applied to the four measured tests using their actual RMS currents.

Loss Model

The model assumes three phases with sinusoidal current, where average current, I_{AVG}, is 0.9 × I_{RMS}.

Equation 1—Conduction power loss:

$$P_{COND} = 3 \times I_{RMS}^2 \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the drain-to-source on-state resistance.

Equation 2—Switching power loss:

$$P_{SW} = 3 \times 1/2 \times V_{BB} \times I_{AVG} \times (t_r + t_f) \times f_{PWM}$$

Equation 3—Dead-time (body-diode) conduction power loss:

$$P_{DT} = 3 \times V_F \times I_{AVG} \times t_{DT(total)} \times f_{PWM}$$

where V_F is the body-diode forward voltage, and $t_{DT(total)}$ is the total dead time (i.e., the rising dead time plus the falling dead time: $t_{DEAD(r)} + t_{DEAD(f)}$).

Equation 4—Junction temperature:

$$T_J = T_A + P_{TOT} \times R_{\theta JA}$$

where P_{TOT} is total bridge/MOSFET power dissipation, and $R_{\theta JA}$ is the package thermal resistance.

Table 3: Model Inputs

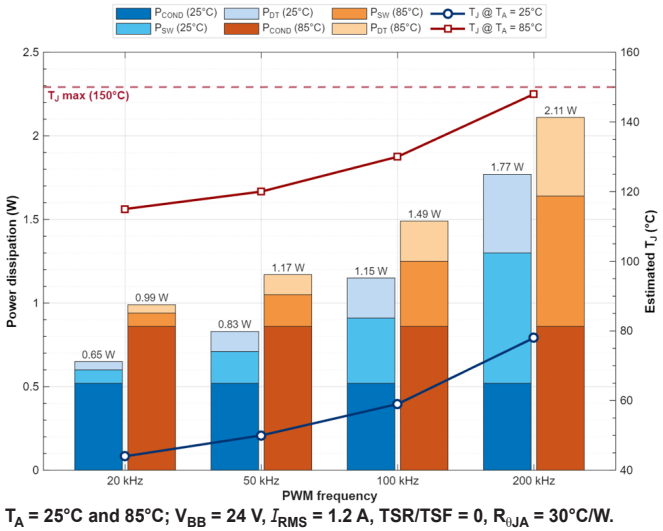
Parameter	Value
V_{BB}	24 V
$R_{DS(ON)}$ per switch	120 mΩ (25°C); 200 mΩ (150°C, hot case)
$t_r = t_f$	TSR/TSF = 0
Dead time $t_{DT(total)}$	500 + 410 = 910 ns per period
V_F (body diode)	0.8 V (assumed)
$R_{\theta JA}$	30°C/W (JEDEC 4-layer PCB); the evaluation board is not thermally characterized

Table 4: Estimated Losses vs. f_{PWM} (V_{BB} = 24 V, I_{RMS} = 1.2 A)

	20 kHz	50 kHz	100 kHz	200 kHz
P_{SW} (W)	0.08	0.19	0.39	0.78
P_{DT} (W)	0.05	0.12	0.24	0.47
P_{COND}, 25°C (W)	0.52	0.52	0.52	0.52
P_{TOT}, 25°C (W)	0.65	0.83	1.15	1.77
T_J at T_A = 25°C	44°C	50°C	59°C	78°C
P_{COND}, 85°C (W)	0.86	0.86	0.86	0.86
P_{TOT}, 85°C (W)	0.99	1.17	1.49	2.11
T_J at T_A = 85°C	115°C	120°C	130°C	148°C

Table 5: Estimated Losses at Measured Operating Points (V_{BB} = 24 V, TSR/TSF = 0)

Test	f_{PWM}/T_A	I_{RMS}	P_{TOT}	T_J (est.)
1.1	100 kHz/25°C	1.19 A	1.13 W	59°C
1.2	200 kHz/25°C	1.30 A	1.96 W	84°C
2.1	100 kHz/85°C	1.18 A	1.45 W	128°C
2.2	200 kHz/85°C	1.20 A	2.11 W	148°C



T_A = 25°C and 85°C; V_{BB} = 24 V, I_{RMS} = 1.2 A, TSR/TSF = 0, $R_{\theta JA}$ = 30°C/W.
NOTE: The 85°C conduction loss uses the worst-case $R_{DS(ON)}$ at T_J = 150°C.

Figure 3: Estimated A89110 Power Dissipation (P_{COND}, P_{SW}, P_{DT}) and T_J vs. f_{PWM}.

DISCUSSION

This section presents first-order estimates. Important notes about these estimates are provided following the descriptions.

Conduction loss does not depend on frequency.

When the PWM frequency is 20 to 50 kHz:

- Conduction losses dominate; and
- For operation at room temperature (~25°C), conduction losses represent approximately 60% to 80% of the total power loss (P_{TOT}).

Switching and dead-time losses scale linearly with f_{PWM}.

When the PWM frequency is 200 kHz:

- Switching losses and dead-time losses contribute approximately 70% of the total losses; and
- For operation at room temperature (~25°C), P_{TOT} is approximately 2.8× greater than it is for 20 kHz.

Thermal margin is the practical limit.

The following confirms continuous, fault-free operation in Test 2.2, albeit with limited thermal margin to 150°C:

- At 85°C ambient and 200 kHz (Test 2.2), the estimated junction temperature (T_J) is approximately 148°C, which approaches the 150°C maximum operating limit. This state correlates with the fault-free operation observed in Test 2.2. However, the remaining thermal margin is very narrow:
  - At this junction temperature, the informational temperature warning flag (TW, 135°C typical) of the device asserts as expected; and
  - Because stop-on-fault for temperature warning is disabled by default (FTW = 0) and T_J remains at a level well below the overtemperature shutdown threshold (OT, 175°C typical)—the bridge continues to operate without interruption.
- Operation at 105°C ambient at the tested current level requires a PWM frequency of 100 kHz or slower, a reduced phase current, or an improved PCB thermal design.

Dead time uses a proportionally bigger share of the period at high frequency.

At 200 kHz, the 910 ns total dead time is approximately 18% of the 5 µs period. This distorts the output voltage, so use of dead-time compensation or modulation-index margin is recommended.

IMPORTANT—Notes about these estimates:

- The edge times use the typical 20% to 80% slew values presented in the datasheet, which are specified at V_{BB} = 12 V:
  - Full transitions at 24 V take longer, so P_{SW} might be underestimated.
- The hot-case conduction loss uses $R_{DS(ON)}$ at T_J = 150°C, so it is conservative:
  - The actual dissipation depends on the PCB thermal performance, real edge times, body-diode characteristics, and load.
  - A designer should check the junction temperature in the specific intended system.

RECOMMENDATIONS AND DESIGN CONSIDERATIONS

The considerations that follow are highly recommended.

Layout

In a system that implements fast edges at high frequency, layout is critical.

- For the power and load connections, use short, wide copper tracks.
- Ensure that the LSSx and OUTx tracks are as short as practicable.
- Tie the three LSS pins together with short tracks.
- Place a 100 nF ceramic capacitor at each VBB pin, as close as practicable to the IC.
- To help limit fast transient spikes, place a 100 pF ceramic capacitor from each phase output to ground.
- Ensure that the PWM wiring from the controller remains short.

Thermal Design

- Connect the exposed pad to GND and use thermal vias.
- Use the loss estimates in Table 4, Table 5, and Figure 3 to choose the f_{PWM} specific to the expected ambient temperature and phase current.
- At 105°C ambient, either limit f_{PWM} to approximately 100 kHz at approximately 1.2 A RMS or reduce the current.

V_{DS} Fault at Higher Current

Each internal MOSFET has a V_{DS} overvoltage monitor that is active only while that MOSFET is commanded to the on state. In bench testing at V_{BB} = 12 V, the device operates at 1.5 A RMS without faults. At V_{BB} = 24 V with the fastest slew setting (TSR/TSF = 0), an increase in the phase current toward 1.5 A RMS triggers the V_{DS} fault. Like the V_{GS} undervoltage fault, the V_{DS} overvoltage fault does not have a stop-on-fault setting. When the DSO diagnostic is enabled (the default setting in the Mask 0 register), a trip sets the DSO bit in the Status 1 register and disables all six MOSFETs, and the outputs enter the high-impedance state. The MOSFETs remain in the latched-off state until the value "1" is written to DSO in the Status 1 register or until the RESETn is pulsed low. DSO can be disabled via the Mask 0 register, but this is not recommended because it removes short-circuit protection for the internal MOSFETs; rather, the following actions are recommended:

- Check that the V_{DS} fault does not trip anywhere across the full range of phase current, supply voltage and temperature.
- Maintain low inductance on the LSSx and OUTx track, and consider a 100 pF ceramic capacitor from each phase output to ground to limit fast transient spikes.
- At higher supply voltages, try a slower slew setting (TSR/TSF = 1 to 3).

  NOTE: A change to the slew setting also changes the integrated dead time.
- Configure the firmware to monitor DSO (through DIAG or the Status 1 register) and to handle recovery.

Supply Voltage

All high-frequency tests in this note are performed at V_{BB} = 24 V. For the specific test conditions presented in this application note, the results show that $V_{CP} - V_{BB}$ remains at 5.89 to 6 V, which is within the 5.4 to 6.6 V regulation range specified for $V_{BB} > 7$ V. In contrast, for V_{BB} between 4.5 V and 7 V, the datasheet [1] guarantees only $V_{CP} - V_{BB} \geq 3.7$ V at charge-pump loads up to 1 mA.

However, gate charge drawn from the charge pump increases in proportion to the PWM frequency, so charge-pump voltage margin at low supply voltage decreases as frequency increases.

For 100 to 200 kHz operation, the minimum operating V_{BB} is required to remain at greater than 7 V, including supply dips and transients. Therefore, when the specific system implementation is at the lowest supply voltage, V_{CP} monitoring is recommended. The typical 12 V and 24 V robotic supplies, which have a minimum of approximately 8 V on a 12 V bus, remain within this range.

Temperature Coverage

The highest-temperature tests reported here are at 85°C ambient. Operation up to 105°C at high-PWM frequency is not verified.

CONCLUSION

The A89110 drives a three-phase sinusoidal PWM load at 100 kHz and 200 kHz from a 24 V supply, at both 25°C and 85°C ambient, as described in this application note. This performance is approximately 8× the typical f_{PWM} specified in the datasheet. All four tests reported here run without faults, at phase currents of 1.18 to 1.30 A RMS. The charge pump maintains the difference between V_{CP} and V_{BB} at 5.89 to 6 V, which is well within the range of 5.4 to 6.6 V specified in the datasheet. [1] Compared to 100 kHz, operation at 200 kHz results in approximately half the phase current ripple. For low-inductance motors, the reduced phase current ripple is an important feature that makes the A89110 a good fit for compact actuator drives in robotics, such as in dexterous hands and small servo joints.

The estimated loss comparison (Table 4, Table 5, and Figure 3) shows that the practical upper limit to the PWM frequency is dictated by thermal limits, not the gate drive. Switching and dead-time losses rise linearly with frequency. At 200 kHz and 85°C ambient, the estimated junction temperature is slightly less than the 150°C operating limit.

IMPORTANT: The results in this note were obtained on the A89110 evaluation board under the specific laboratory conditions described. Performance in an end application depends on PCB layout, thermal design, motor parameters, supply voltage, load current, slew and dead-time settings, and ambient temperature. Customers must evaluate and validate the A89110 in their own system across all intended operating conditions before using it in production.

Revision History

Number	Date	Description	Responsibility
–	November 10, 2026	Initial release	M. Kumar

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