Ultra-Sensitive Hall-Effect Speed and Direction Sensor with TPOS

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: September 30, 2024

Deadline for receipt of LAST TIME BUY orders: January 31, 2025

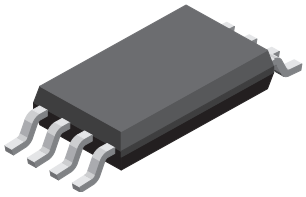
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Ultra-Sensitive Hall-Effect Speed and Direction Sensor with TPOS

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- Senses speed and direction of ring magnets
  - □ Two matched bipolar Hall-effect switches on a single substrate
  - □ True Power-On State (TPOS): Recognizes hysteresis region at power-on
- Superior temperature stability
- Internal regulator for 3.3 to 24 V operation
- Symmetrical, high-sensitivity switch points
- Automotive grade
  - □ Solid-state reliability
  - □ Integrated ESD diodes
  - □ Robust structures for EMC protection
  - □ Short-circuit protected outputs
  - □ Reverse battery protection
  - □ –40°C to +150°C operating range

Package: 8-pin TSSOP (suffix LE)



Not to scale

DESCRIPTION

The A1232 is a highly sensitive, temperature-stable magnetic sensing device ideal for use in ring-magnet-based speed and direction systems in harsh automotive and industrial environments. It contains two bipolar, Hall-effect switches precisely arranged 1.63 mm apart. The switch outputs are thus in quadrature when interfaced with the proper ring magnet design. Internal logic processes the resulting digital signals to derive speed and direction information that is presented at the device's outputs, OUTPUT A and OUTPUT B.

The A1232 is designed for demanding, high-performance motor commutation applications. The Hall elements are photolithographically aligned to better than 1 µm. Accurately locating the two Hall elements eliminates a major manufacturing hurdle encountered in fine-pitch applications. The A1232 also has true power-on state (TPOS), the ability to detect when it is in the hysteresis band, beyond B_{OP}, or below B_{RP} at power-on. This provides reduced angle accuracy error due to missed start-up edges.

Post-assembly factory programming at Allegro provides sensitive, symmetrical switch points for both switches. Extremely low-drift amplifiers maintain this symmetry. The Allegro high-frequency chopper stabilization technique cancels offsets in each channel and allows for increased signal-to-noise ratio at the input of the internal comparators. This leads to stable operation across the operating temperature and voltage ranges and industry leading jitter performance.

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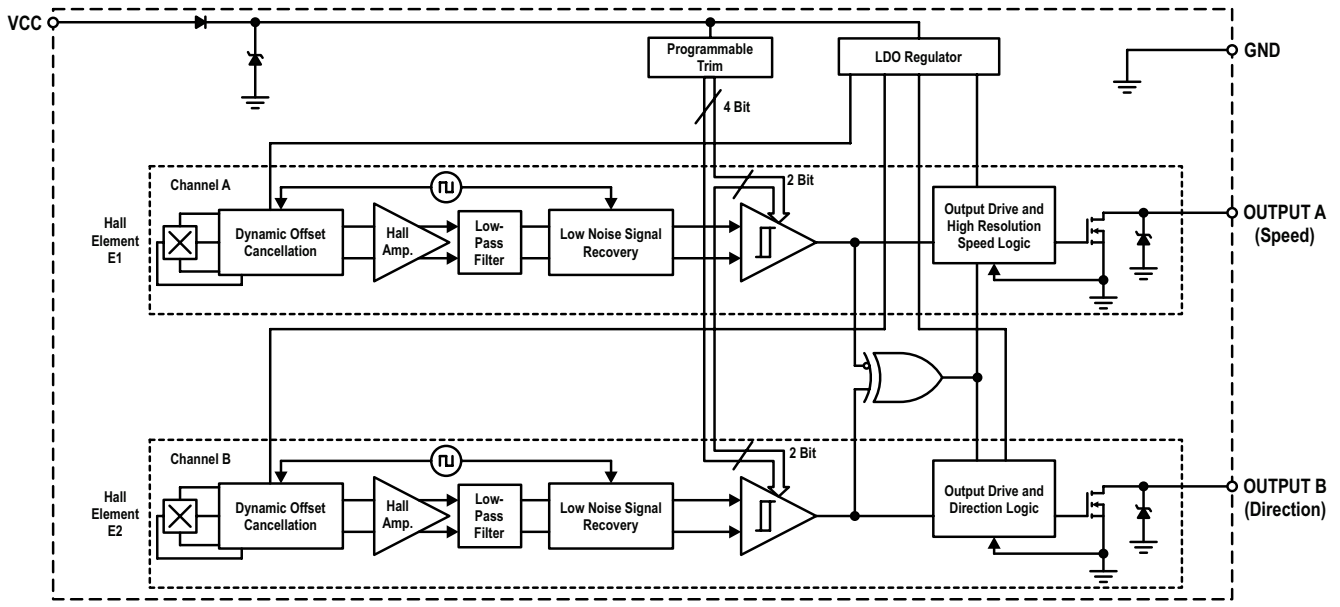

Functional Block Diagram

DESCRIPTION (continued)

An on-chip regulator provides a wide operating voltage range. The A1232 is packaged in a plastic 8-pin surface mount TSSOP (LE). This gull-wing style package is optimized for the extended temperature range of –40°C to 150°C. It is lead (Pb) free and RoHS-compliant, with a 100% matte-tin-plated leadframe.

SELECTION GUIDE

Part Number	Packing*	Mounting	Ambient (T_A)
A1232LLETR-T	4000 units per reel	8-Pin TSSOP Surface Mount	–40°C to 150°C

*Contact Allegro™ for additional packing options.

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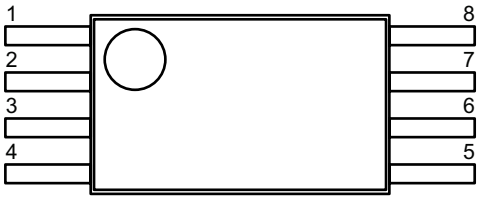
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Off Voltage	$V_{OUT(OFF)}$		V_{CC}	V
Output Sink Current	I_{OUT}		Internally Limited	–
Magnetic Flux Density	B		Unlimited	–
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pinout Diagram and Terminal List Table



Package LE, 8-Pin TSSOP Pinout Diagram

Terminal List Table

Name	Number	Function
3	VCC	Connects power supply to chip
4	OUTPUT B	Start-up Mode: Output from E2 via first Schmitt circuit Running Mode: Direction
5	OUTPUT A	Start-up Mode: Output from E1 via second Schmitt circuit Running Mode: High-Resolution Speed
6	GND	Terminal for ground connection
1, 2, 7, 8	NC	No connections

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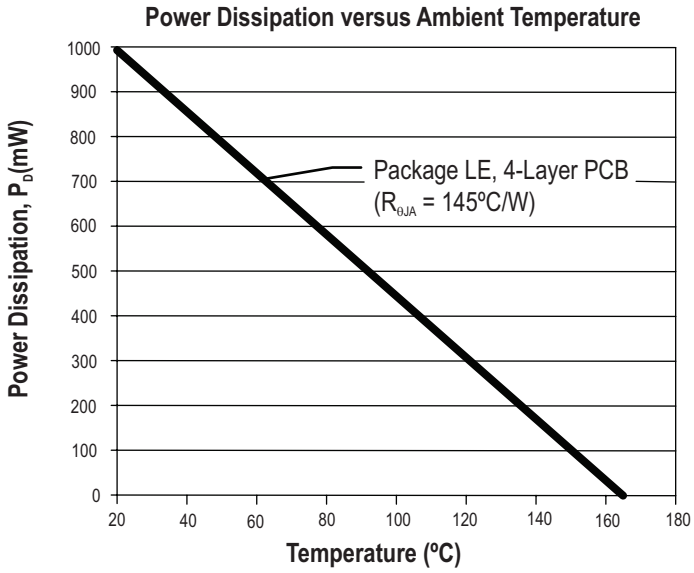
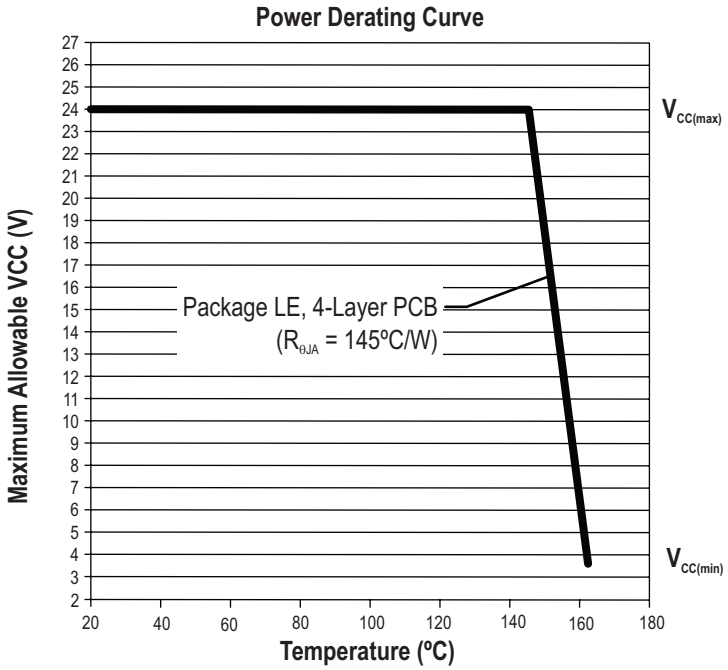
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Power Derating section.

Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard JESD51-7	145	°C/W





[1] Additional thermal information is available on the Allegro website, www.AllegroMicro.com

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ELECTRICAL CHARACTERISTICS: Valid over full operating temperature range unless otherwise noted; typical data applies to V_{CC} = 12 V and T_A = 25°C; see typical application circuits

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS [2]							
Supply Voltage [3]	V_{CC}	Operating: $T_A \le 150°C$		3.3	–	24	V
Output Leakage Current	I_{OFF}	Either output		–	<1	10	µA
Supply Current	I_{CC}			2.5	3.7	6.0	mA
Low Output Voltage	$V_{OUT(ON)}$	I_{OUT} = 20 mA $B > B_{OP(A)}$, $B > B_{OP(B)}$		–	185	500	mV
Middle Output Voltage [4]	$V_{OUT(MID)}$	$B_{RP} < B < B_{OP}$, $V_{PULL-UP}$ = 12 V, R_{LOAD} = 12 kΩ		–	6	–	V
Output Sink Current, Middle	$I_{OUT(MID)}$	$B_{RP} < B < B_{OP}$, $V_{PULL-UP}$ = 12 V, R_{LOAD} = 12 kΩ		–	0.5	–	mA
Output Sink Current Limit	I_{OM}	V_{CC} = 12 V		30	–	70	mA
Chopping Frequency	f_C			–	750	–	kHz
Output Rise Time [5]	t_r	C_S = 20 pF, R_{LOAD} = 820 Ω		–	1.8	–	µs
Output Fall Time [5]	t_r	C_S = 20 pF, R_{LOAD} = 820 Ω		–	1.2	–	µs
Power-On Time [6]	t_{ON}			–	50	65	µs
Power-On State [7]	POS	$t < t_{ON}$	B = 0 G	$V_{OUT(OFF)}$			–
		$t \ge t_{ON}$	$B_{RP} < B < B_{OP}$	$V_{OUT(MID)}$			–
			$B > B_{OP}$	$V_{OUT(ON)}$			–
			$B < B_{RP}$	$V_{OUT(OFF)}$			–
TRANSIENT PROTECTION CHARACTERISTICS							
Supply Zener Clamp Voltages	V_Z	I_{CC} = 9 mA, T_A = 25°C		28	46	–	V
Supply Zener Current [8]	I_Z	V_S = 28 V		–	–	9.0	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V, $T_J < T_{J(max)}$		–	2	15	mA

[2] Output related specifications listed in the characteristic column are applicable to each output transistor unless otherwise noted.
[3] Maximum voltage operation must not exceed maximum junction temperature. Refer to power de-rating curves.
[4] $V_{OUT(MID)}$ and $I_{OUT(MID)}$ specified typical values are found when connected as shown in Figure 10 and Figure 11. This information is only guaranteed available before the first magnetic field transition has occurred and after the power-on time has occurred. The output state transition from the $t < t_{ON}$ POS and the $t > t_{ON}$ POS is not considered the first magnetic field transition. See Figure 1 and the Magnetic Truth Table for power-on behavior.
[5] C_S = oscilloscope probe capacitance
[6] Power-On Time is the duration from when V_{CC} rises above $V_{CC(MIN)}$ until both outputs have attained valid states.
[7] POS for both outputs is undefined for $V_{CC} < V_{CC(MIN)}$. Use of a V_{CC} slew rate greater than 25 mV/µs is recommended.
[8] Maximum specification limit is equivalent to $I_{CC(MAX)}$ + 3 mA.

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MAGNETIC CHARACTERISTICS: Valid over full operating temperature range unless otherwise noted; typical data applies to V_{CC} = 12 V and T_A = 25°C; see typical application circuits

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units [9]
MAGNETIC CHARACTERISTICS [10]						
Operate Point: B > B_{OP}	$B_{OP(A)}$, $B_{OP(B)}$		–	10	30	G
Release Point: B < B_{RP}	$B_{RP(A)}$, $B_{RP(B)}$		–30	–10	–	G
Hysteresis: $B_{OP(A)}$ - $B_{RP(A)}$, $B_{OP(B)}$ - $B_{RP(B)}$	$B_{HYS(A)}$, $B_{HYS(B)}$		5	20	35	G
Symmetry: Ch A, Ch B $B_{OP(A)}$ + $B_{RP(A)}$, $B_{OP(B)}$ + $B_{RP(B)}$	SYM_A, SYM_B		–35	–	35	G
Operate Symmetry: $B_{OP(A)}$ – $B_{OP(B)}$	$SYM_{AB(OP)}$		–25	–	25	G
Release Symmetry: $B_{RP(A)}$ – $B_{RP(B)}$	$SYM_{AB(RP)}$		–25	–	25	G

[9] 1G (gauss) = 0.1 mT (millitesla)

[10] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. The algebraic convention used here supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).

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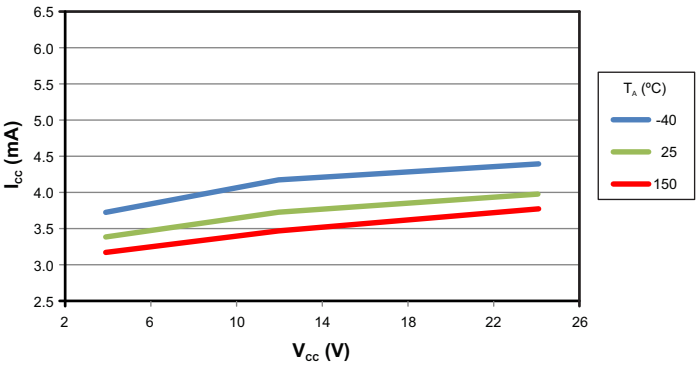
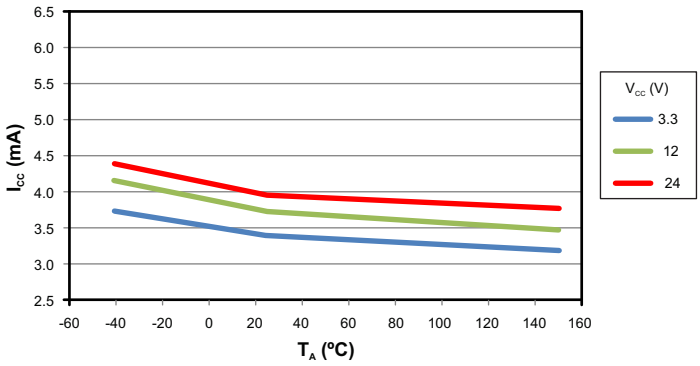
ELECTRICAL OPERATING CHARACTERISTICS

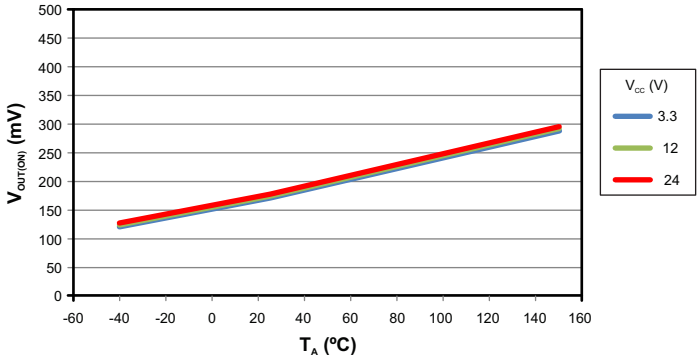
Average Supply Current versus Supply Voltage



Average Supply Current versus Ambient Temperature



Average Low Output Voltage versus Ambient Temperature for I_{OUT} = 20 mA



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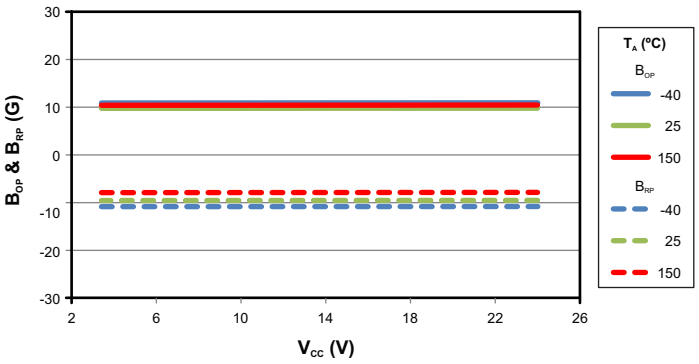
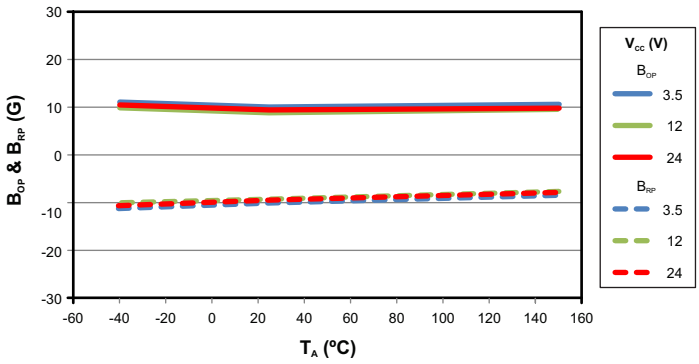
MAGNETIC CHARACTERISTICS

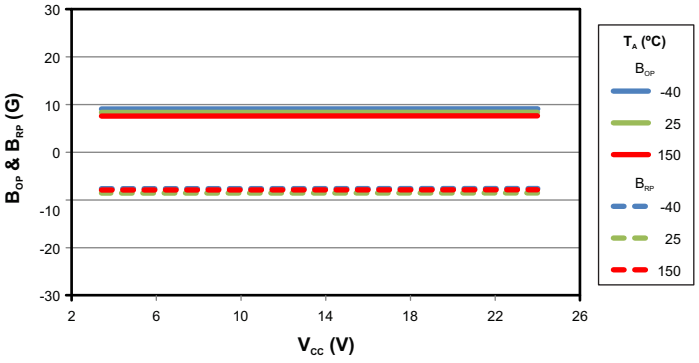
Channel A: Average Operate & Release Points versus Supply Voltage



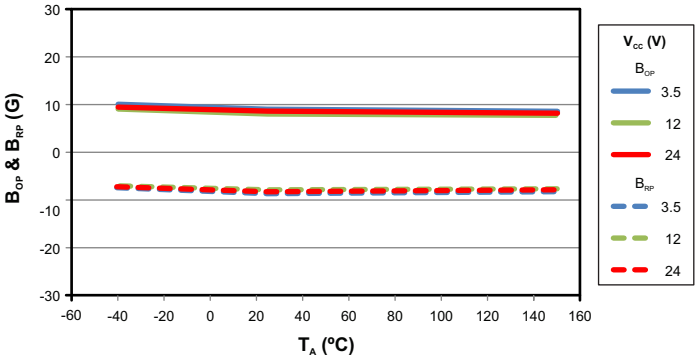
Channel A: Average Operate & Release Points versus Ambient Temperature



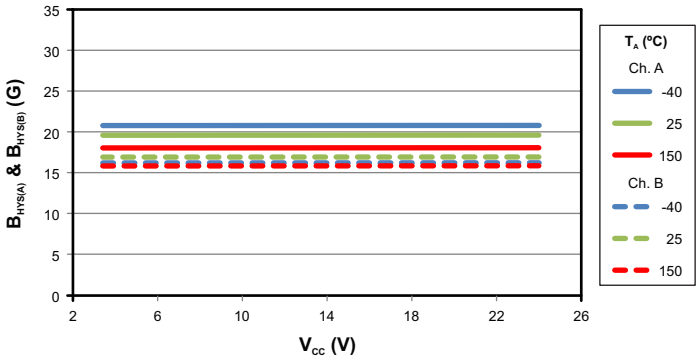
Channel B: Average Operate & Release Points versus Supply Voltage



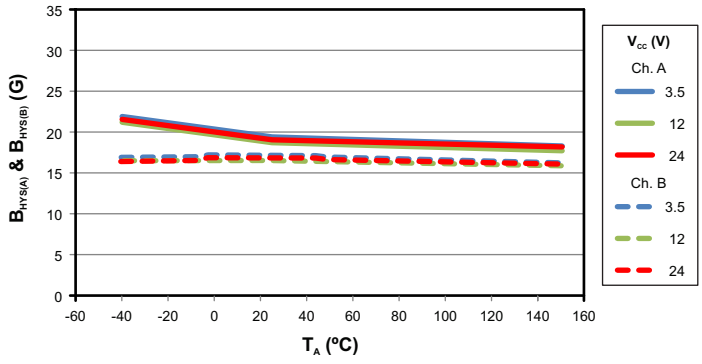
Channel B: Average Operate & Release Points versus Ambient Temperature



Channel A & B: Average Switchpoint Hysteresis versus Supply Voltage



Channel A & B: Average Switchpoint Hysteresis versus Ambient Temperature



Additional Magnetic Characteristics on next page.

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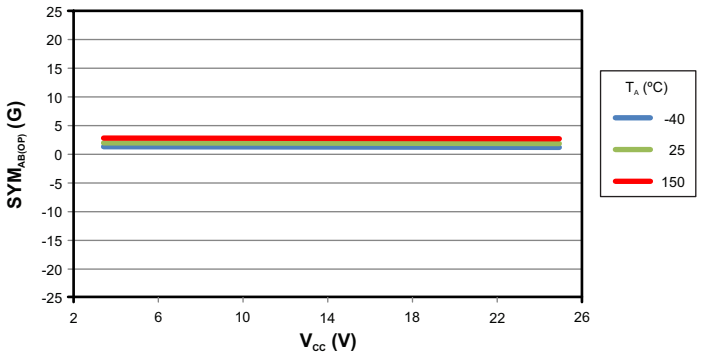
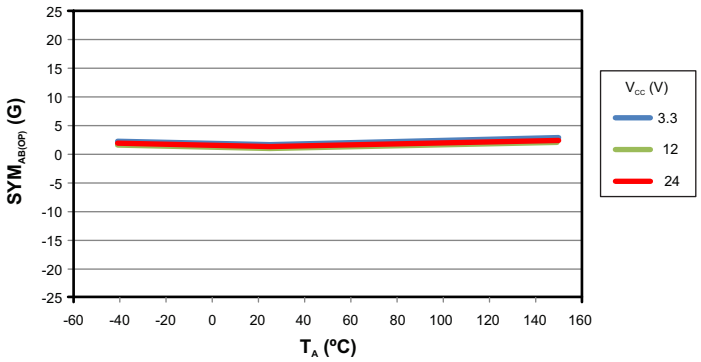
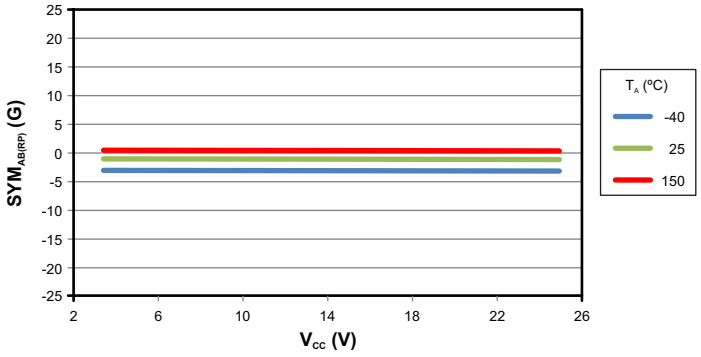
Average Operate Point Symmetry versus Supply Voltage



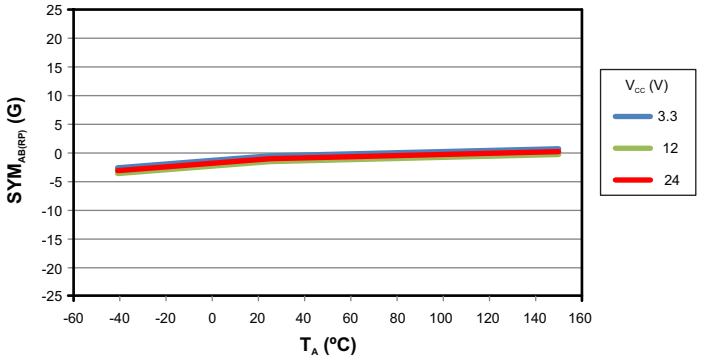
Average Operate Point Symmetry versus Ambient Temperature



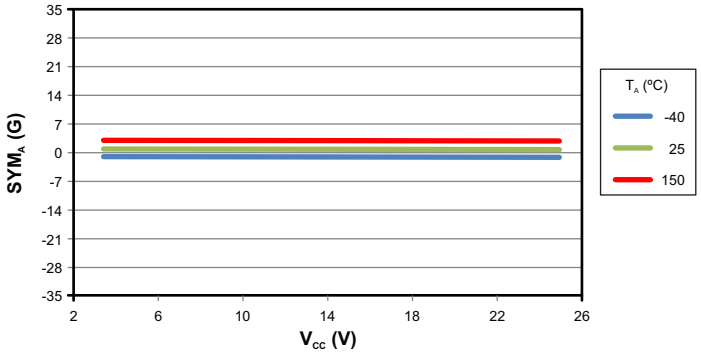
Average Release Point Symmetry versus Supply Voltage



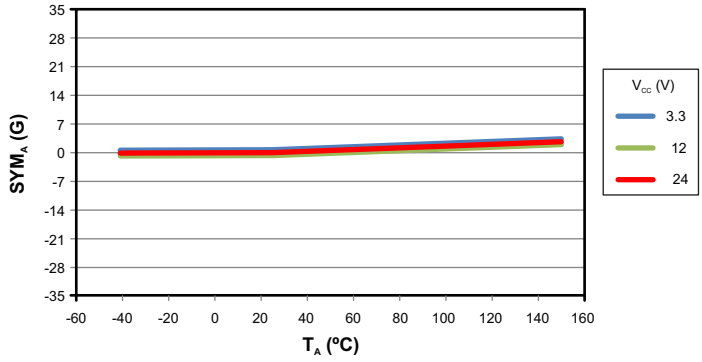
Average Release Point Symmetry versus Ambient Temperature



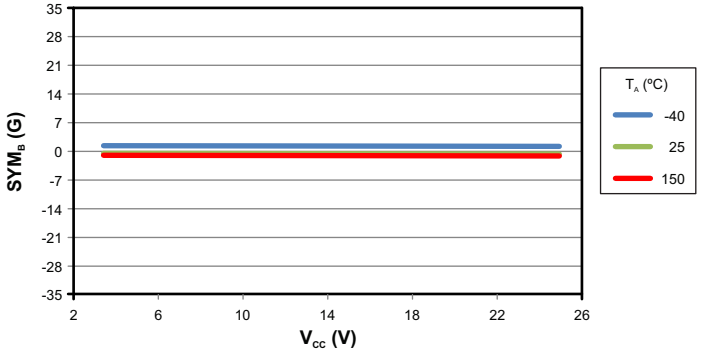
Channel A Symmetry versus Supply Voltage



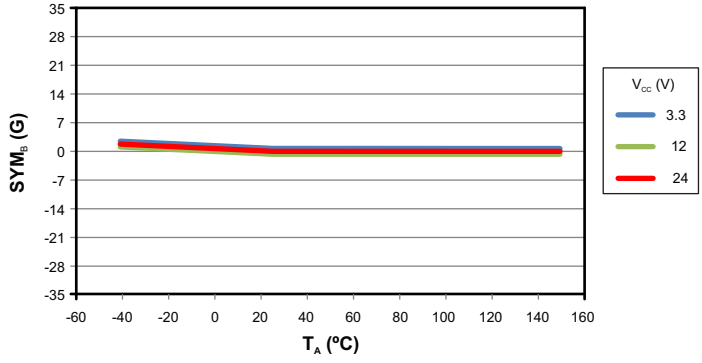
Channel A Symmetry versus Ambient Temperature



Channel B Symmetry versus Supply Voltage



Channel B Symmetry versus Ambient Temperature



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MAGNETIC TRUTH TABLE

Conditions	Magnetic Field B_{E1} at Hall Element E1	Magnetic Field B_{E2} at hall Element E2	OUTA	OUTB
$t < t_{ON}$	–	–	X	X
$t > t_{ON}$ Power-On Time has occurred and fields B_{E1} and B_{E2} have not yet each transitioned	$B_{E1} < B_{RP(A)}$	$B_{E2} < B_{RP(B)}$	H	H
	$B_{E1} < B_{RP(A)}$	$B_{RP(B)} < B_{E2} < B_{OP(B)}$	H	M
	$B_{E1} < B_{RP(A)}$	$B_{E2} > B_{OP(B)}$	H	L
	$B_{RP(A)} < B_{E1} < B_{OP(A)}$	$B_{E2} < B_{RP(B)}$	M	H
	$B_{RP(A)} < B_{E1} < B_{OP(A)}$	$B_{RP(B)} < B_{E2} < B_{OP(B)}$	M	M
	$B_{RP(A)} < B_{E1} < B_{OP(A)}$	$B_{E2} > B_{OP(B)}$	M	L
	$B_{E1} > B_{OP(A)}$	$B_{E2} < B_{RP(B)}$	L	H
	$B_{E1} > B_{OP(A)}$	$B_{RP(B)} < B_{E2} < B_{OP(B)}$	L	M
	$B_{E1} > B_{OP(A)}$	$B_{E2} > B_{OP(B)}$	L	L
$t > t_{ON}$ & B_{E1} and B_{E2} have already each transitioned at least one time	Any	Any	SPD	DIR

Key

L = $V_{OUT(ON)}$, Low
M = $V_{OUT(MID)}$, Middle
H = $V_{OUT(OFF)}$, High
SPD = High-Resolution Speed
DIR = Direction
X = Output Not Defined

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FUNCTIONAL DESCRIPTION

Typical Applications Operation

As shown in Figure 1, the bipolar Hall-effect switches in the A1232 turn on when a south-polarity magnetic field perpendicular to the Hall element exceeds the operate point threshold (B_{OP}); the switches turn off when a north-polarity magnetic field of sufficient strength exceeds the release point (B_{RP}) The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device.

$$B_{HYS} = B_{OP} - B_{RP}$$

This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

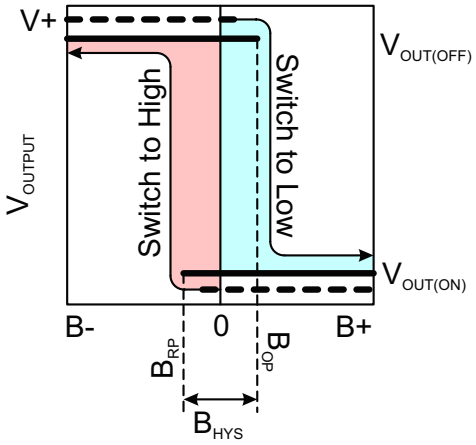

Figure 1: Output Voltage in Relation to Magnetic Flux Density Received

The Hall-effect sensing elements are precisely located 1.63 mm apart across the width of the package (see Figure 2: A1232 Sensors and Relationship to Target). When used with a properly designed ring magnet, the outputs of the two switches will be in quadrature, or 90 degrees out of phase. The relationship of the various signals and the typical system timing is shown in Figure 3: Typical System Timing.

During operation (Run Mode), the output of the internal switches is encoded into a pair of signals representing the speed and direction of the target (see Functional Block Diagram on page 1). These signals appear at the OUTPUT A (speed) and OUTPUT B (direction) pins.

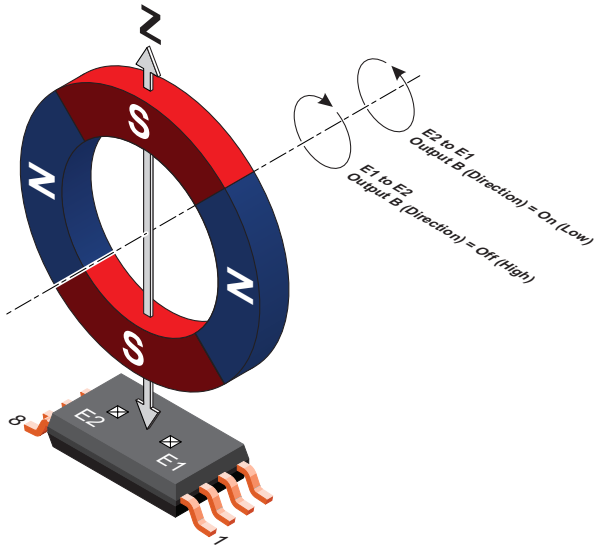

Figure 2: A1232 Sensor and Relationship to Target

OUTPUT B (direction) is a logic signal indicating the direction of rotation (assuming a ring magnet target). It is defined as off (high) for targets moving in the direction from E1 to E2 and on (low) for the direction E2 to E1. For instances when the rotation direction of the target changes, OUTPUT B changes state and then the speed output (OUTPUT A) resumes after a short delay (t_d, approximately 3 to 5 µs). OUTPUT B (direction) is always updated before OUTPUT A (speed) and is updated at each Hall element's switching transition. This sequencing and built-in delay allow the tracking of target speed or position with an external counter without the loss of pulses.

OUTPUT A (speed) is a logic output representing the combined (XOR'ed) outputs of the two Hall-effect switches. This produces a digital output edge at each switch's transition beyond B_{OP} and B_{RP}. It will change state as the magnetic poles pass across the device at a rate given by Equation A and with a period given by Equation B:

$$f_{OUTPUTA}\,(Hz) = \frac{V \times \omega}{60\ seconds} \times 2 \qquad (A)$$

$$T_{OUTPUTA}\,(s) = \frac{1}{f_{OUTPUTA}} \qquad (B)$$

Example for ω = 2 and V = 60 rpm (based on target depicted in Figure 3):

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$$f_{OUTPUTA}\,(Hz) = \frac{60 \times 2}{60\ seconds} \times 2 = 4\ Hz$$

$$T_{OUTPUTA}\,(s) = \frac{1}{4\ Hz} = 250\ ms$$

Key:

- V = Axle Shaft Speed (rpm)
- ω = Number of North and South Pole-Pairs per Axle Mechanical Revolution
- f = Cycles per Second (Hz)
- T = Time Duration of One Mechanical Period (s)

Immediately after turn-on, the device will be in a special True Power-On State (TPOS) mode. This mode allows the device to detect and indicate that one or both of the switches is in the hysteresis region, i.e., that the applied field is between B_{OP} and B_{RP}.

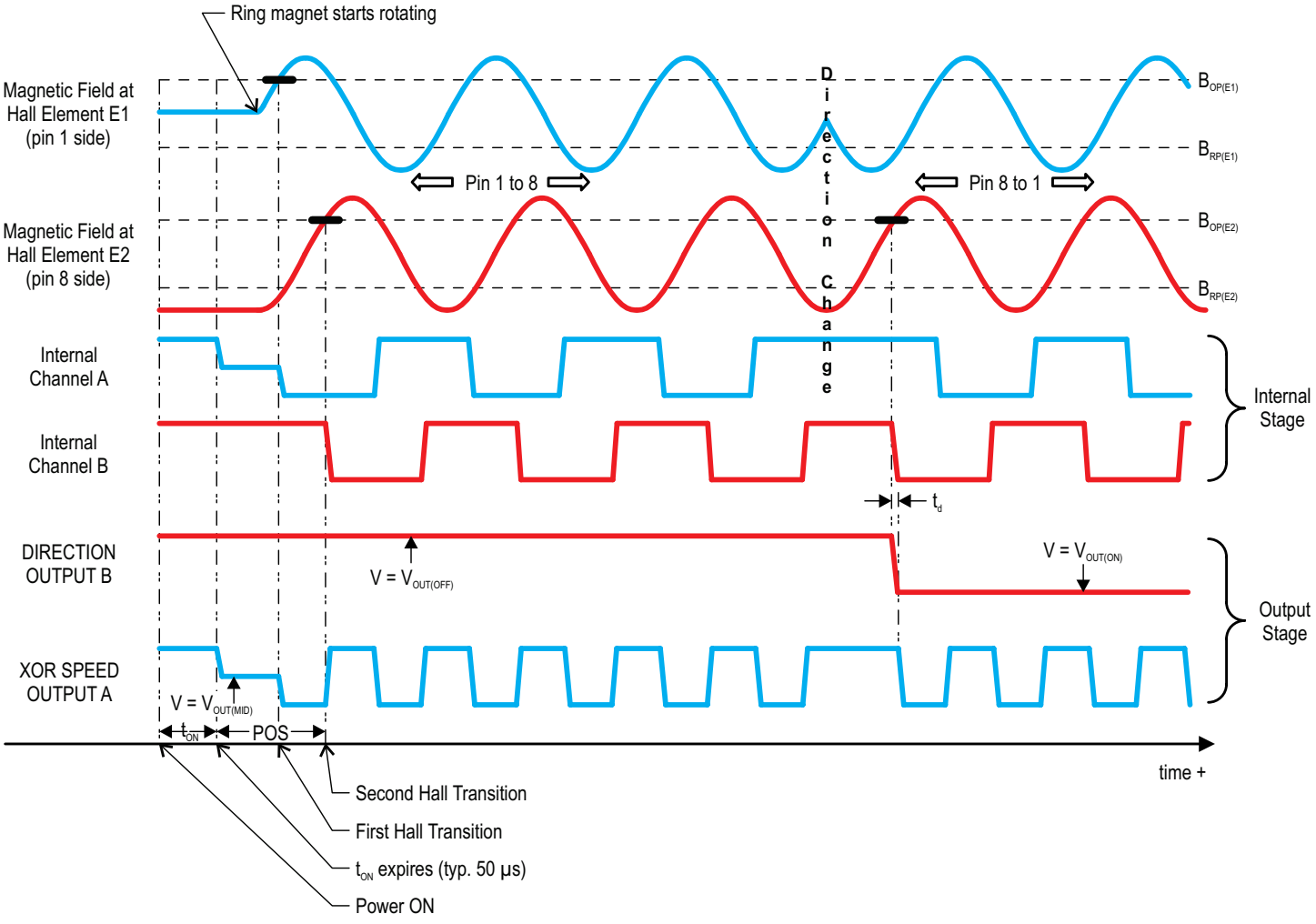

Figure 3: Typical System Timing

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Power-On Sequence and Timing

The states of OUTPUT A and OUTPUT B are only valid when the supply voltage is within the specified operating range ($V_{CC(min)} \le V_{CC} \le V_{CC(max)}$) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 4: Power-On Sequence and Timing for an illustration of the power-on sequence.

True Power-On State (TPOS)

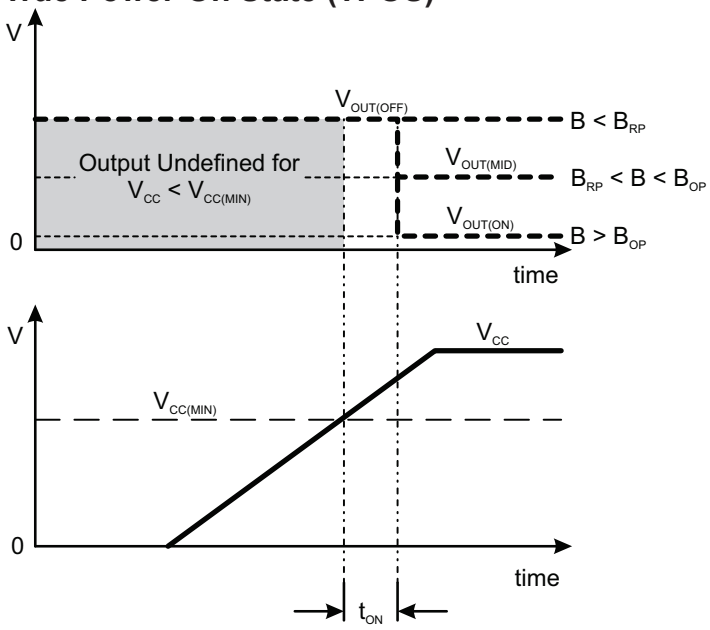

Figure 4: Power-on Sequence and Timing

Immediately after power-on (Figure 4, after t_{ON} has elapsed), OUTPUT A and OUTPUT B will follow the state of the corresponding switches rather than the outputs of the speed and direction logic. This mode allows the device to detect and indicate that one or both of the switches is in the hysteresis region (i.e., that the applied field is between B_{OP} and B_{RP}). Additionally, while in TPOS mode, the outputs will report if the corresponding switch is beyond B_{OP} or below B_{RP}. These output states, $V_{OUT(ON)}$ for $B > B_{OP}$ and $V_{OUT(OFF)}$ for $B < B_{RP}$, reflect the output polarity and level corresponding to the target feature (magnet pole) nearest the switch.

In Run Mode, the outputs will be driven only either high or low, that is, to $V_{OUT(OFF)}$ or $V_{OUT(ON)}$, as the A1232 indicates the movement of the target. (The precise voltage levels are dictated by the load circuit and pull-up voltage on each output.) While the A1232 is in TPOS mode and either or both of the sensors are in their hysteresis range ($B_{OP} < B < B_{RP}$), a third state is present on the corresponding output as shown in Figure 5: Power-On State vs. Applied Field. Dynamic current limiting circuitry holds the output sink current at $I_{OUT(MID)}$, creating an output state known as $V_{OUT(MID)}$.

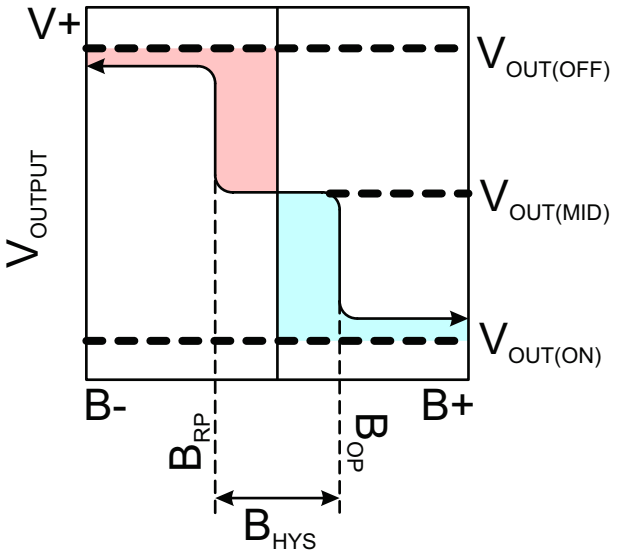

Figure 5: Power-On State vs. Applied Field

The output voltage corresponding to $V_{OUT(MID)}$ is given by:

$$V_{OUT(MID)} = V_{OUT(OFF)} - [I_{OUT(MID)} \times R_{LOAD}]$$

By choosing the correct load resistor, R_{LOAD}, this middle output state can be made equal to half of the pull-up voltage. This is the case when using the typical application circuits shown in Figures 10 and 11. See the Circuit Analysis Example table following the typical application circuits for more details. The host must be able to detect this middle state in order to make use of the TPOS information.

After exiting TPOS mode, only the standard low ($V_{OUT(ON)}$) and high ($V_{OUT(OFF)}$) output states are produced to indicate target speed and direction. Both outputs exit TPOS mode together, and only after each switch has detected a magnetic field transition from their power-on state (that is, beyond B_{OP} or B_{RP}). Internal comparators prevent the outputs from entering the $I_{OUT(MID)}$ state if it was not activated at the moment of power-on. Once having exited TPOS mode, the outputs will not re-enter TPOS mode as long as power is maintained.

NOTE:
The states of OUTPUT A and OUTPUT B are only valid when the supply voltage is within the specified operating range and the power-on time has elapsed. See Power-on Sequence and Timing for details.

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Target Design/Selection

Internal logic circuitry produces outputs representing the speed (OUTPUT A) and direction (OUTPUT B) of the magnetic field passing across the face of the package. The response of the device to the magnetic field produced by a rotating ring magnet is shown in Figure 3. (Note the phase shift between the two integrated Hall elements.)

For the direction signal to be correct, the switch points of the Hall elements must be adequately matched and a quadrature relationship must be maintained between the target's magnetic poles and the spacing of the two Hall elements (E1 and E2). A quadrature relationship produces Hall switch phase separation of 90°.

For optimal performance, the device should be actuated by a ring magnet that presents to the front of the device fields with a pole pitch two times the Hall element-to-element spacing of 1.63 mm. The period (T) is then equal to twice the pole pitch (P), as depicted by Figure 6 and Equation C. This will produce a sinusoidal magnetic field whose period corresponds to four times the element-to-element spacing:

$$For\ P = 2 \times 1.63\ mm = 3.26\ mm \qquad (C)$$

$$T = 2 \times 3.26\ mm = 6.52\ mm$$

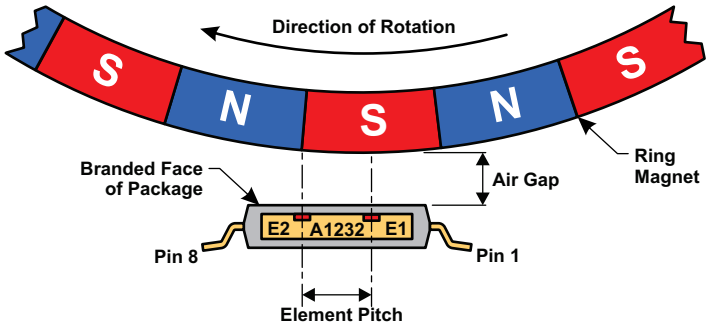

Figure 6a: Device Orientation to Target

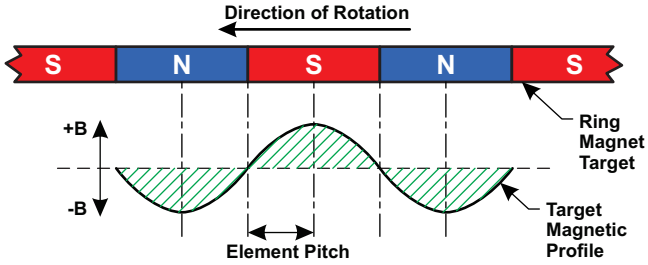

Figure 6b: Mechanical Position
(Target moves past device pin 1 to pin 8)

Figure 6: Target Profiling During Operation

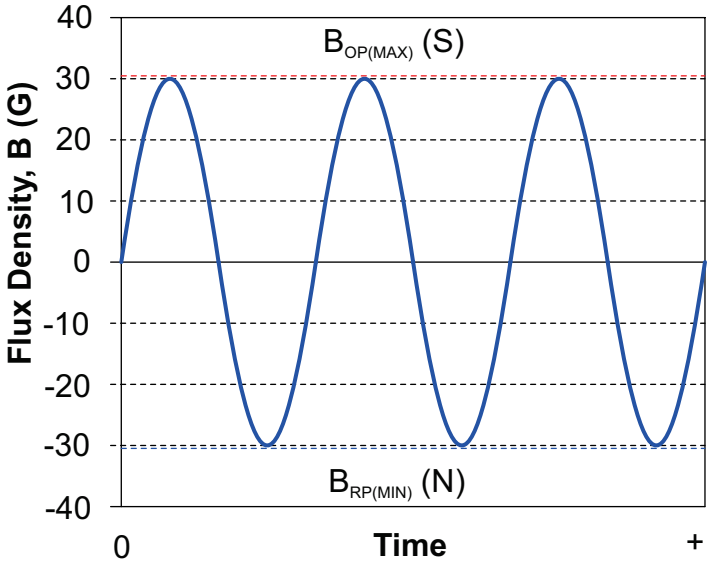

Figure 7a: Example of Ring Target Magnetic Profile

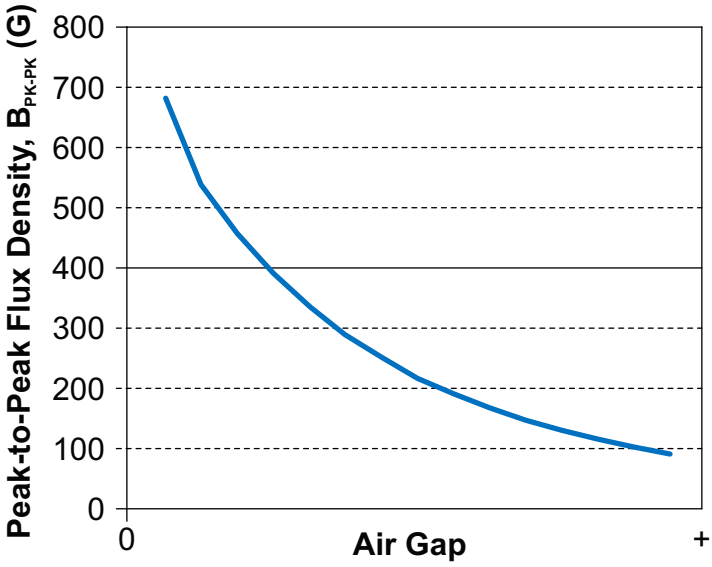

Figure 7b: Example of Ring Magnetic Flux Density Peak-to-Peak vs. Air Gap

Figure 7: Example of Target Magnetic Field Profile

The A1232 requires a minimum magnetic field input to guarantee switching, as described in Equation D:

$$B_{PK\text{-}PK} = B_{OP(MAX)} + |B_{RP(MIN)}|, \qquad (D)$$

$$B_{PK\text{-}PK} = 30\ G + 30\ G = 60\ G$$

Based on the maximum operate point ($B_{OP(MAX)}$) and the mini-

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mum release point ($B_{RP(MIN)}$), it is recommended to ensure the target's magnetic input signal remains above 60 G peak-to-peak when centered about 0 G. If the system has a magnetic offset component present, field values B_{OP} and B_{RP} must be exceeded to continue switching. Thus, for optimal performance it is recommended to interface the sensor with an alternating bipolar magnetic field profile that continuously exceeds $B_{OP(MAX)}$ and $B_{RP(MIN)}$.

As depicted in Figure 7, the sinusoidal profile created by the alternating north and south poles of a rotating ring magnet decreases in magnitude as the air gap is increased. The minimum peak-to-peak flux density must be accounted for in system air gap tolerances.

Operation with Fine-Pitch Ring Magnets

For targets with a circular pitch of less than 4 mm, a performance improvement can be observed by rotating the front face of the device (refer to Figure 8). This rotation decreases the effective Hall element-to-element spacing (D), provided that the Hall elements are not rotated beyond the width of the target.

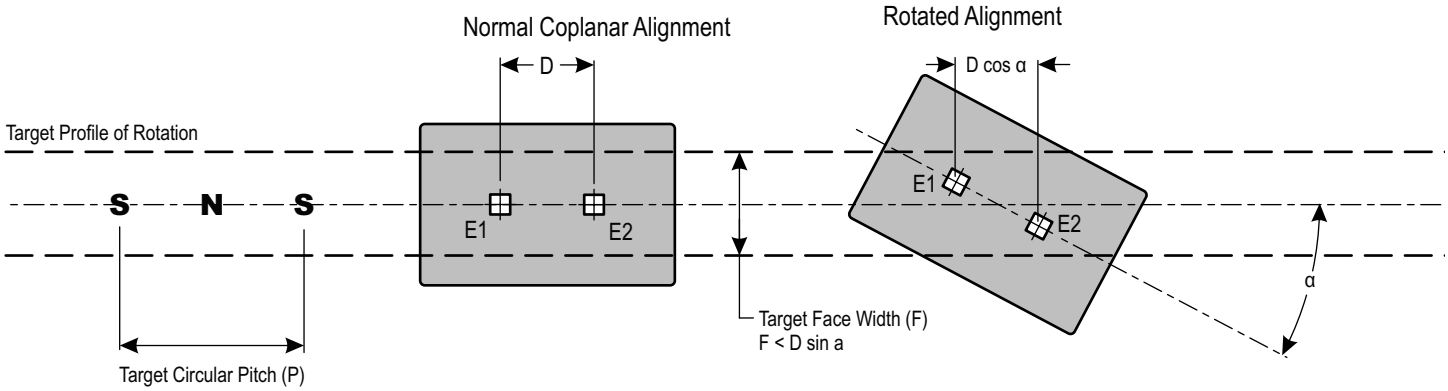

Figure 8: Operation with Fine-Pitch Ring Magnets

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Chopper Stabilization Technique

A limiting factor for switch point accuracy when using Hall-effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper Stabilization is a proven approach used to minimize Hall offset.

The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 9: Example of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the dc offset becomes a high frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed.

Allegro's innovative chopper-stabilization technique uses a high frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the A1232 that utilize this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample and hold circuits.

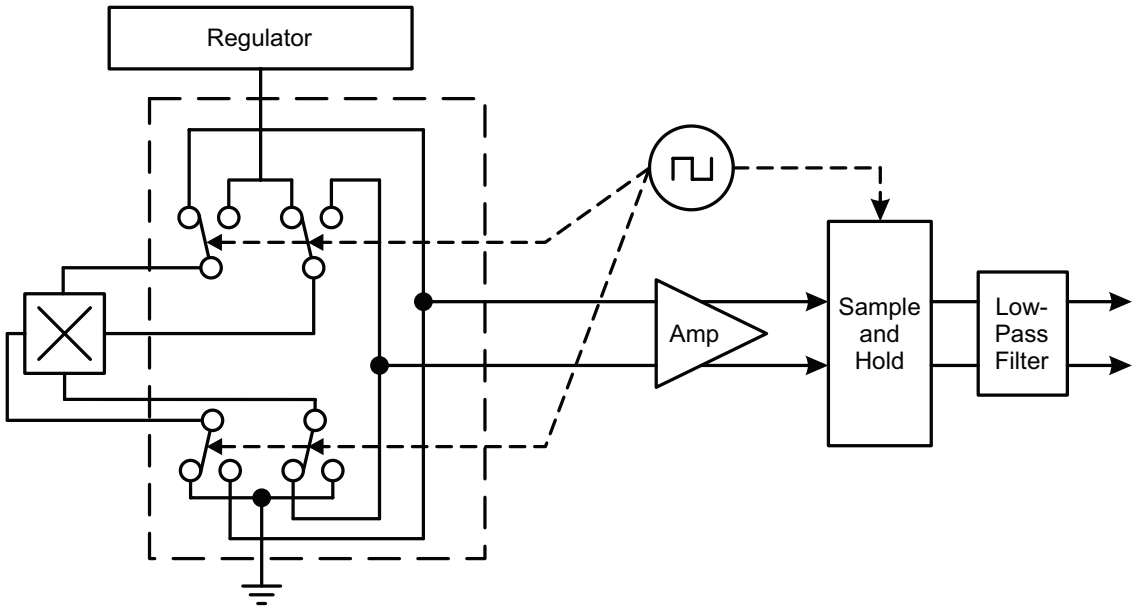

Figure 9: Example of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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Regulated Supply

This device requires minimal protection circuitry for operation from a regulated power supply. The on-chip voltage regulator provides immunity to power supply variations between 3.3 V and 18 V. Because the device has open-drain outputs, pull-up resistors must be used. If protection against coupled and injected noise is required, then a simple bypass capacitor filter is recommended. Refer to the circuit in Figure 10 for an example.

Unregulated Supply

In applications where the A1232 receives its power from an unregulated source such as a car battery, additional measures may be required to protect it against supply-side transients. Specifications for such transients will vary so protection-circuit design should be optimized for each application. For example, the circuit shown in Figure 11 includes an optional Zener diode that offers additional high voltage load-dump protection and noise filtering by means of a series resistor and capacitor. In addition to this, an optional series diode is included, and this protects against high-voltage reverse battery conditions beyond the capability of the built-in reverse-battery protection.

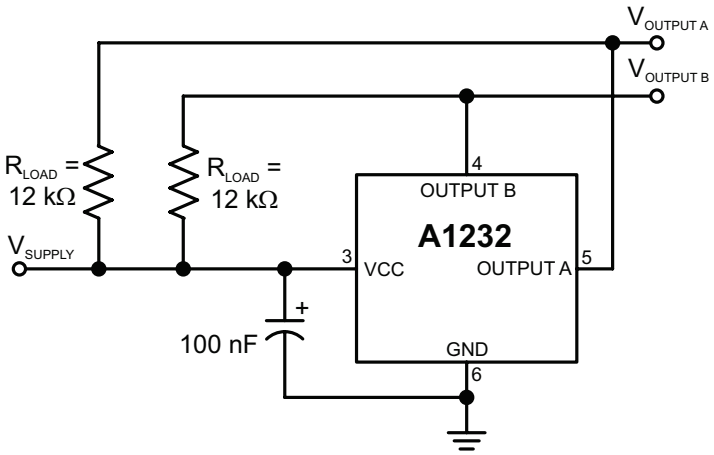

Figure 10: Typical Application Circuit for Regulated Power Supply

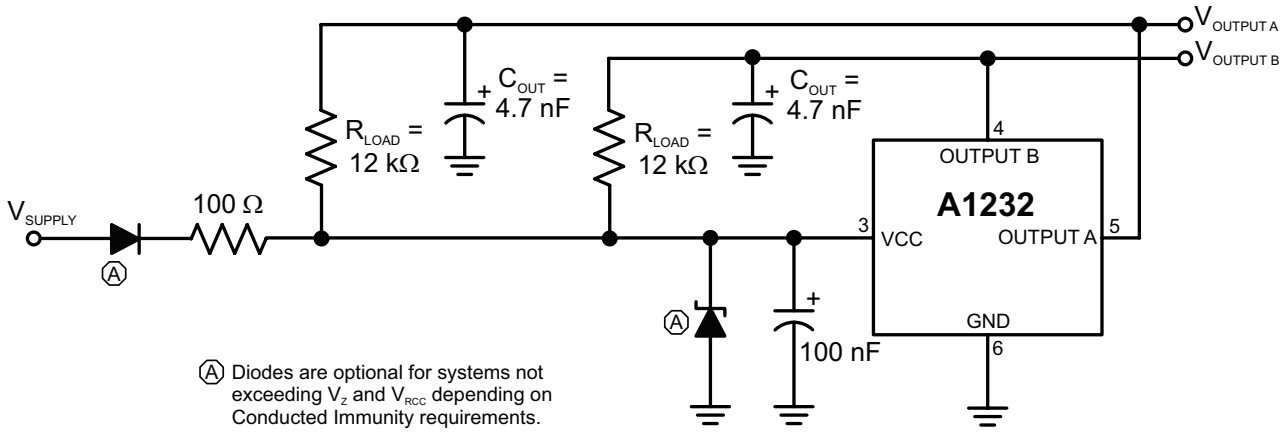

Figure 11: Typical Application Circuit for Unregulated Power Supply

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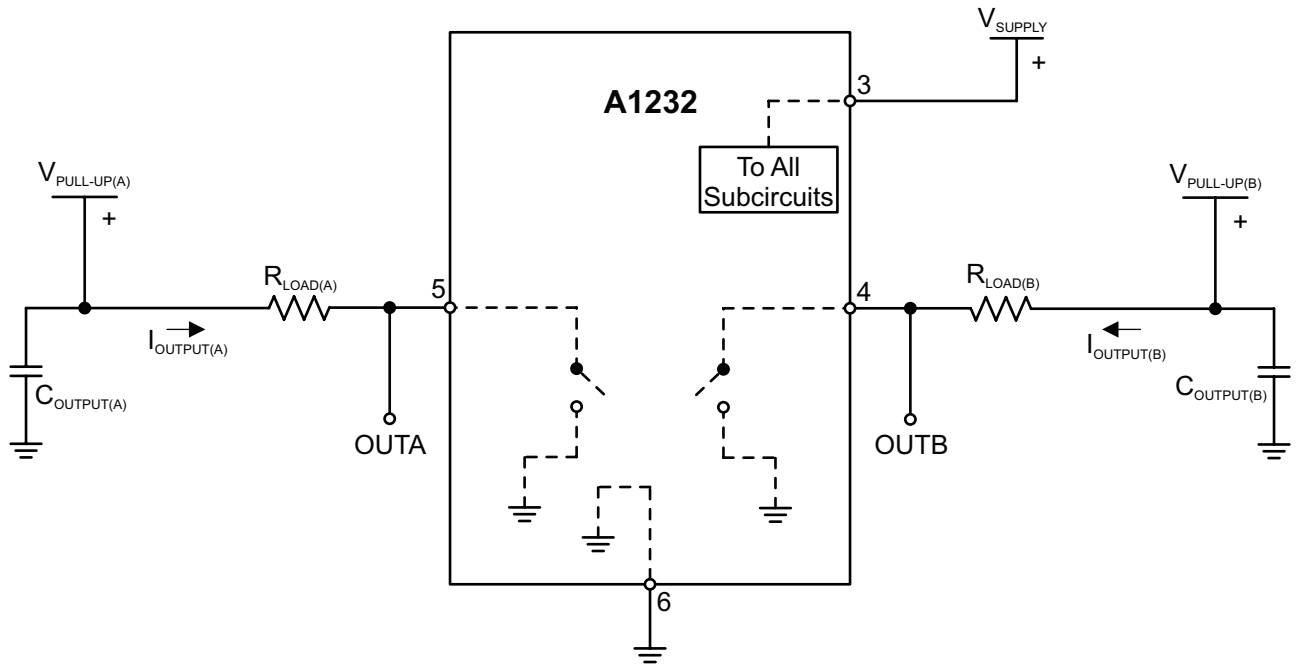

Figure 12: Application Circuit Example

Table 1: Circuit Analysis Example

STARTUP OPERATION ANALYSIS				
Condition	**$V_{PULL-UP(A/B)}$ (V)**	**$R_{LOAD(A/B)}$ (Ω)**	**OUTPUT (V)**	**$I_{OUTPUT(A/B)}$ (Internally Limited)**
$t > t_{ON}$ Before first magnetic field transition of each channel $B_{RP} < B < B_{OP}$	3.3	2.8 k	1.9	0.5
	5	4.5 k	2.75	0.5
	12	12 k	6	0.5
	18	18 k	9.0	0.5
NORMAL OPERATION ANALYSIS				
Condition	**$V_{PULL-UP(A/B)}$ (V)**	**$R_{LOAD(A/B)}$ (Ω)**	**OUTPUT (mV) [12]**	**$I_{OUTPUT(A/B)}$ [13]**
$t > t_{ON}$ After first magnetic field transition of each channel $B > B_{OP}$	3.3	2.8 k	500	1
	5	4.5 k	500	1
	12	11.84 k	160	1
	18	875	500	20

[12] Except for the 12 V typical calculations, the output on voltage is assumed worse case of 500 mV. Actual application values will vary.
[13] Output sink current calculations are for demonstrational purposes only and actual $I_{OUT(ON)}$ and $V_{OUT(ON)}$ values will vary with different pull-up source and resistor values, in addition to T_J and V_{CC}. During normal operation the device's output sink current is internally limited to between 30 mA and 70 mA.

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J (Thermal data is also available on the Allegro MicroSystems Web site, www.AllegroMicro.com).

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:

T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 145°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 145°C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate ($P_{D\ (max)}$) represents the maximum allowable power level, without exceeding $T_{J\ (max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A = 150°C, package LE, using a four-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 145°C/W, $T_{J\ (max)}$ = 165°C, $V_{CC\ (max)}$ = 24 V, and $I_{CC\ (max)}$ = 6 mA.

Calculate the maximum allowable power level ($P_{D\ (max)}$). First, invert equation 3:

$$\Delta T\ (max) = T_{J\ (max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D\ (max)} = \Delta T\ (max) \div R_{\theta JA}$$

$$P_{D\ (max)} = 15°C \div 145°C/W = 103\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC\ (est)} = P_{D\ (max)} \div I_{CC\ (max)}$$

$$V_{CC\ (est)} = 103\ mW \div 6\ mA = 17.2\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC\ (est)}$.

Compare $V_{CC\ (est)}$ to $V_{CC\ (max)}$. If $V_{CC\ (est)} \leq V_{CC\ (max)}$, then reliable operation between $V_{CC\ (est)}$ and $V_{CC\ (max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC\ (est)} \geq V_{CC\ (max)}$, then operation between $V_{CC\ (est)}$ and $V_{CC\ (max)}$ is reliable under these conditions.

In cases where the $V_{CC\ (max)}$ level is known, and the system designer would like to determine the maximum allowable ambient temperature ($T_{A\ (max)}$), the calculations can be reversed.

For example, in a worst-case scenario with conditions $V_{CC\ (max)}$ = 24 V and $I_{CC\ (max)}$ = 6 mA, using equation 1 the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 6\ mA = 144\ mW$$

Then, by rearranging equation 3:

$$T_{A\ (max)} = T_{J\ (max)} - \Delta T$$

$$T_{A\ (max)} = 165°C/W - (144\ mW \times 145°C/W)$$

$$T_{A\ (max)} = 165°C/W - 20.88°C = 144.12°C$$

In another example, the maximum supply voltage is equal to $V_{CC(MIN)}$. Therefore, $V_{CC\ (max)}$ = 3.3 V and $I_{CC\ (max)}$ = 6 mA. By using equation 1 the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 3.3\ V \times 6\ mA = 19.8\ mW$$

Then, by rearranging equation 3:

$$T_{A\ (max)} = T_{J\ (max)} - \Delta T$$

$$T_{A\ (max)} = 165°C/W - (19.8\ mW \times 145°C/W)$$

$$T_{A\ (max)} = 165°C/W - 2.9°C = 162.1°C$$

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDED MO-153AA)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

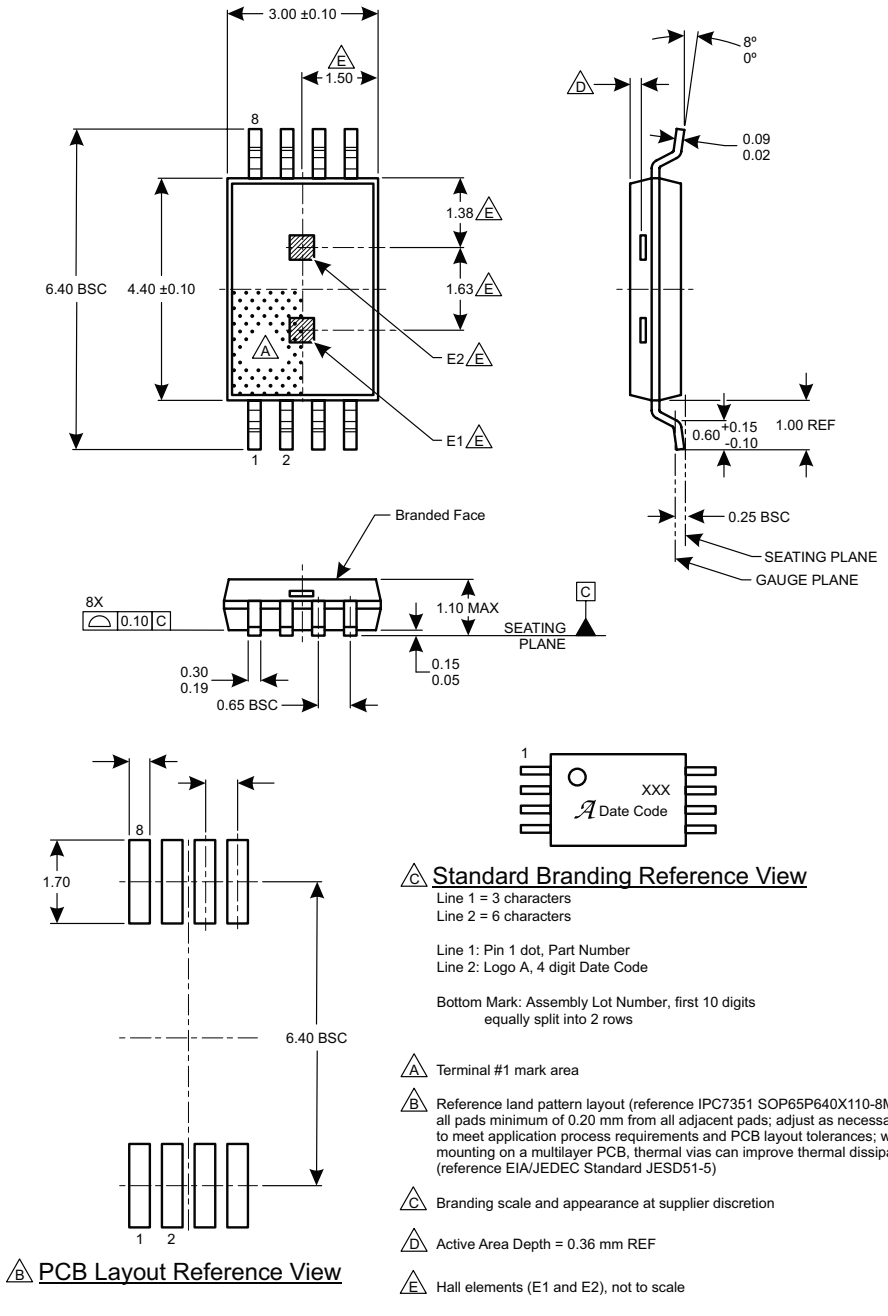

Figure 13: Package LE, 8-Pin TSSOP

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REVISION HISTORY

Number	Date	Description
–	December 10, 2014	Initial Release
1	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
2	February 19, 2019	Minor editorial updates
3	February 24, 2020	Minor editorial updates
4	February 16, 2022	Updated package drawing (page 20)
5	September 30, 2024	Updated product status to Last-Time Buy

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