A1335N

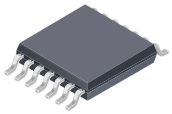
Programmable Hall-Effect Angle Sensor
Featuring Harmonic Compensation, I²C and SPI Interfaces

FEATURES AND BENEFITS

- 360° contactless high-resolution angle position sensor
- Circular vertical Hall (CVH) technology
- Digital output format selectable among serial port interface (SPI) and inter-integrated circuit (I²C)
- SPI interface allows use of multiple independent sensor ICs for applications requiring redundancy
- Refresh rate: 32 µs, 12-bit resolution
- Industrial temperature range: –40°C to 125°C
- Two types of linearization algorithms offered: harmonic linearization and segmented linearization
  - □ Enables off-axis operation
- Programmable range—can scale 22.5° to full-scale digital output
- Microprocessor-based output linearization
- EEPROM with error correction control (ECC) for trimming calibration
- 1 mm-thin (TSSOP) package
- Improved air gap performance, based on continuous background calibration

PACKAGE

Single SoC, 14-pin TSSOP (suffix LE)



Not to scale

DESCRIPTION

The A1335 is a 360° contactless high-resolution programmable magnetic angle position sensor IC. It is designed for digital systems and is capable of communicating via I²C or SPI.

This system-on-chip (SoC) architecture includes a front end based on circular vertical Hall (CVH) technology, programmable microprocessor-based signal processing, and an interface capable of supporting I²C and SPI. In addition to providing full-turn angular measurement, the A1335 also provides scaling for angle measurement applications of less than 360°. It includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible programming of calibration parameters.

Digital signal processing functions, including temperature compensation and gain/offset trim, as well as advanced output linearization algorithms, provide an extremely accurate and linear output for both end-of-shaft applications and off-axis applications.

The A1335 is designed with on-chip linearization to maximize performance in off-axis and on-axis applications. The linearization allows for compensation of systematic non-linearities due to mechanism placement and tolerancing, allowing the device to be used in position control application such as robotic joints, industrial automation, and mobile robot applications.

The A1335 is available as a single die in a 14-pin TSSOP. The package is lead (Pb) free with 100% matte tin leadframe plating.

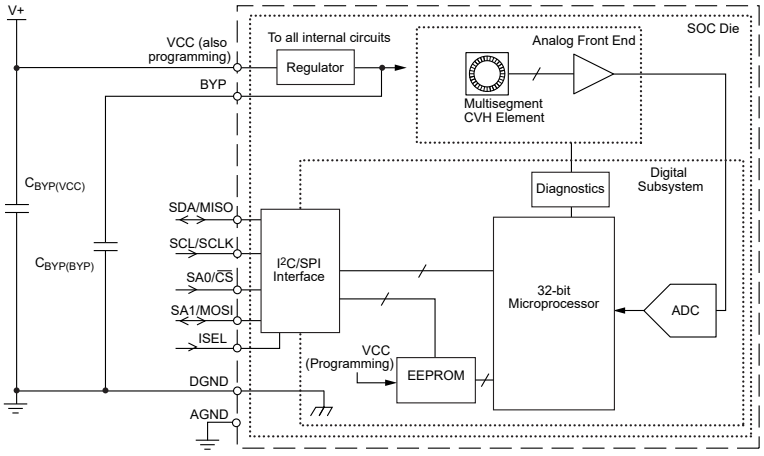


Figure 1: Functional Block Diagram

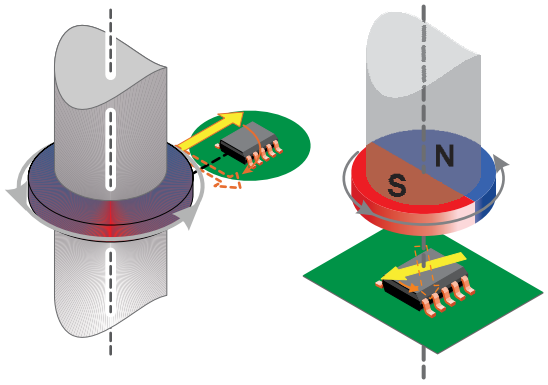


Figure 2: Industry-leading linearization enables off-axis (left) and on-axis (right) (side-shaft) operation

SELECTION GUIDE

Part Number	System Die	Package	Packing [1]
A1335KLEATR-N	Single	14-pin TSSOP	4000 pieces per 13-in. reel

[1] Contact Allegro for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		24	V
Reverse Supply Voltage	V_{RCC}		–18	V
All Other Pins	V_{IN}		–0.5 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

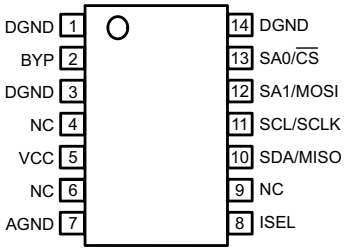
Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package	82	°C/W

[1] Additional thermal information available on the Allegro website.

Table of Contents

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST



LE-14 Package
(Single SoC)

Terminal List Table

Pin Name	Pin Number	Function
DGND	1, 3, 14	Device digital ground terminal.
BYP	2	Internal bypass node, connect with bypass capacitor to DGND.
NC	4, 6, 9	Not Connected; connect to GND for optimal ESD performance.
VCC	5	Device power supply and input for EEPROM writing pulses.
AGND	7	Device analog ground terminal.
ISEL	8	Selects between I²C operation (set to logic low) or SPI operation (set to logic high)
SDA/MISO	10	I2C: Digital data terminal: digital output of evaluated target angle, also programming data input; open drain, pull up externally to 3.3 V. SPI: Master Input / Slave Output terminal.
SCL/SCLK	11	Digital input: Serial clock (I²C: SCL, SPI: SCLK); open drain, pull up externally to 3.3 V.
SA1/MOSI	12	I²C: SA1 digital input: Sets peripheral address bit 1 (LSB) [1]; tie to BYP for 1, tie to DGND for 0. SPI: Controller output/slave input terminal.
SA0_1/$\overline{CS}$	13	I²C: SA0 digital input. Sets peripheral address bit 0 (LSB) [1]; tie to BYP for 1, tie to DGND for 0. SPI: Chip-select input, active low.

[1] For additional information regarding the INTF register, I2CM field, refer to the Programming Reference addendum, EEPROM Description and Programming section.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS: Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}		–	15	20	mA
VCC Low Flag Threshold	$V_{CCLOW(TH)}$		4.4	4.55	4.75	V
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{ZCC} = I_{CC}$ + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Voltage	V_{RCC}	I_{RCC} = –3 mA, T_A = 25°C	–	–	–18	V
Power-On Time [3][4]	t_{PO}	T_A = 25°C	2	–	40	ms
SPI INTERFACE SPECIFICATIONS [5]						
Digital Input High Voltage [3]	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage [3]	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, T_A = 25°C	2.93	3.3	3.69	V
SPI Output Low Voltage	V_{OL}	MISO pins	–	0.3	–	V
SPI Clock Frequency [3]	f_{SCLK}	MISO pins, C_L = 50 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [3]	D_{fSCLK}		40	–	60	%
Chip Select to First SCLK Edge [3]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [3]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [3]	t_{DAV}	Data output valid after SCLK falling edge	–	45	–	ns
MOSI Setup Time [3]	t_{SU}	Input setup time before SCLK rising edge	10	–	–	ns
MOSI Hold Time [3]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to $\overline{CS}$ Hold Time [3]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [3]	C_L	Loading on digital output (MISO) pin	–	–	50	pF
I²C INTERFACE SPECIFICATIONS (V_{PU} = 3.3 V on SDA and SCL pins)						
Bus Free Time Between Stop and Start [3]	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition [3]	$t_{HD(STA)}$		0.6	–	–	µs
Setup Time for Repeated Start Condition [3]	$t_{SU(STA)}$		0.6	–	–	µs
SCL Low Time [3]	t_{LOW}		1.3	–	–	µs
SCL High Time [3]	t_{HIGH}		0.6	–	–	µs
Data Setup Time [3]	$t_{SU(DAT)}$		100	–	–	ns
Data Hold Time [3]	$t_{HD(DAT)}$		0	–	900	ns
Setup Time for Stop Condition [3]	$t_{SU(STO)}$		0.6	–	–	µs
Logic Input Low Level (SDA and SCL pins) [6]	$V_{IL(I2C)}$		–	–	0.9	V
Logic Input High Level (SDA and SCL pins) [6]	$V_{IH(I2C)}$		2.1	–	3.63	V
Logic Input Current [3]	I_{IN}	V_{IN} = 0 V to V_{CC}	–1	–	1	µA
Output Voltage (SDA pin)	$V_{OL(I2C)}$	R_{PU} = 1 kΩ, C_B = 100 pF, T_A = 25°C	–	–	0.6	V
Logic Input Rise Time (SDA and SCL pins) [3]	$t_{r(IN)}$		–	–	300	ns

Continued on the next page…

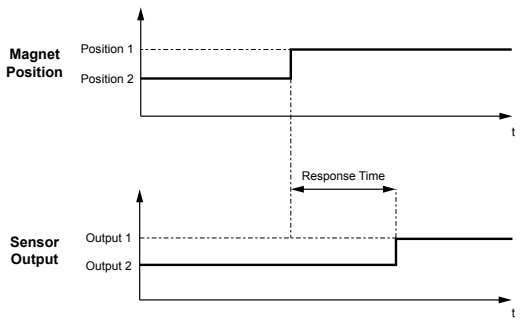
ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
I²C INTERFACE SPECIFICATIONS (V_{PU} = 3.3 V on SDA and SCL pins) (continued)						
Logic Input Fall Time (SDA and SCL pins) [3]	$t_{f(IN)}$		–	–	300	ns
SDA Output Rise Time [3]	$t_{r(OUT)}$	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
SDA Output Fall Time [3]	$t_{F(OUT)}$	R_{PU} = 1 kΩ, C_B = 100 pF	–	–	300	ns
SCL Clock Frequency [6]	f_{CLK}		–	–	400	kHz
SDA and SCL Bus Pull-Up Resistor	R_{PU}		–	1	–	kΩ
Total Capacitive Load on SDA Line [3]	C_B		–	–	100	pF
Pull-Up Voltage [3]	V_{PU}	R_{PU} = 1 kΩ, C_B = 100 pF	2.97	3.3	3.63	V
Magnetic Characteristics						
Magnetic Field [7]	B	Range of input field	–	–	1500	G
ANGLE CHARACTERISTICS						
Output Resolution [8]	RES_{ANGLE}	Angle word length	–	12	–	bit
Angle Refresh Rate [10]	t_{ANG}	ORATE = 0	–	32	–	µs
Response Time [11]	$t_{RESPONSE}$	All linearization and computations disabled, see Figure 3	–	60	–	µs
Angle Error [12][14]	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0, no linearization	–	±0.5	–	degrees
		T_A = 125°C, ideal magnet alignment, B = 300 G, target rpm = 0, no linearization	–1.75	–	+1.75	degrees
Angle Noise [12][13]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, 3 sigma value	–	0.5	–	degrees
		T_A = 125°C, B = 300 G, no internal filtering, 3 sigma value	–	0.6	–	degrees
Noise-Free Number of Bits [9]	b_{NOISE_FREE}	T_A = 25°C, ideal magnet alignment, B = 300 G, target RPM = 0, no linearization, ORATE = 0	–	8.5	–	bits
		T_A = 125°C, ideal magnet alignment, B = 300 G, target RPM = 0, no linearization, ORATE = 0	–	8.2	–	bits
Temperature Drift [14]	$ANGLE_{DRIFT}$	T_A = 125°C, B = 300 G	–1.5		1.5	degrees
		T_A = –40°C, B = 300 G	–	±1.2	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V and it is for design information only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Parameters for this characteristic are determined by design. They are not measured at final test.
[4] Power-on time may be reduced by disabling CVH self-test at power-on.
[5] During the power-on phase, the A1335 SPI transactions are not guaranteed.
[6] Parameter is tested at wafer probe only.
[7] The A1335 operates in Magnetic fields lower than 300 G, but with reduced accuracy and resolution. CVH self-test operation is not guaranteed at field levels above 300 G.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] The Noise-Free Number of Bits is defined as: $\log_2(\frac{360}{6\times\sigma})$ where σ is the standard deviation.
[10] The rate at which a new angle reading is ready. This value varies with the ORATE selection.
[11] This value assumes no post-processing and is the response time to read the magnetic position with no further computations. Actual response time is dependent on EEPROM settings. Settings related to filter design, signal path computations, and linearization will increase the response time.
[12] Error and noise values are with no further signal processing. Angle Error can be corrected with linearization algorithm, and Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value.
[13] 3 sigma value at 300 G. Operation with a larger magnetic field results in improved noise performance. For 600 G operation, noise reduced by 40-50% vs. 300 G.
[14] Performance based on characterization data, not directly measured at final test.



Definition of Response Time

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The A1335 incorporates a Hall sensor IC that measures the direction of the magnetic field vector through 360° in the X-Y plane (parallel to the branded face of the device). The A1335 computes the angle based on the actual physical reading, as well as any internal parameters that have been set by the user. The end user can configure the output dynamic range, output scaling, and filtering.

This device is an advanced, programmable internal microprocessor-driven system-on-chip (SoC). It includes a Circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter, digital filtering, a 32-bit custom microprocessor, a digital control interface capable of supporting I²C and SPI, and digital output of processed angle data.

Advanced linearization, offset, and gain adjustment options are available in the A1335. These options can be configured in onboard EEPROM providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Operation

The device is designed to acquire angular position data by sampling a rotating bipolar magnetic target using a multisegmented circular vertical Hall-effect (CVH) detector. The analog output is processed, then digitized and compensated before being loaded into the output register. For a depiction of the signal process flow described here, refer to Figure 3.

• ***Analog Front End.*** In this stage, the applied magnetic signal is detected and digitized for more-advanced processing.

A1 CVH Element. The CVH is the actual magnetic-sensing element that measures the direction of the applied magnetic vector.

A2 Analog Signal Conditioning. The signal acquired by the CVH is sampled.

A3 Analog-to-Digital Converter. The analog signal is digitized and handed off to the digital-front-end stage.

• ***Digital Front End.*** In this preprocessing stage, the digitized signal is conditioned for analysis.

D1 Digital Signal Conditioning. The digitized signal is decimated and bandpass filtered.

D2 Raw Angle Computation. For each sample, the raw angle value is calculated.

• ***Microprocessor.*** The preprocess signal is subjected to various user-selected computations. The type and selection of computations used involves a trade-off between precision and increased response time in producing the final output.

P1 Angle Averaging. The raw angle data is received in a periodic stream, and several samples are accumulated and averaged based on the user-selected output rate. This feature increases the effective resolution of the system. The amount of averaging is determined by the user-programmable output rate (ORATE) field. The user can configure the quantity of averaged samples by powers of two to determine the *refresh rate*, the rate at which successive averaged angle values are fed into the post-processing stages. The available rates are set as shown in Table 1.

Table 1: Refresh Rates of Averaged Samples

ORATE [2:0]	Quantity of Samples Averaged	Refresh Rate (µs)
000	1	32
001	2	64
010	4	128
011	8	256
100	16	512
101	32	1024
110	64	2048
111	128	4096

P1a IIR Filter (Optional). The optional infinite impulse response (IIR) filter can provide more-advanced multiorder filtering of the input signal. Filter coefficients can be user-programmed, and the filter (FI) bit can be programmed by the user to enable or disable this feature.

P2 Angle Compensation. The A1335 is capable of compensating for drift in angle readings that result from changes in the device temperature through the operating ambient temperature range. The device comes from the factory preprogrammed with coefficient settings to allow compensation of linear shifts of angle with temperature.

P2a Prelinearization Rotation (Optional, but required if linearization is used). The linearization algorithms require input functions that are both continuous and monotonically increasing. The LR bit sets which relative direction of target rotation results in an increasing angle value. The bit must be set such that the input to the linearization algorithm is increasing.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

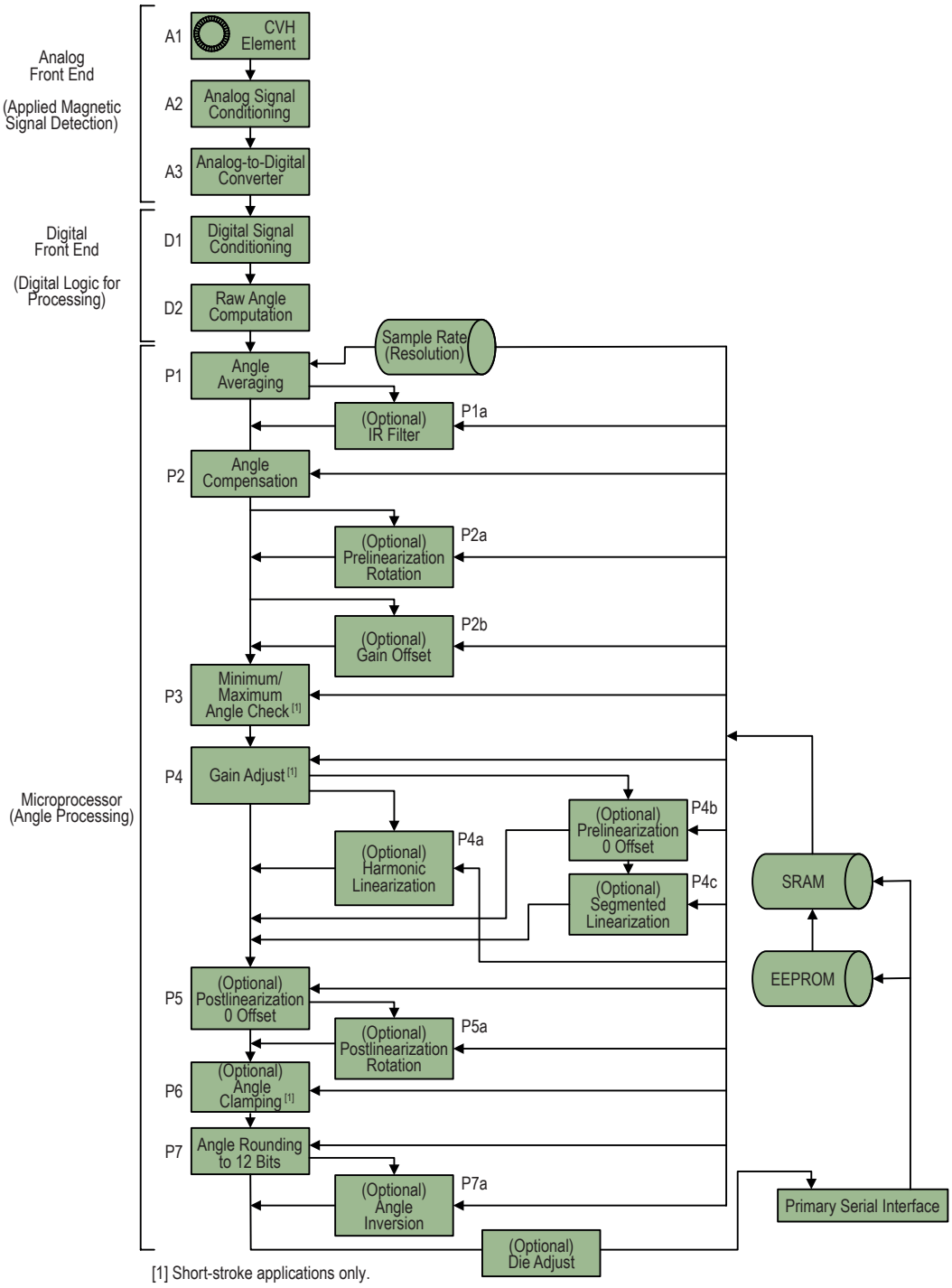


Figure 3: Signal Processing Flow (refer by index number to text descriptions)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

P2b Gain Offset (Optional). Allows zeroing out of the angle prior to applying gain. Set via the GAIN_OFFSET field.

$$\text{Angle} = \text{Angle} - \text{GAIN\_OFFSET}.$$

P3 Minimum/Maximum Angle Check (Short-Stroke Applications Only). The device compares the raw angle value to the angle-value boundaries set by user-programming of the MIN_ANGLE_S or MAX_ANGLE_S fields. If the angle is excessive, an error flag is set at ERR[AH] (high boundary violation) or ERR[AL] (low boundary violation). This feature is useful for applications that use angle strokes less than 360 degrees (short stroke). (Note: This feature is only active if the short-stroke bit has been set.)

P4 Gain Adjust (Short-Stroke Applications Only). This bit adjusts the output dynamic range of the device. For example, if the application only requires 45 degrees of stroke, the user can set this field such that a 45-degree angular change would be distributed across the entire 4095 → 0 code range. Set using the GAIN field. (Note: This feature is only active if the short-stroke bit has been set.)

P4a Harmonic Linearization (Optional). Applies user-programmed error correction coefficients (set in the LINC registers) to the raw angle measurements. Use the HL bit to enable harmonic linearization.

P4b Prelinearization 0 Offset (optional but required if segmented linearization is used). The expected angle values should be distributed throughout the input dynamic range to optimize angle post-processing. This is mostly needed for applications that use full 360-degree rotations. This value establishes the position that corresponds to zero error. This value should be set such that the 360 ≥ degree range corresponds to the 4095 ≥ 0 code range. Setting this point is critical if segmented linearization is used. This is required prior to going through linearization, as the compensation requires a continuous input function to operate correctly. Set using the LIN_OFFSET field.

P4c Segmented Linearization (Optional). Applies user-programmed error correction coefficients (set in the LINC registers) to the raw angle measurements. Use the SL bit to enable segmented linearization.

P5 Postlinearization 0 Offset (Optional). This computation assigns the final angle offset value, to set the low expected angle value to code 0 in the output dynamic range, after all linearization and processing has been completed. Set using the ZERO_OFFSET field.

P5a Postlinearization Rotation (Optional). This feature allows the user to chose the polarity of the final angle output, relative to the result of the prelinearization rotation direction setting (LR bit, previously described). Set using the RO bit.

P6 Angle Clamping (Short-Stroke Applications Only). The A1335 has the ability to apply digital clamps to the output signal. This feature is most useful for applications that use angle strokes less than 360 degrees. If the output signal exceeds the upper clamp, the output stays at the clamped value. If the output signal is lower than the lower clamp, the output stays at the low clamp value. Set using the CLAMP_HI and CLAMP_LO fields. (Note: This feature is only active if the short-stroke bit has been set.)

P7 Angle Rounding to 12 Bits. All internal calculations for angle processing in the A1335 are performed with 16-bit precision. This step rounds the data into a 12-bit word for output through the primary serial interface.

P7a Angle Inversion (Short-Stroke Applications Only). Rotation within the high and low clamp values:

$$\text{CLAMP\_HI} - (\text{Angle} - \text{CLAMP\_LO})$$

(Note: This feature is only active if the short-stroke bit has been set.)

P8 Die Adjust (Optional). Rotates final angle 180 degrees.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Diagnostic Features

The A1335 was designed with diagnostic requirements in mind and supports many on-chip diagnostics as well as error/status flags, enabling the host microcontroller to assess the operational status of each die.

In addition, the A1335 supports three different on-chip user-initiated diagnostics.

USER-INITIATED DIAGNOSTICS

The following three internal self-tests may be configured to run at power-on, and may also be initiated at any time by the system microcontroller via extended access commands through the SPI/I²C interface. A failure of any one of the three self-tests asserts the self-test (ST) failure flag within the extended error register. The specific failing test can be identified by performing an extended address read (address 0xFFFC).

- **CVH Self-Test**
  The CVH self-test is a signal-path diagnostic used to verify both analog and digital system integrity. Test execution requires approximately 36 ms, during which time no new angle measurements are generated by the sensor. The test is implemented by changing the transducer switch configuration from typical mode into a test configuration, allowing a test current to drive the CVHD in place of the magnetic field. By changing the direction of the test current and sequencing different elements within the CVH, the self-test emulates a changing magnetic-field angle. The measured angle is monitored to determine a passing or failing device. A failure of the CVH self-test asserts the ST flag. If the self-test was initiated via the extended access command, test results for the individual Hall elements are stored in the SRAM CMDSTATUS field (0x00) and the primary serial interface ERD register (0x0E through 0x11).
  Due to the sensitivity of the self-test, test results are only valid at field levels equal to or less than 300 G and temperatures at or above 25°C.
- **SRAM BIST**
  The SRAM built-in self-test (BIST) verifies proper functionality of the SRAM. The test may be run in either long or short mode, and can be configured to halt on error. A failure of the SRAM BIST asserts the ST flag. When enabled to run on power-up, the short-test mode is used, requiring approximately 100 µs to complete. For more information on SRAM BIST options, consult the A1335 programming guide.

Table 2: Status and Error Flags

Fault Condition	Description	Sensor Response
$V_{CC} < V_{CCLOW(TH)(min)}$	Indicates potential for reduced angle accuracy	UV error flag is set
$V_{CC} > 8.8$ V	Indicates possible system-level power supply failure	OV error flag is set [1]
Field > MAG_HIGH	MAG_HIGH programmable from 0 to1240 G in 40 G steps. Monitors level of MAG field in case of mechanical failure	MH flag is set
Field < MAG_LOW	MAG_LOW programmable from 0-620 G in 20 G steps. Monitors level of MAG field in case of mechanical failure	ML flag is set
–60°C > T_A > 180°C	Ambient temperature beyond maximum rating detected	TR flag is set
Processor Halt	Monitors digital logic for proper functionality	WT and WC flags are set
Single-Bit EEPROM Error (correctable)	Detects and corrects a single-bit EEPROM Error	ES error flag is set
Multi-Bit EEPROM Error (uncorrectable)	Detects a multi-bit uncorrectable EEPROM ERROR	EU error flag is set
Single-Bit SRAM Error (correctable)	Detects and corrects a single-bit SRAM Error	SS error flag is set
Multi-Bit SRAM Error (uncorrectable)	Detects a multi-bit uncorrectable SRAM ERROR	SU error flag is set
Angle-Processing Errors	New angle measurement did not occur within the maximum time allotted.	AT flag is set
Angle Out of Range	Angle value (prior to scaling by gain) is outside the range set by MIN_ANGLE and MAX_ANGLE. Short-stroke only.	AL or AH flag is set
Loss of V_{CC}	Determines if system power was lost. Also detects a reset of the internal microprocessor	POR and RC flags are set
Self-Test Failure	Indicates a failure of one of the three internal self-tests: SRAM BIST, ROM checksum verification, and CVH self-test. Tests can be individually configured to run at power-up and may also be user initiated.	ST flag is set

[1] EEPROM programming pulses result in OV flag assertion.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

- **ROM Checksum**
  Verification of the ROM checksum may be configured to occur at power-on. In addition, the checksum is continuously recalculated in the background during typical operation (independent of power-on configuration). This test may be initiated at any time by the system microcontroller via an extended access command (0xFFE0). If the self-test was initiated via the extended access command, the failing checksum is stored in the CMDSTATUS SRAM register (0x00). A bad ROM checksum asserts the self-test (ST) failure flag.

LOW VOLTAGE DETECTION

In addition to setting the undervoltage (UV) flag, a V_{CC} ramp also changes the state of the output pin (SDA/MISO) as the part enters and exits the reset condition. This is shown in Figure 4.

For more information about diagnostic features and flags, refer to the more-complete description of the available flags and settings in the A1335 Programming Manual. [1]

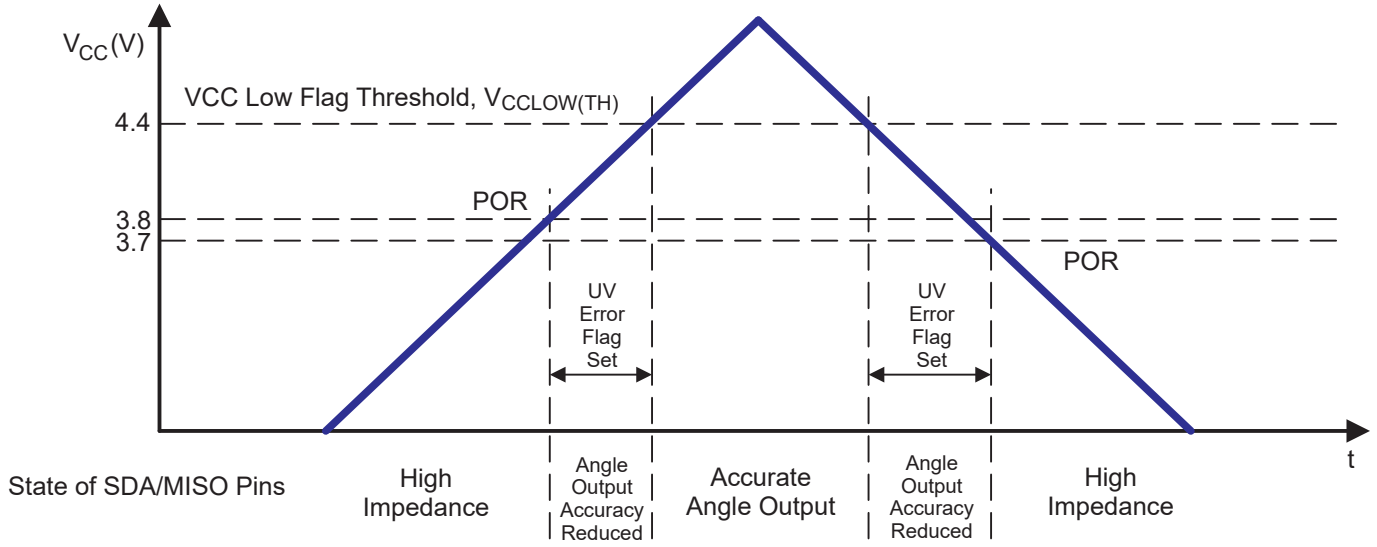


Figure 4: Relationship of V_{CC} and Output

Programming Modes

The EEPROM can be written through the dedicated I²C or SPI interface pins or via Manchester encoding on the VCC pin, allowing process coefficients to be entered and options selected. (Note: programming EEPROM also requires the VCC line to be pulsed, which could adversely affect other devices if powered from the same line). Certain operating commands also are available by writing directly to SRAM. The EEPROM and SRAM provide parallel data structures for operating parameters. The SRAM provides a rapid test and measurement environment for application development and bench-testing. The EEPROM provides persistent storage at the end of line for final parameters. At power-on initialization, the EEPROM contents are read into the corresponding SRAM. Provided the lock microprocessor (LM) bit within EEPROM is not set, SRAM can be overwritten during operation (use caution). The EEPROM is permanently locked by setting the lock EEPROM (LE) bit in the EEPROM.

The A1335 EEPROM is programmed via either the I²C, the SPI, or the VCC pin serial interface, with additional power provided by pulses on the VCC pin to set the EEPROM bit fields.

[1] https://www.allegromicro.com/en/products/sense/linear-and-angular-position/motor-position-sensors-2d/a1335

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C AND SPI INTERFACE

Interface Structure

The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information. All forms of communication operate through these registers, whether it be via I²C or SPI. These registers also provide a data and address location for accessing extended memory locations under control of the onboard processor. (EEPROM writing requires additional procedures. For more information, see the EEPROM Description and Programming section.)

- Table 3 lists the primary serial interface registers.
- Table 4 lists all of the bits by address in the primary interface registers.

Table 3: Primary Serial Interface Registers (Reserved Registers Not Shown)

Address [1] (Hex)	Name	Usage
02:03	EWA	Extended Write Address
04:07	EWD	Extended Write Data
08:09	EWCS	Extended Write Control and Status
0A:0B	ERA	Extended Read Address
0C:0D	ERCS	Extended Read Control and Status
0E:11	ERD	Extended Read Data
1E:1F	CTRL	Device control
20:21	ANG	Current angle and related data
22:23	STA	Device status
24:25	ERR	Device error status
26:27	XERR	Extended error status
28:29	TSEN	Temperature sensor data
2A:2B	FIELD	Magnetic field strength
34:35	ERM	Device error status masking
36:37	XERM	Extended error status masking

[1] Addresses that span multiple bytes are addressed by the most significant byte (lower address in the address range corresponds to the most significant byte).

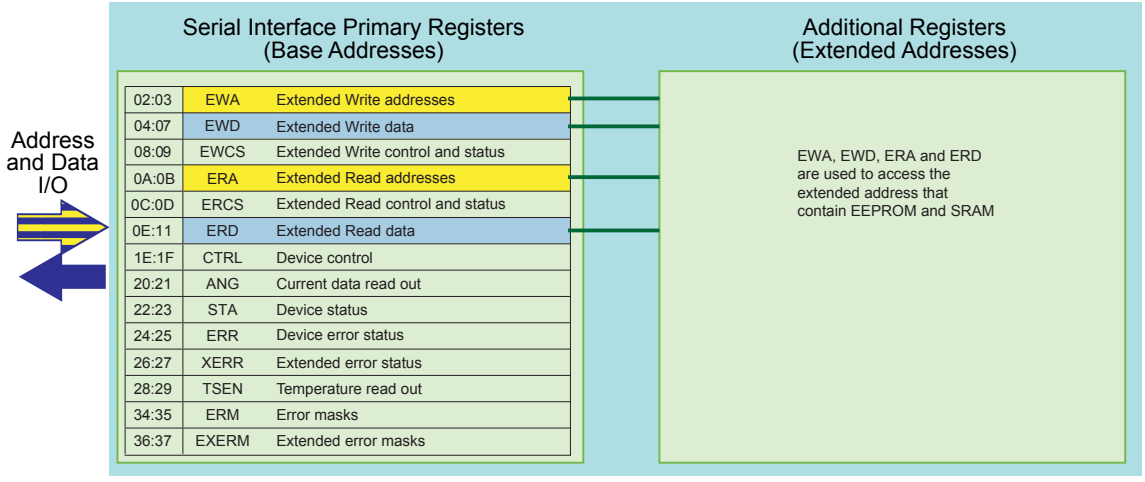


Figure 5: Basic address space for direct access by Serial Interface also provides registers for storing target addresses for extended memory areas, as well as for staging data transferred to and from those areas.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 4: Primary Serial Interface Registers Bits Map (Reserved Registers Not Shown)

Address [1] (0x00)	Register Symbol	Addressed Byte (MSB)								Addressed Byte + 1 (LSB)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
02:03	EWA	Addresses for Extended Memory Write															
04:05	EWD	Data for Extended Memory Write (EWD[31:16])															
06:07		Data for Extended Memory Write (EWD[15:0])															
08:09	EWCS	EXW	–	–	–	–	–	–	–	–	–	–	–	–	–	–	WDN
0A:0B	ERA	Addresses for Extended Memory Read															
0C:0D	ERCS	EXR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	RDN
0E:0F	ERD	Data for Extended Memory Read (ERD[31:16])															
10:11		Data for Extended Memory Read (ERD[15:0])															
1E:1F	CTRL	CDS		HDR	SFR	–	CSR	CXE	CER	KEYCODE							
20:21	ANG	RIDC	EF	NF	P	ANGLE											
22:23	STA	Register identifier code				POR	SR	NF	ERR	MPS				PHASE			
24:25	ERR	Register identifier code				XER	XOV	IER	CRC	NR	AT	AH	AL	OV	UV	MH	ML
26:27	XERR	Register identifier code				SS	ES	AW	TR	SU	EU	WC	WT	RC	XE	ME	ST
28:29	TSEN	Register identifier code				TEMPERATURE											
2A:2B	FIELD	Register identifier code				FIELD STRENGTH											
34:35	ERM	Register identifier code				–	XOV	IER	CRC	NR	APE	AH	AL	OV	UV	MH	ML
36:37	XERM	Register identifier code				SS	ES	AW	TR	SU	EU	WC	WT	RC	XE	ME	ST

[1] Addresses that span multiple bytes are addressed by the most significant byte.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C Interface Description

I²C is a serial interface that uses two bus lines, SCL and SDA, to access the internal device registers. Data is exchanged between a master controller (for example, a microcontroller) and the A1335, the slave. The master can directly read and write the primary serial interface registers (see Table 3). These registers are accessible without involving the A1335 processor, so are accessible with no additional latency. Extended addressing also is available, giving access to data through processor controlled code.

The clock input to SCL is generated by the master, while the SDA line functions as either an input or an open drain output, depending on the direction of the data transfer. I²C timing is summarized in Figure 6.

I²C communication is composed of several steps in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 device (slave) Address bits, plus 1 bit to indicate write (0) or read (1), followed by an acknowledge bit.
3. Data Cycles. Reading or writing 8 data bits, followed by an acknowledge bit. This cycle can be repeated for multiple bytes of data transfer. The first data byte on a write could be the register address. See the following sections for further information.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a start or stop condition, SDA must be stable while SCL is high. SDA can only be changed while SCL is low for data bits.

It is possible for the start or stop condition to occur at any time during a data transfer. The A1335 always responds by resetting the data transfer sequence.

The state of the read/write bit is set low to indicate a write cycle and set high to indicate a read cycle.

The master monitors for an acknowledge bit to determine if the slave device is responding to the address byte sent to the A1335. When the A1335 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A1335 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow the handshaking to occur.

The default slave address for the A1335 is 00011xx, where the two LSB bits are set by the package pins (SA1 and SA0) being tied high or low. This selects one of four unique hardware addresses, as follows:

Default I²C Slave Addresses

Pin Connection		Address Value
SA1 [A1]	SA0[A0]	
BYP	BYP	00011 11
BYP	GND	00011 10
GND	BYP	00011 01
GND	GND	00011 00

Refer to the INTF field (0x319) in the EEPROM description and Programming section for alternative, programmatic settings.

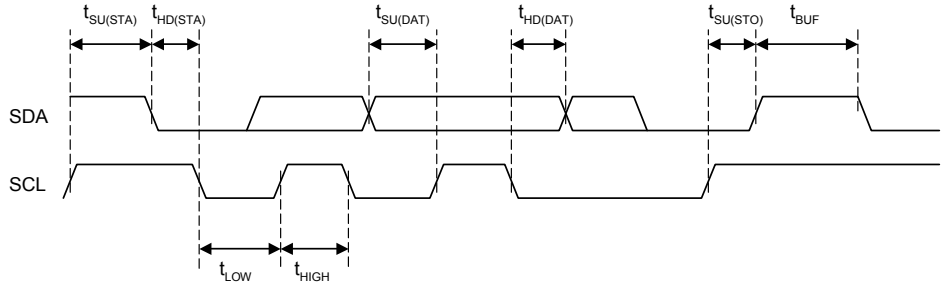


Figure 6: I²C input and output timing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The I²C is a byte-oriented protocol. The communication interface maintains an internal interface register pointer (IRP). This is always set by the first byte on an I²C write and then is indexed to each consecutive byte thereafter for every subsequent byte written or read. The primary serial interface registers memory locations are automatically read or written based on this IRP.

The following tokens are used as an I²C protocol glossary. Individual tokens may be composed of terms sent from both the master (the application microcontroller) and the slave (A1335), so bold typeface indicates terms sent by the slave to the master, and plain typeface indicates terms sent from the master to the slave.

• [S]: Start condition – bus becomes busy (master addresses a slave device)

• [RS]: Restart condition – same as [S], but within a transaction

• [P]: Stop condition – bus becomes free (no slave addressed)

• [SLVA+R/W+**[n]acK**]: 7-bit Slave device address, read/write mode bit, acknowledge bit from slave

• [IRP+ **[n]acK**]: 7-bit register address, acknowledge bit from slave

• [**D**+ [n]acK]: 8-bit read data from slave, acknowledge bit from master

Notes:
• The acknowledge bit can be either acK (0) or nacK (1).

• A *condition* is when the SDA line transitions high or low while the clock (SCL) is high. This is used to signal the beginning/end of I²C transactions on the bus.

Writing to Base Addresses with I²C

The I²C master controls the A1335 by programming it as a slave. To do so, the master transmits data bits to the SDA input of the A1335, in synchronization with the clocking signal it transmits simultaneously on the SCL input. The data stream of writing data to an individual register is shown in Figure 7.

The general I²C protocol to write a primary serial interface register is as follows:

[S][SLVA+W+**acK**][IRP+**acK**][D+**acK**]

A complete transmission begins with the master pulling SDA low (start bit) with SCL high, and completes with the master releasing the SDA line (Stop bit) with SCL high. Between these points, the master transmits a bit pattern consisting of: slave device (A1335) address bits, a write command bit (0), the target register address (within that slave device), and finally the data for the register.

After each byte, the slave A1335 acknowledges by transmitting a low to the master on the SDA line. After writing data to a register, if writing is completed the master must issue a stop or restart condition. If a stop or restart condition is not sent, then the next byte will be written to the current register address + 1 (IRP+1). Writing will continue in this fashion until the stop or restart condition is received.

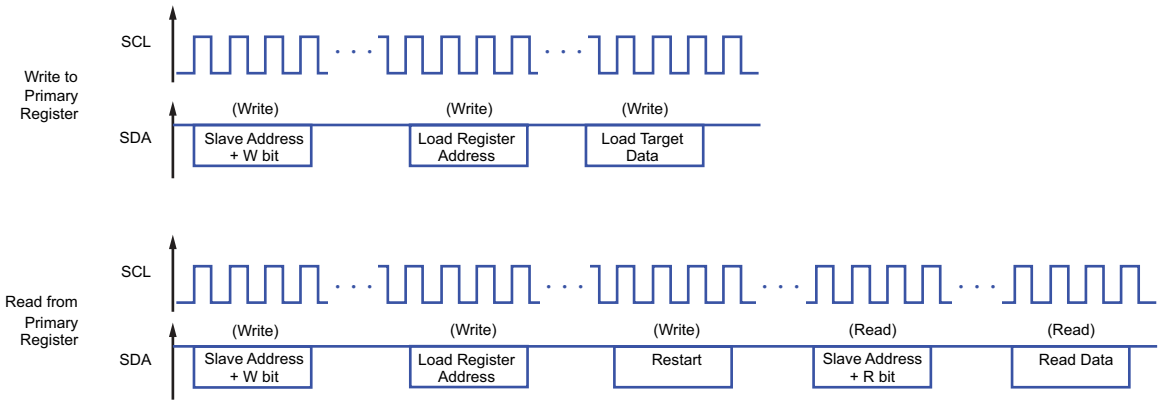


Figure 7: I²C Base Address Write and Read Sessions Examples.

High-voltage pulses are required on VCC only to invoke an EEPROM write.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

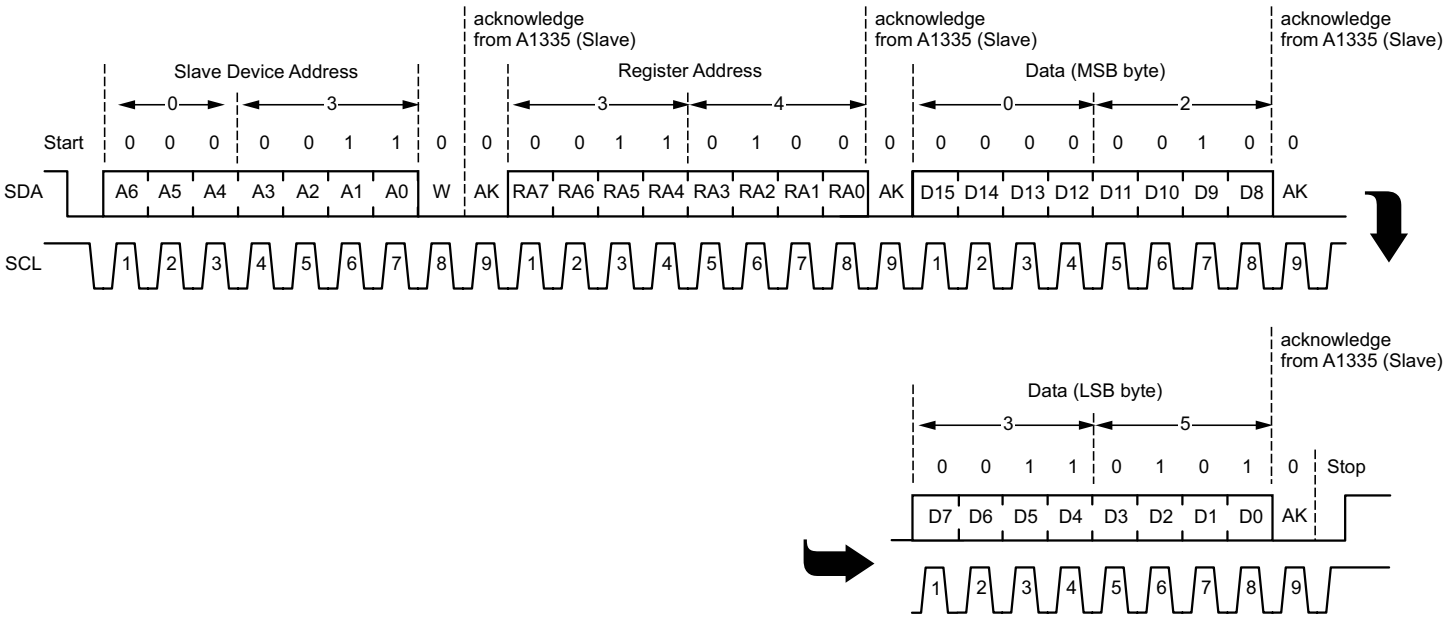


Figure 8: I²C Base Address Write: value 0x0235 to register address 0x34 (ERM) in slave device 0x3. All steps must occur immediately after the first step, with no intervening transmissions.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPI Interface Description

The A1335 provides a full-duplex 4-pin SPI interface for each die using SPI mode 3. The sensor responds to commands received on the corresponding MOSI (master-out slave-in), SCLK (serial clock), and CS (chip select) pins, and outputs data on the MISO (master-in slave-out) pin. The SPI pins double as I²C data, clock, and address lines. A separate ISEL (interface select) pin is used to select between the two communication protocols. SPI is selected when ISEL is brought to a logic high. This is easily accomplished by tying the ISEL pin directly to the BYP pin of the A1335, which provides a constant ≈2.8 V.

SPI Interface Timing

The SPI interface operates in pure Slave mode, with the master controlling the SCLK, MOSI, and CS lines. The master can maximize data throughput, up to f_{SCLK}(max) of 10 MHz. Figure 14 shows the timings of the write and read cycles.

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
SPI Interface Specifications [3]						
Digital Input High Voltage [4]	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage [4]	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, T_A = 25°C	2.93	3.3	3.69	V
SPI Output Low Voltage	V_{OL}	MISO pins	–	0.3	–	V
SPI Clock Frequency [4]	f_{SCLK}	MISO pins, C_L = 50 pF	0.1	–	10	MHz
SPI Clock Duty Cycle	D_{fSCLK}		40	–	60	%
Chip Select to First SCLK Edge [4]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [4]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [4]	t_{DAV}	Data output valid after SCLK falling edge	–	45	–	ns
MOSI Setup Time [4]	t_{SU}	Input setup time before SCLK rising edge	10	–	–	ns
MOSI Hold Time [4]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to $\overline{CS}$ Hold Time [4]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [4]	C_L	Loading on digital output (MISO) pin	–	–	50	pF

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V and it is for design information only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] During the power-on phase, the A1335 SPI transactions are not guaranteed.
[4] Parameters for this characteristic are determined by design. They are not measured at final test.

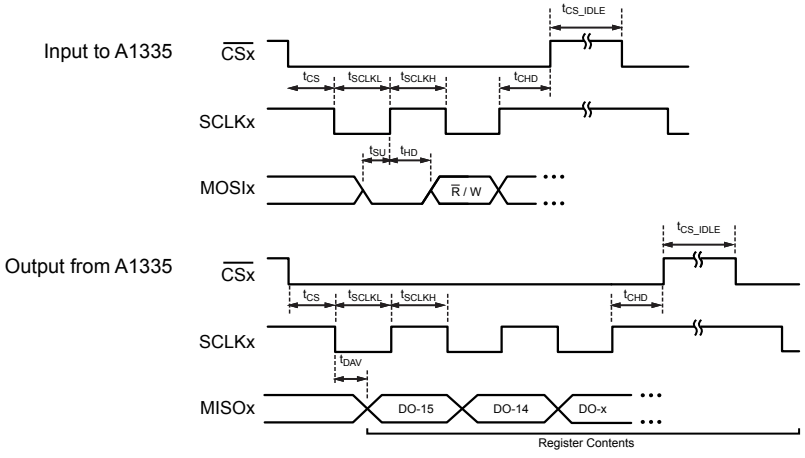


Figure 9: A1335 SPI Interface Timings: (upper) input and (lower) output

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPI Message Frame Size

A SPI transaction is a minimum of 16 bits in length. An extended 20-bit SPI packet allows 4 bits of CRC to accompany every data packet. The 4-bit CRC is automatically generated and placed on the MISO line once a 17th SCLK edge is detected by the A1335. The incoming CRC on the MOSI line is ignored unless the SC bit is set within EEPROM (0x319 bit 20). When enabled, a SPI packet with an incorrect CRC will be discarded, and the CRC error flag set (bit 8 within Serial register 0x24:0x25).

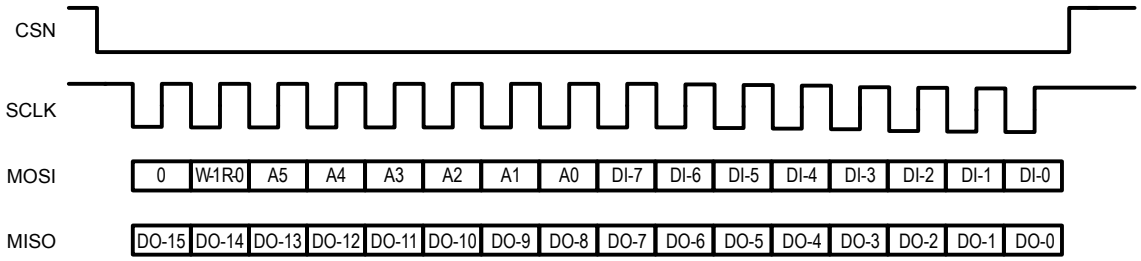


Figure 10: Sixteen Bit SPI Transaction

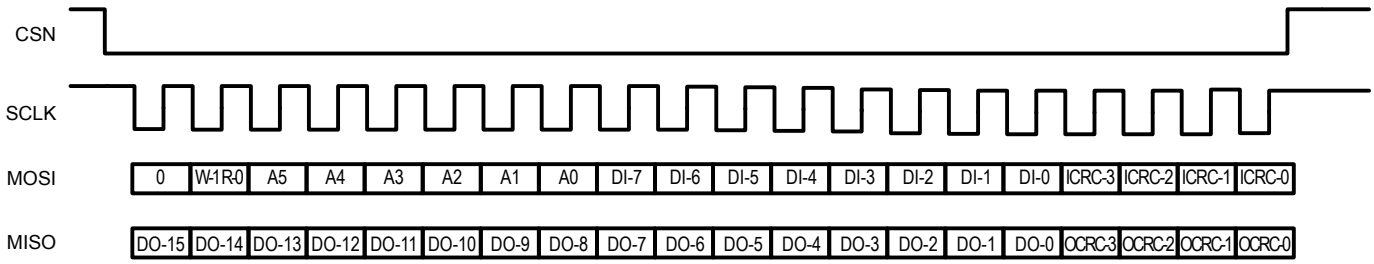


Figure 11: Twenty Bit SPI Transaction

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Write Cycle Overview

Write cycles consist of a 1-bit sync (low), a 1-bit $\overline{R}$/W asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16 bit serial register, two Write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the Master-generated SCLK signal. The complete SPI packet is latched on the rising edge of the master-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet. Including 16 data bits and 4 optional CRC bits, automatically included if a 17th SCLK edge is detected. The data bits correspond to the register contents selected during the previous read command. In the case where no previous read command was issued, the MISO line will transmit all zeros.

Read Cycle Overview

Read cycles have two stages: a Read command, selecting a serial register address, followed by another Read command to transmit the data from the selected register. Both commands consist of a 1-bit sync (low), a 1-bit $\overline{R}$/W asserted low, 6 address bits identifying the target register, and 8 data bits (all zeros because no data is being written).

In the first stage, as with the write command, read command MOSI bits are clocked-in on the rising edge of the master generated SCLK signal, and data latched on the rising edge of the ($\overline{CS}$) signal. During the first read stage, the simultaneous MISO signal output is the contents of the SPI read data from the previous read command cycle.

In the second stage, the read command continues on the next falling edge of the master-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, read 16 bits at a time. The MISO bits transmit on the falling edges of the SCLK signal, such that the Master can sample them on the SCLK rising edges.

Because a SPI read command can transmit 16 data bits at one time, and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame (See Table 6 for Serial Register format). This is accomplished by providing an even serial address value. If an odd value address is sent, only the contents of the single byte will be returned, with the eight most significant bits within the SPI packet set to zero.

Example: To read all 16 bits of the error register (0x24:0x25), a SPI read request using address 0x24 should be sent. If only the 8 LSBs are desired, the address 0x25 should be used.

Figure 19 shows examples of both a SPI write and a SPI read request, using a 16-bit SPI message frame.

(A) SPI Write example
(duplexed read available)

(B) SPI Read example:
register selection
(duplexed read available)

(C) SPI Read example:
data output from
selected register

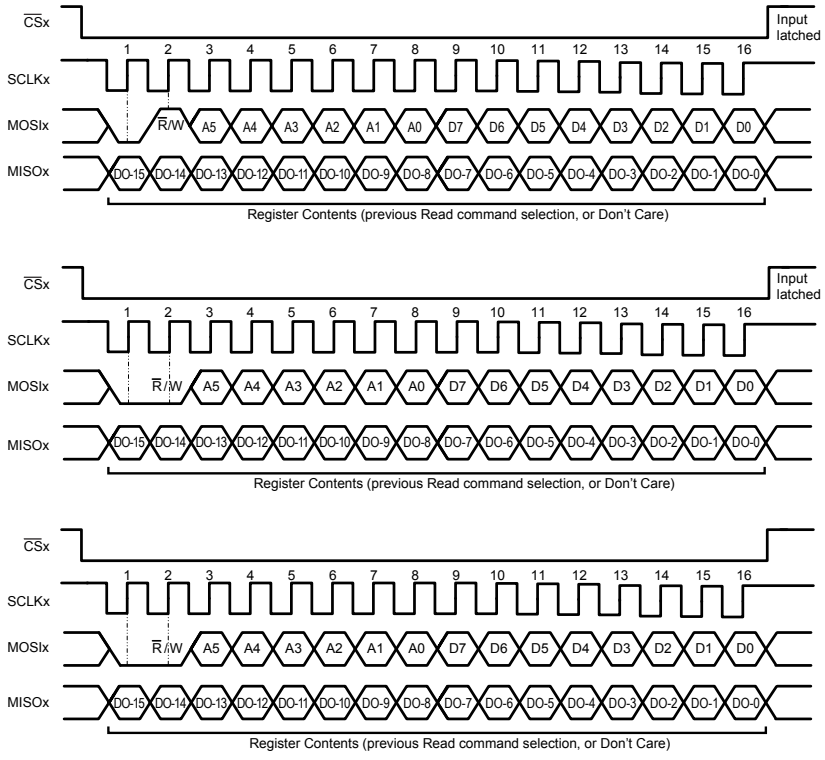


Figure 12: SPI Read and Write Pulse Sequences

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Writing to EEPROM

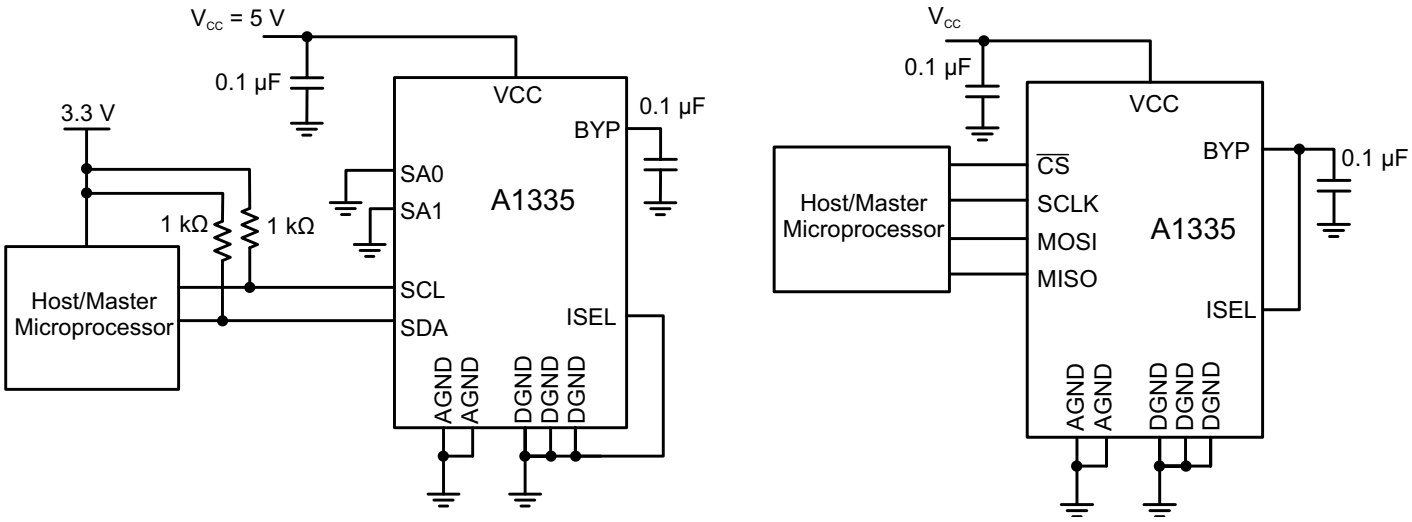
When a write command requires writing to nonvolatile EEPROM, after the write command, the controller must also send two *programming pulses*, high-voltage strobes via the VCC pin. These strobes are detected internally, allowing the A1335 to boost the voltage on the EEPROM gates. For specific details about sensor programming and protocols, refer to the A1335 Programming Manual.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Serial Interface Description

The A1335 features I²C- and SPI-compliant interfaces for communication with a host microcontroller or other controller. A basic circuit for configuring the A1335 package is shown in Figure 13.



(A) Typical A1335 configuration using I²C interface; A1335 set up for serial address 0xC

(B) Typical A1335 configuration using SPI interface

Figure 13: Typical A1335 configurations

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Magnetic Target Requirements

There are two main sensing configurations for magnetic angle sensing: on-axis and off-axis. On-axis (end of shaft) refers to when the center axis of a magnet lines up with the center of the sensing element. Off-axis (side shaft) refers to when the angle sensor is mounted along the edge of a magnet. On- and off-axis sensing configurations are illustrated in the Effect of Orientation on Signal section.

FIELD STRENGTH

The A1335 actively measures and adapts to its magnetic environment. This allows operation throughout a large range of field strengths (recommended range is 300 to 1000 G; operation beyond this range is allowed with no long-term impact). Due to the greater signal-to-noise ratio provided at higher field strengths, performance inherently increases with increasing field strength. Typical angle performance over applied field strength is shown in Figure 14 and Figure 15.

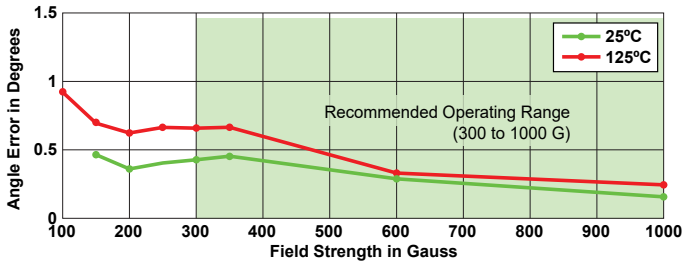


Figure 14: Typical Maximum Angle Error Over Field Strength

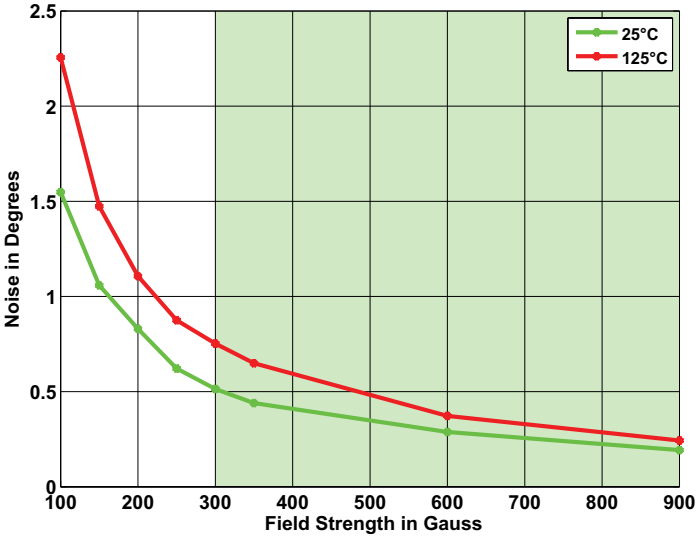
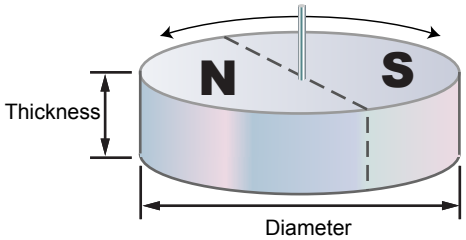


Figure 15: Typical One-Sigma Angle Noise Over Field Strength

Table 5: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (sintered) [1]	10	4
Neodymium (sintered)	8	3
Neodymium/SmCo	6	2.5



[1] A sintered neodymium magnet with 10 mm (or greater) diameter and 4 mm thickness is the recommended magnet for redundant applications.

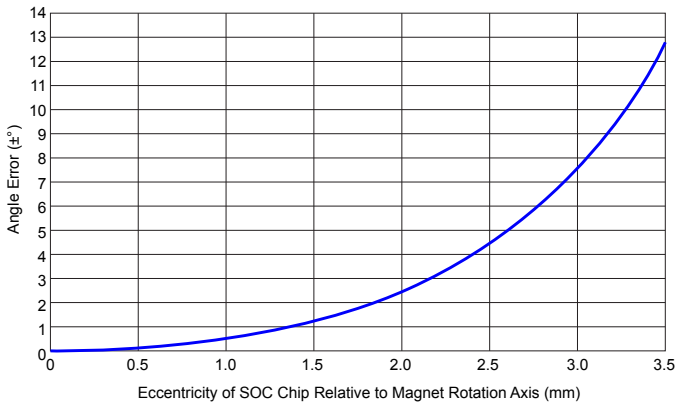


Figure 16: Simulated Error versus Eccentricity for a 10 mm × 4 mm Neodymium Magnet at a 2.7 mm Air Gap

Typical systemic error versus magnet to sensor eccentricity (d_{axial}), Note: “Systemic error” refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Calculating Target Zero-Degree Angle

When shipped from the factory, the default angle value when oriented as shown in Figure 17, is approximately 0° (180° on secondary die). In some cases, the end user may want to program an angle offset in the A1335 to compensate for variation in magnetic assemblies, or for applications where absolute system-level readings are required.

The internal algorithm for computing the output angle is:

$$Angle_{OUT} = Angle_{postLin} - Zero\ Offset\ . \quad (1)$$

The procedure to "zero out" the A1335 follows.

During final application calibration, position the magnet above the sensor in the required zero-degree position and record the angle reading from the device. Program the Zero Offset field in EEPROM (0x306 bits 12:0) with this value (for additional details, refer to the A1335 Programming Manual).

It is important to keep in mind that the zero offset adjustment occurs after linearization within the A1335 signal path (see Figure 1). As a result, the zero offset adjustment should be performed following end-of-line linearization.

Bypass Pin Usage

The bypass pin is required for proper device operation and is intended to bypass internal IC nodes of the A1335. A 0.1 µF capacitor must be placed in close proximity to the bypass pin. It is not intended to be used to source external components.

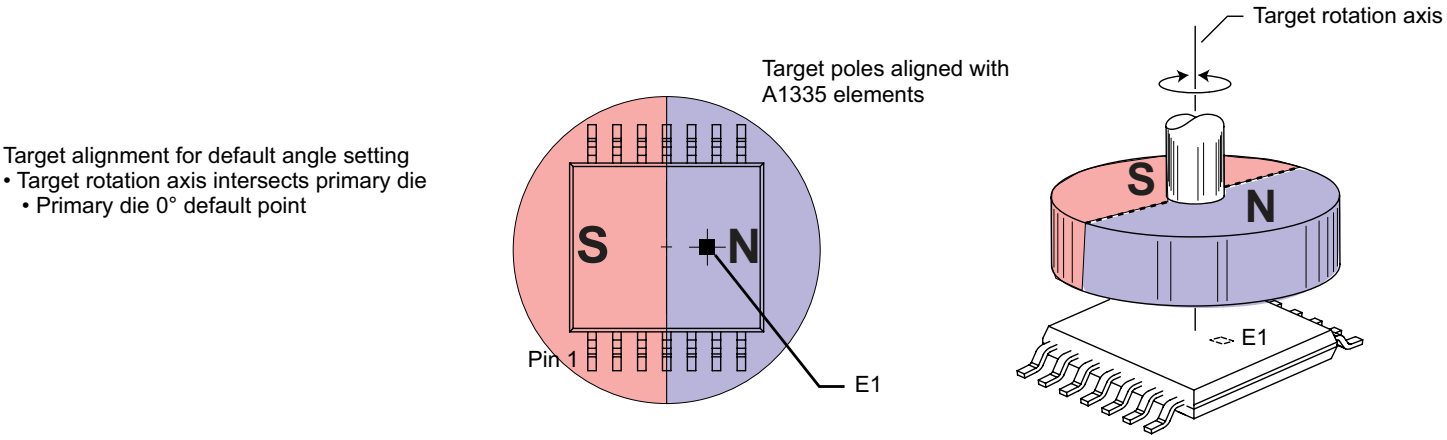


Figure 17: Orientation of Magnet Relative to Primary Die

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ON-AXIS APPLICATIONS

Some common on-axis applications for the device include digital potentiometer, motor sensing, power steering, and throttle sensing. The A1335 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 5. The device has two internal linearization algorithms that can compensate for much of the error due to alignment. For more-detailed information about magnet selection and theoretical error, contact Allegro.

OFF-AXIS APPLICATIONS

There are two major challenges with off-axis angle-sensing applications. The first is field strength. All efforts should be conducted to maximize magnetic signal strength observed by the device. The goal is a minimum of 300 G. Field strength can be maximized by using high-quality magnetic material, and by minimizing the distance between the sensor and the magnet. Another challenge is overcoming the inherent nonlinearity of the magnetic-field vector generated at the edge of a magnet. The device has two linearization algorithms that can compensate for much of the geometric error. Harmonic linearization is recommended for off-axis applications.

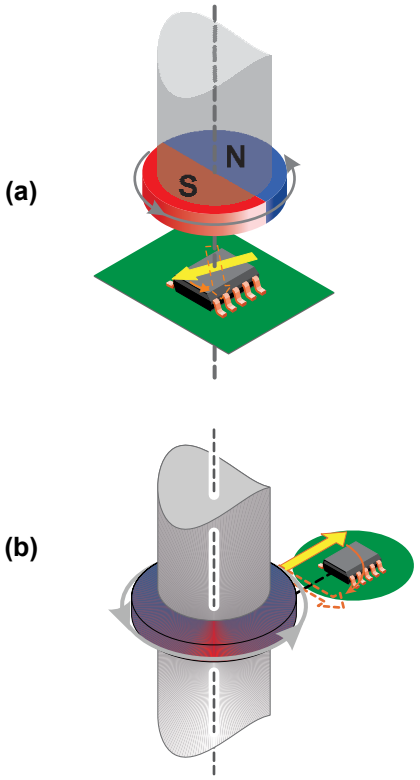


Figure 18: Typical On-Axis (a) and Off-Axis (b) Orientation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Effect of Orientation on Signal

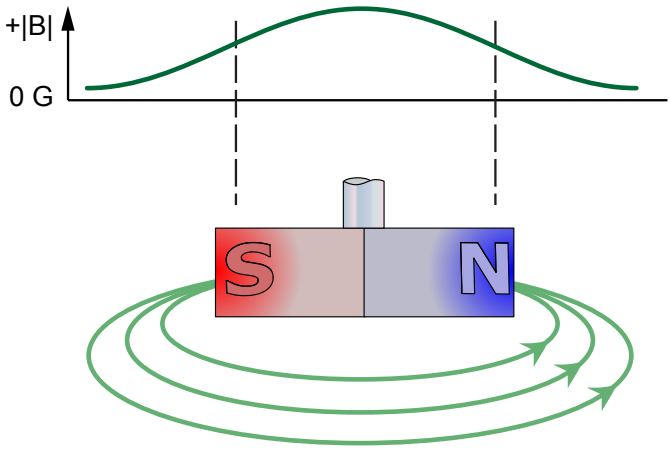


Figure 19: The magnetic field flux lines run between the north pole and south pole of the magnet. The peak flux densities are between the poles.

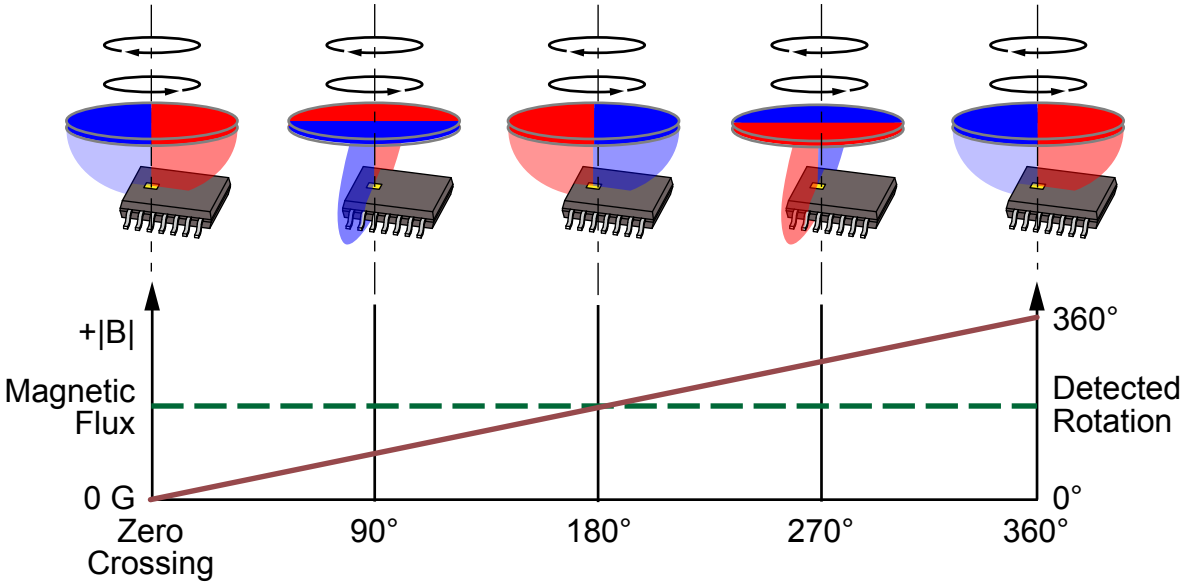


Figure 20: As the magnet rotates, the Hall element detects the rotating relative polarity of the magnetic field (solid line). When the center of rotation is centered on the Hall element, the magnetic flux amplitude is constant (dashed line).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

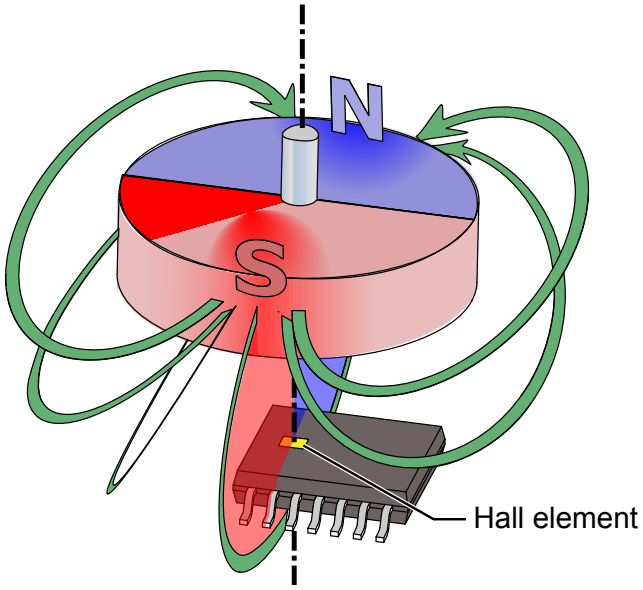


Figure 21: Centering the axis of magnet rotation on the Hall element provides the strongest signal in all degrees of rotation.

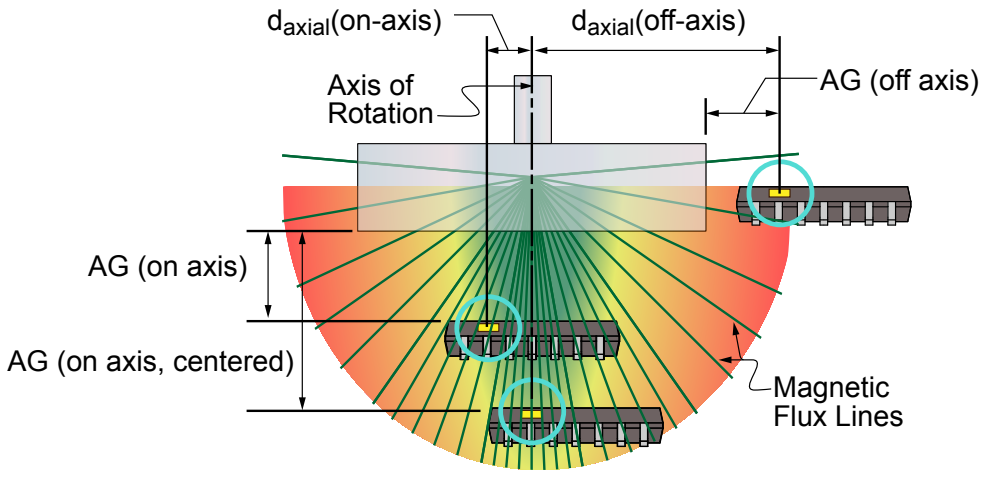


Figure 22: The magnetic flux density degenerates rapidly away from the plane of peak north-south polarity. When the axis of rotation is placed away from the Hall element, the device must be placed closer to the magnetic poles to maintain an adequate level of flux at the Hall element.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Linearization

Magnetic fields are generally not completely linear throughout the full range of target positions. This can be the result of non-uniformities in mechanical motion or of material composition. In some applications, it may be required to apply a mathematical transfer function to the angle that is reported by the A1335.

The A1335 has built-in functions for performing linearization on the acquired angle data. It is capable of performing one of two different linearization methods: harmonic linearization and piecewise (segmented) linearization.

Segmented linearization divides the output dynamic range into 16 equal segments. Each segment is then represented by the equation of a straight line between the two endpoints of the segment. Using this basic principle, it is possible to tailor the output response to compensate for mechanical nonlinearity.

Harmonic linearization uses the Fourier series to compensate for periodic error components. In the most basic terms, the Fourier series is used to represent a periodic signal using a sum of ideal periodic waveforms. The A1335 is capable of using up to 11 Fourier series components to linearize the output transfer function.

While it can be used for many applications, harmonic linearization is most useful for 360-degree applications. The error curve for a rotating magnet that is not perfectly aligned most often has an error waveform that is periodic. This phenomenon is especially true for systems where the sensor is mounted off-axis relative to the magnet. This periodic error is illustrated in Figure 23.

An initial set of linearization coefficients is created by characterizing the application experimentally. With all signal processing options configured, the device is used to sense the applied magnetic field at a target zero degrees of rotation reference angle and at regular intervals. For segmented linearization, 16 samples are taken: at nominal zero degrees and every 1/16 interval (22.5°) of the full 360° rotational input range. Each angle is read from the angle (ANG) register and recorded.

These values are loaded into the Allegro ASEK programming utility for the device, or an equivalent customer software program, to generate coefficients corresponding to the values. The user then uses the software load function to transmit the coefficients to the EEPROM. Each of the coefficient values can be individually overwritten during normal operation by writing directly to the corresponding SRAM.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

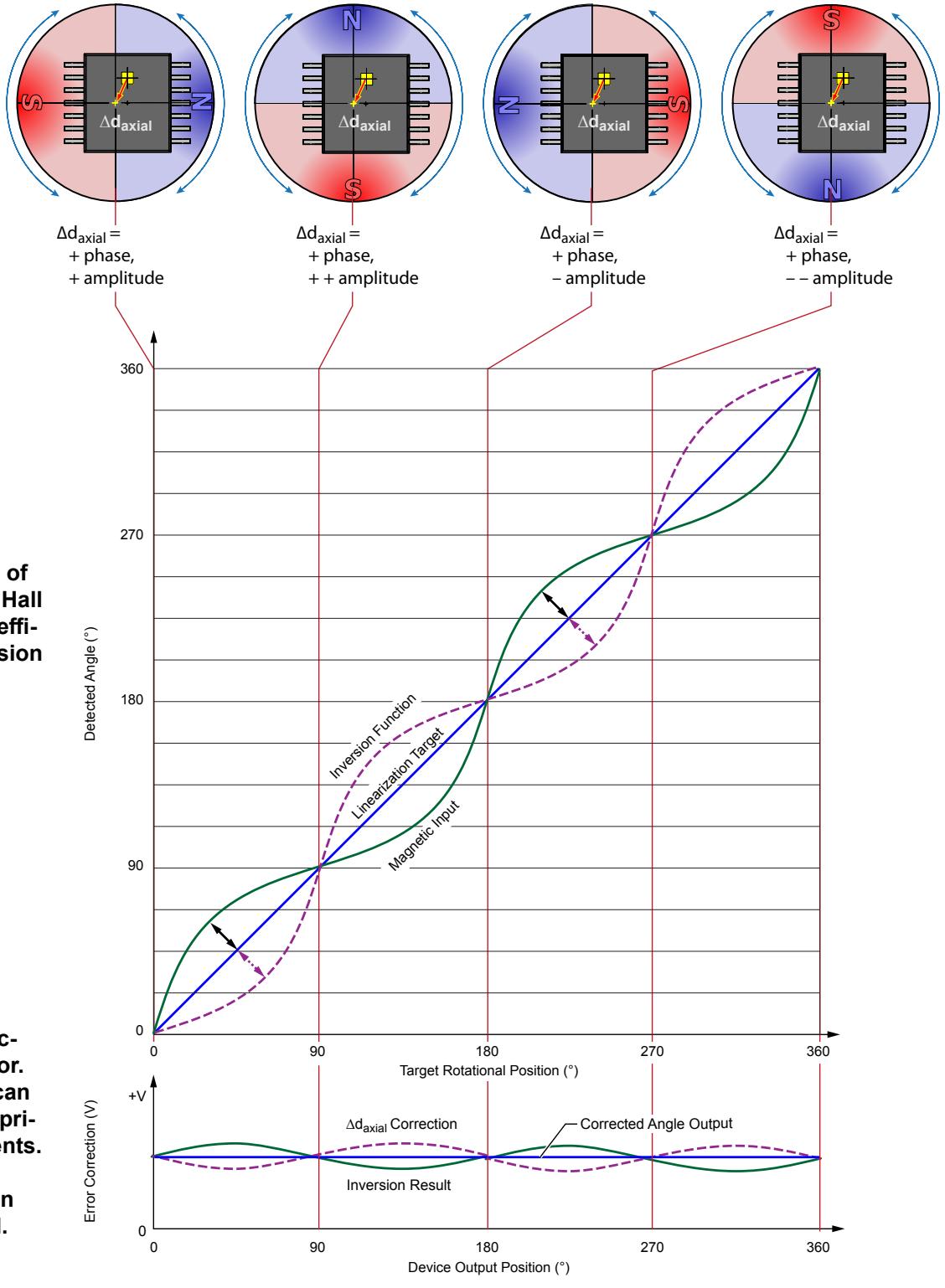


Figure 23a: With the axis of rotation aligned with the Hall element, linearization coefficients are a simple inversion of the input.

Figure 23b: Any eccentricity is evaluated as an error. Systematic eccentricity can be factored out by appropriate linearization coefficients. For off-axis applications, the harmonic linearization method is recommended.

Figure 23: Correction for Eccentric Orientation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

HARMONIC COEFFICIENTS

The device supports up to 11 harmonics. Each harmonic is characterized by an amplitude and a phase coefficient.

To apply harmonic linearization, the device:

1. Calculates the error factors.
2. Applies any programmed offsets.
3. Calculates the linearization factor as:

$$A_n \times sin(n \times t + \varphi_n)$$

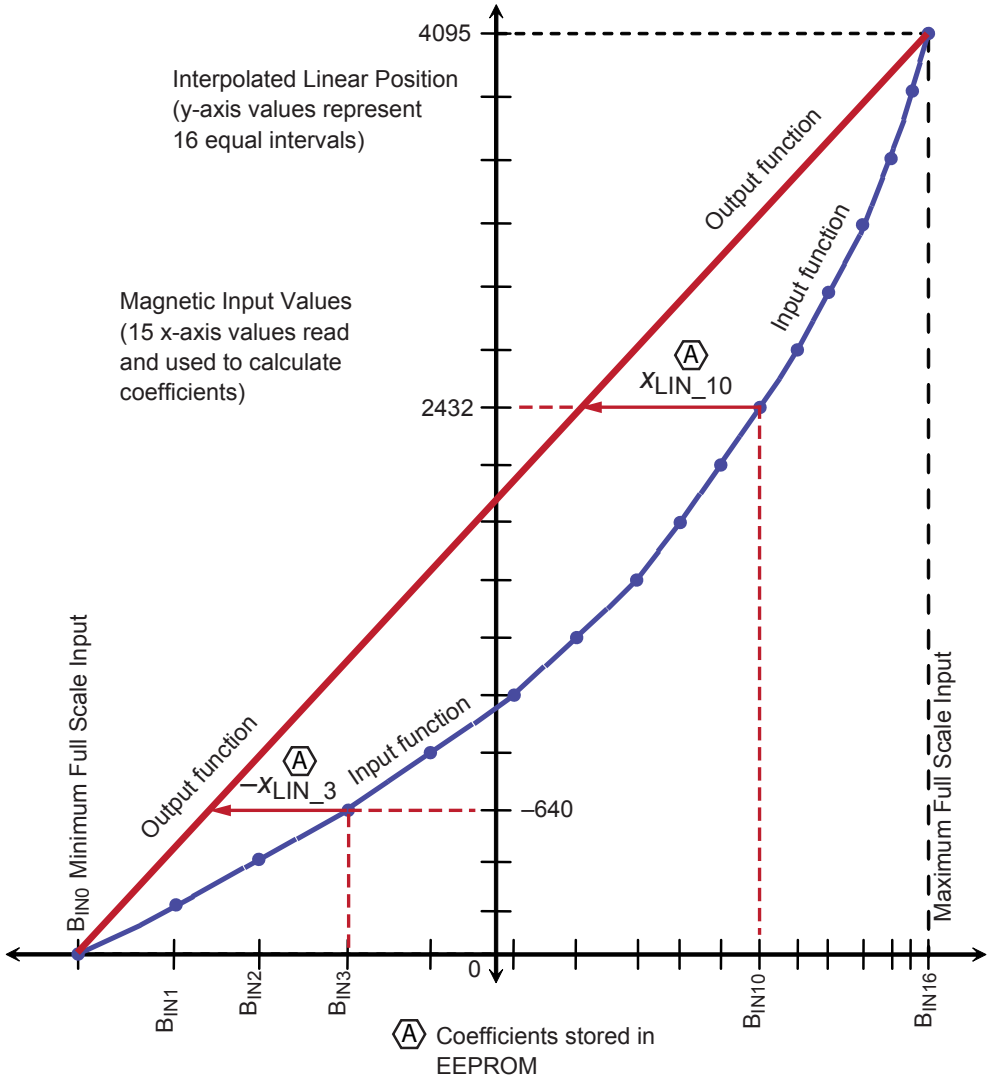


Figure 24: Sample of Linearization Function Transfer Characteristic

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TYPICAL PERFORMANCE CHARACTERISTICS

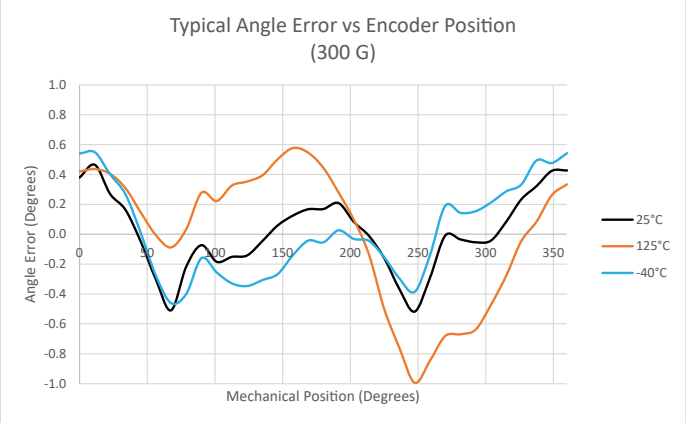


Figure 25: Typical Angle Error versus Encoder Position (300 G, 25°C)

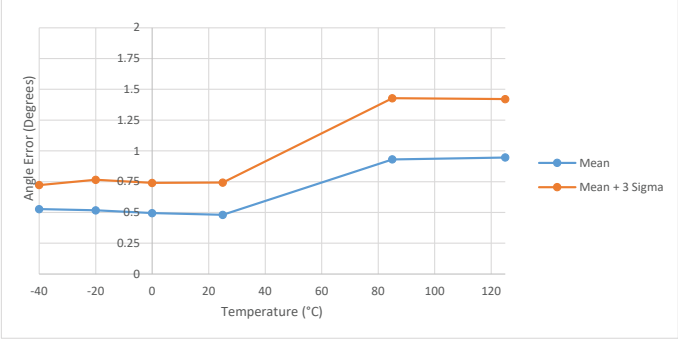


Figure 26: Peak Angle Error over Temperature (300 G)

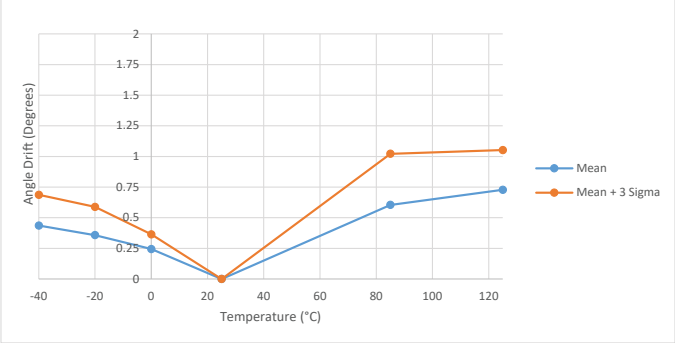


Figure 27: Maximum Temperature-Induced Drift from 25°C (300 G)

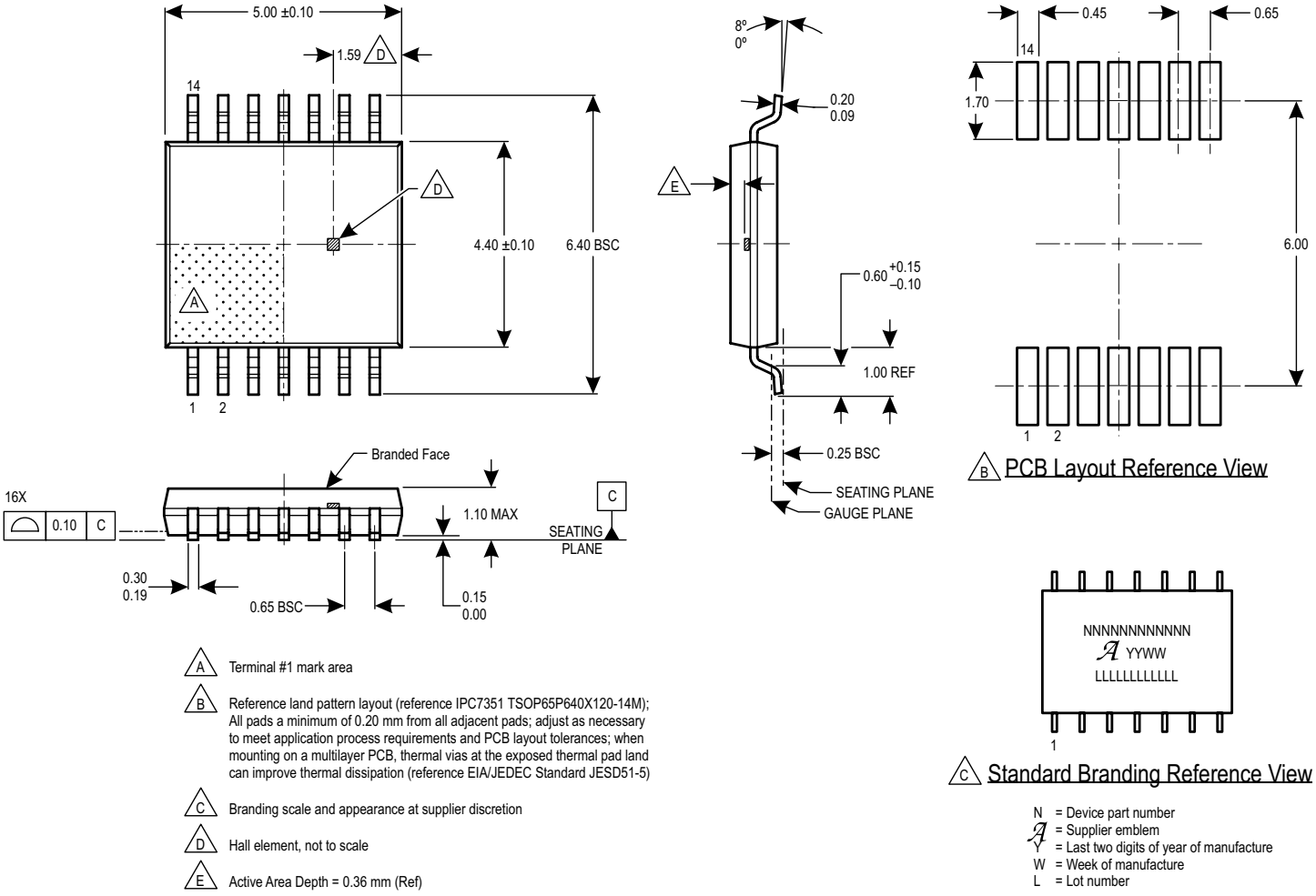
Note: Plots depict distributions taken from a laboratory characterization set. Data does not include shifts over lifetime.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 AB-1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth = 0.36 mm (Ref)

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 28: Package LE, 14-Pin TSSOP (Single-Die Version)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPENDIX A: SPI INTERFACE ERROR FLAG DESCRIPTION

IER Flag

The IER flag is located in bit 9 of the ERR serial register (0x24:0x25). This flag is designed to assert when the IC detects an improper communication frame, via either SPI or Manchester. For the purposes of this appendix, only the behavior in regards to the SPI bus is discussed. The IER flag asserts upon the following conditions:

- An improper number of SPI clocks is detected.
- The MSB of the MOSI packet is a logic = 1.

Table 6: Err Serial Register

Addr.	0x24								0x25							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Register identifier				XER	XOV	IER	CRC	NR	AT	AH	AL	OV	UV	MH	ML

Behavior When Sharing SPI lines

The IER flag may provide an erroneous indication when sharing the SCLK line among multiple ICs. In the case where an IC is held inactive by bringing the CS line high, the inactive IC(s) continue to count falling SCLK edges. This results in an invalid number of observed SCLK edges, and assertion of the IER flag on the next SPI transaction of the IC. False IER flag assertions differ based on the size of the SPI packet.

SIXTEEN BIT SPI PACKETS

The IER flag always asserts if, during the CS high period, the SCLK line is brought low as follows:

- At least one time, if using a 16-bit SPI packet.

Impact of IER Flagging with 16-Bit Packets

When an incorrect number of SCLK edges is observed by the IC, the following occurs:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read is not discarded, potentially corrupting the next immediate response from the device.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

TWENTY BIT SPI PACKETS

When using 20-bit SPI packets, the IER flag may occur when the SCLK line is brought low while CS is high. The probability of a false IER flag asserting is timing dependent and differs from device to device, but should not occur on more than 3.2% of all SPI transactions. Lab characterization has shown significantly lower assertion rates, with false flags on 0.00% to 0.80% of all SPI transactions.

Impact of IER Flagging with a 20-Bit Packet

When using a 20-bit SPI packet, if an incorrect number of SCLK edges is observed, the following occurs:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read occurs as expected.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

Avoiding IER Flag Assertion

The following methods may be used to avoid false IER flag assertions:

1. Use dedicated SCLK lines for each IC and hold the SCLK line high when CS is high.
   A. This prevents the IC from observing SCLK edge transitions when CS is high.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

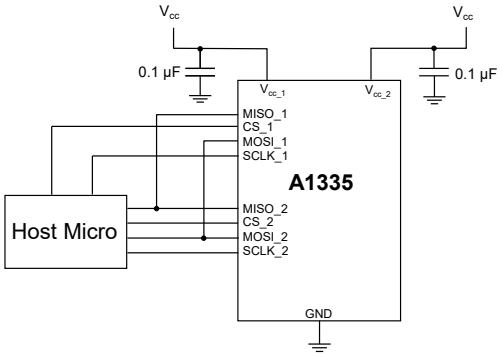


Figure 29: Separate SCLK Lines

2. Use a 21-bit SPI packet.

   A. When using a 21-bit SPI packet, the IC does not count SCLK edges when the CS pin is held high. This prevents the IER flag from improperly asserting, with the exception of power-on.

USING A 21-BIT SPI PACKET

No special EEPROM programming is required for the A1335 to support a SPI packet size of 21 bits; the controller must simply send 21 SCLK pulses during the CS low period. The format of the SPI message is shown in Figure 30.

The controller output-peripheral in (MOSI) signal consists of: a 1-bit SYNC bit defined as a logic of 0, 1-bit read/write (R/W), 6 address bits, 4 CRC bits, and an additional logic of 0. The extra logic of 0 sent on the 21st clock tick effectively shifts the standard 20-bit packet left by one place value.

The controller input-peripheral out (MISO) signal consists of: 16 data bits, the contents of which are determined by the address of the register being read, 4 CRC bits, and a repeat of the MSB of the CRC value. The repeated CRC bit shifted out on the 21st clock edge should be ignored by the controller when processing the CRC to validate the message contents.

POWER-ON BEHAVIOR WITH A 21-BIT SPI PACKET

If the SCLK line is shared on two or more ICs, the IER flag asserts on all idle A1335 die (CS held high) after the first SPI transaction (on the bus) following power-up. This occurs *independent* of the 21-bit SPI packet. This spurious IER flag asserts, on the idle die only during the first SPI transaction. All subsequent SPI transactions process correctly. This spurious assertion does not affect any future reads or writes to the device while power is maintained. If the IC is programmed to validate the CRC on MOSI, a CRC error flag (bit 8 of the ERR serial register) related to the spurious detection of a bad SPI packet also asserts.

To prevent an initial false error report that results from the initial assertion of the IER flag and risks the masking of real SPI communication issues, clear all error and warning flags on all A1335 ICs after power-on.

NOTE: This is a good practice that is also recommended independent of the false IER flag assertion.

By clearing the false IER flag, real SPI communication issues are not masked.

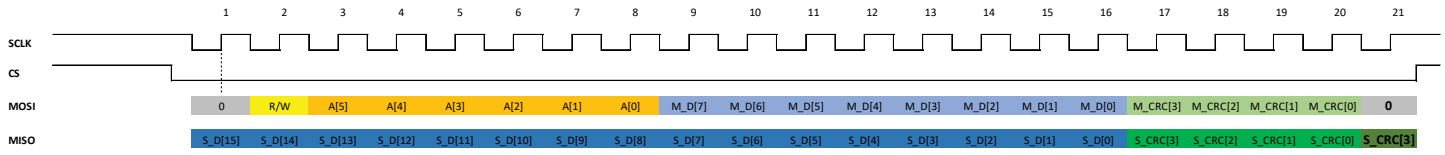


Figure 30: 21-bit SPI Packet Format

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Additional SPI Examples

The examples below show differing SPI implementations. All figures assume a shared SPI bus (MISO, MOSI, SCLK) between two sensors, with individual CS lines.

An example of pipelining SPI reads between two sensors, which can result in discarded packets or corrupted data when used with 16 SPI packets, is shown in Figure 31. In this example, SPI reads are bounced between Sensor 1 and Sensor 2, one frame at a time. During the interval in which the CS lines are high, the inoperative sensor detects an incorrect number of edges, asserting the IER flag and potentially corrupting the following read response.

A modified version of this pipelining approach is shown in Figure 32. The first read response from each sensor is known to be corrupt and is ignored. Because of this, the second read request (which results in the first read response on the next sequence) can be a NOP command, resulting in all zeros from the device (a NOP command is a read of serial register 0x0, which is hardcoded with all 0s). Inserting a NOP command between each valid read response ensures the data placed in the SPI buffers prior to the second response is valid.

It should be noted that the IER flag asserts on every changeover to a new die (CS line) when using this implementation due to the incorrect number of SCLK edges detected during the CS high period.

A 20-bit SPI packet is shown in Figure 33. This removes the potential for incorrect read data (assuming the SCLK edge occurs 70 ns or later following the CS rising edge), allowing the two sensors to be addressed in a sequential manner, one frame per sensor. This implementation has the added advantage of including a 4-bit CRC within each response. The IER flag may still assert when using a 20-bit packet.

Implementation of a 21-bit SPI packet is shown in Figure 34. This removes the false IER flag assertion and any potential for incorrect data interpretation. Allegro recommends using a 21-bit SPI packet when sharing SPI lines.

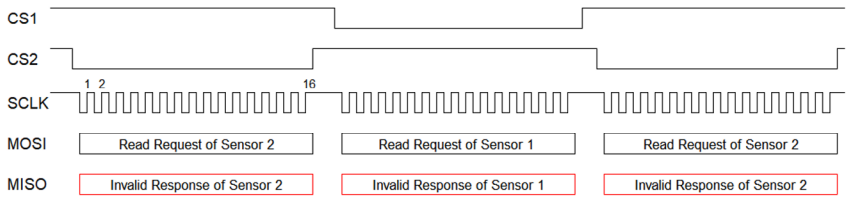


Figure 31: Implementation of SPI using 16-bit packets resulting in IER flag assertion and potentially corrupted data

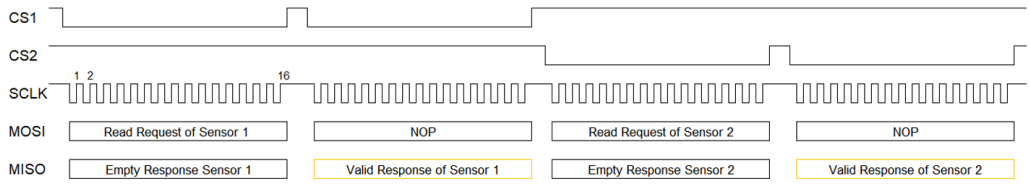


Figure 32: Implementation of SPI using 16-bit packets; valid data, IER flag still asserts

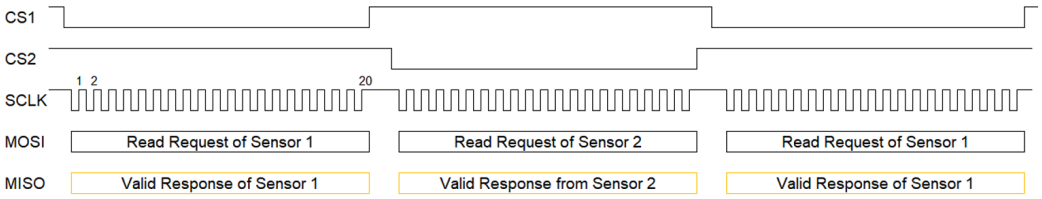


Figure 33: SPI Implementation using 20-bit packets; data contents are valid; however, IER flag may still assert

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

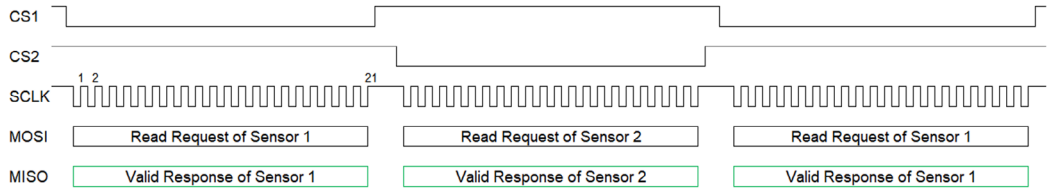


Figure 34: SPI Implementation using 21-bit packets; data contents are valid; no false IER flag generation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

REVISION HISTORY

Number	Date	Description	Pages	Responsible
–	September 23, 2025	Initial release	All	W. Wilkinson

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com