A17803

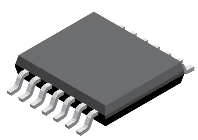
High-Speed Interface IC for Inductive Sensing with Digital Output

FEATURES AND BENEFITS

- Highly integrated inductive position sensor interface IC optimized for use in e-motor applications.
- State-of-the-art signal conditioning algorithms ensure high accuracy over a wide range of system configurations
- Up to 16-bit resolution at up to 250,000 rpm for traction motor and motor position sensing applications
- Large output interface selection: SPI, SENT, motorSENT, PWM, and ABI
- Qualified to AEC-Q100 grade 0
- ASIL-Compliant: ASIL C(D) safety element out of context (SEooC) developed in accordance with ISO26262, when used as specified in the safety manual

PACKAGE

Not to scale



14-pin TSSOP (Single Die, Suffix LE)

DESCRIPTION

The A17803 is a high-accuracy, high-resolution inductive position sensor interface IC for industrial and automotive applications. It is optimized for use as a position sensor interface in transmission actuators, traction motors, EPS electrical motors, and other high-speed applications.

The A17803 incorporates a coil driver for the transmitting application coil, and two receiving inputs for the receiving application coils. Both receiving signals are subjected to EMC filtering and demodulation in order to extract the target position information.

Compensation of possible error due to coils-target alignments and system design, located in the digital domain of signal path, offers offset adjustment, gain adjustment, and compensation of undesired electrical harmonics.

Due to the possibility of high-frequency input in e-motor applications, the device calculates the speed of the input signals and angle in order to reduce effective latency, resulting in fast tracking position sensing.

The A17803 is offered in surface-mount lead (Pb) free 14-pin TSSOP package.

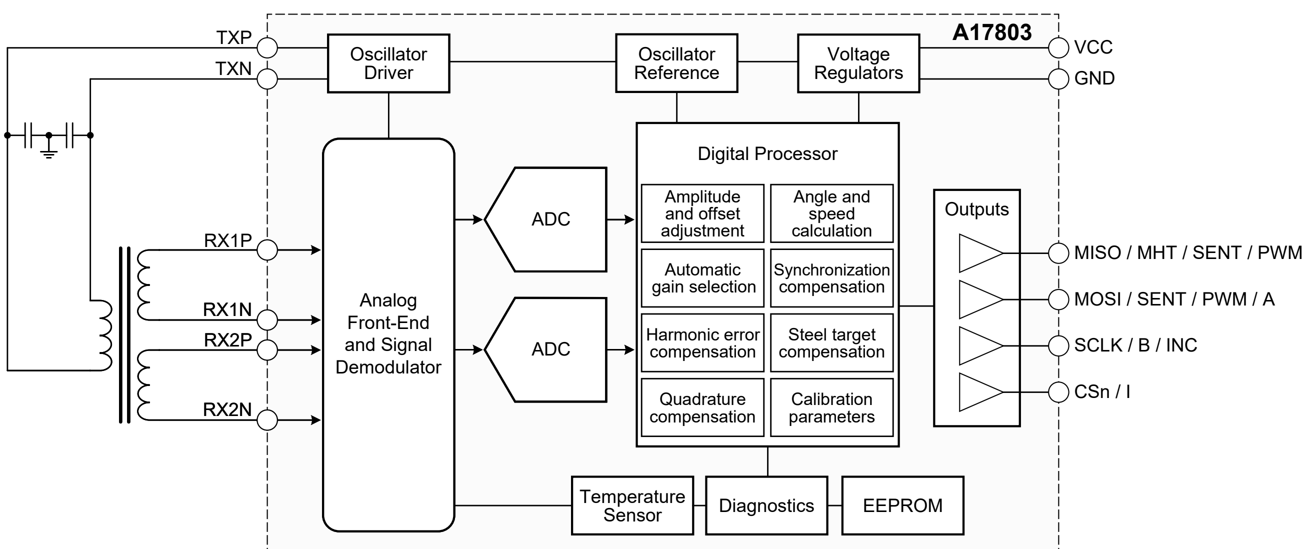


Figure 1: Functional Block Diagram

SELECTION GUIDE

Part Number	Programming Interface	Package	Packing
A17803PLEATR-M	Manchester	14-pin TSSOP	4000 pieces per 13-in reel
A17803PLEATR-S	SPI	14-pin TSSOP	4000 pieces per 13-in reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Refer to Power Derating section	24	V
Reverse Supply Voltage	V_{RCC}		–18	V
Digital I/O Forward Voltage	V_{OUT}	On pins 1, 2, 3, 4	14	V
Digital I/O Reverse Voltage	V_{ROUT}	On pins 1, 2, 3, 4	–14	V
Transmitting Coil Pins Forward Voltage	$V_{IN(TX)}$	On TXP, TXN	4	V
Transmitting Coil Pins Reverse Voltage	$V_{R(TX)}$	On TXP, TXN	–0.5	V
Receiving Coil Pins Forward Voltage	$V_{IN(RX)}$	On RX1N, RX1P, RX2N, RX2P	4	V
Receiving Coil Pins Reverse Voltage	$V_{R(RX)}$	On RX1N, RX1P, RX2N, RX2P	–0.5	V
Operating Ambient Temperature	T_A	P range	–40 to 160	°C
Maximum Junction Temperature	$T_{J(MAX)}$		175	°C
Storage Temperature	T_{STG}		–65 to 170	°C
ESD Rating (VCC, GND, pin-1, pin-2, pin-3, pin-4)	V_{ESD}	HBM testing per AEC-Q100	>4	kV
ESD Rating (all other pins)		HBM testing per AEC-Q100	>2	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Operating Characteristics section

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package on 4-layer PCB based on JEDEC standard JESD51-7	82	°C/W

[1] Additional thermal information available on the Allegro website.

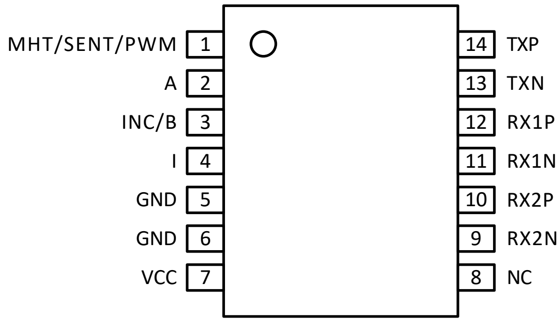
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table of Contents

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAMS AND TERMINAL LISTS

A17803PLEATR-M



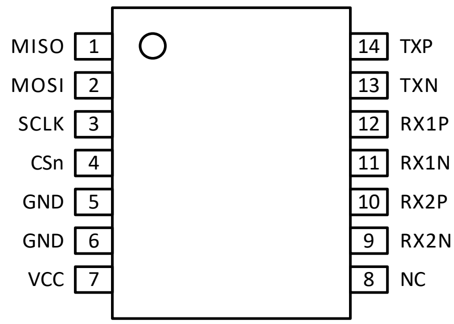
Package LE 14-pin TSSOP Pinout Drawing

Terminal List

Number	Name	Function
1	MHT/ SENT/ PWM	SENT/PWM output and Manchester communication
2	A	ABI protocol: “A“ signal
3	INC/B	motorSENT: Incremental output; ABI protocol: “B“ signal
4	I	ABI protocol: “I“ signal
5	GND	Ground
6	GND	Ground
7	VCC	Power supply
8	NC	Not connected Connect to ground in application
9	RX2N	Receiving coil 2 negative pin
10	RX2P	Receiving coil 2 positive pin
11	RX1N	Receiving coil 1 negative pin
12	RX1P	Receiving coil 1 positive pin
13	TXN	Transmitting coil negative pin
14	TXP	Transmitting coil positive pin

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

A17803PLEATR-S



Package LE 14-pin TSSOP Pinout Drawing

Terminal List Table

Number	Name	Function
1	MISO	SPI controller input/peripheral output
2	MOSI	SPI controller output/peripheral input
3	SCLK	SPI clock terminal input
4	CSn	SPI chip select terminal (active low input)
5	GND	Ground
6	GND	Ground
7	VCC	Power supply
8	NC	Not connected Connect to ground in application
9	RX2N	Receiving coil 2 negative pin
10	RX2P	Receiving coil 2 positive pin
11	RX1N	Receiving coil 1 negative pin
12	RX1P	Receiving coil 1 positive pin
13	TXN	Transmitting coil negative pin
14	TXP	Transmitting coil positive pin

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

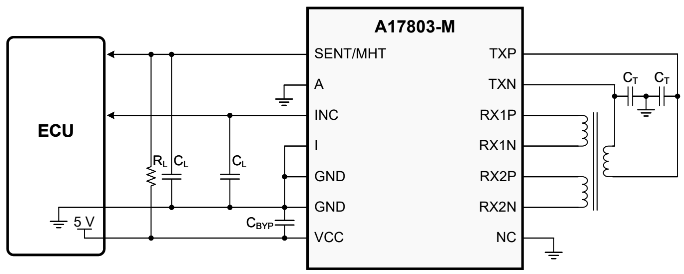


Figure 2: Typical A17803 configuration using motorSENT interface

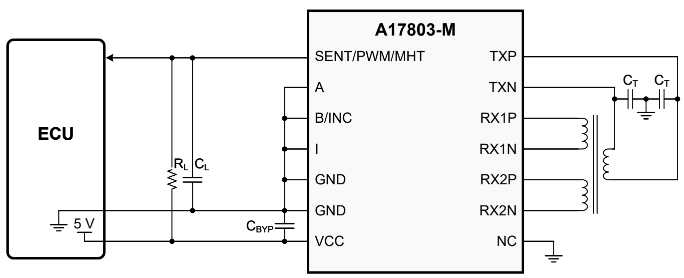


Figure 3: Typical A17803 configuration using SENT or PWM interface

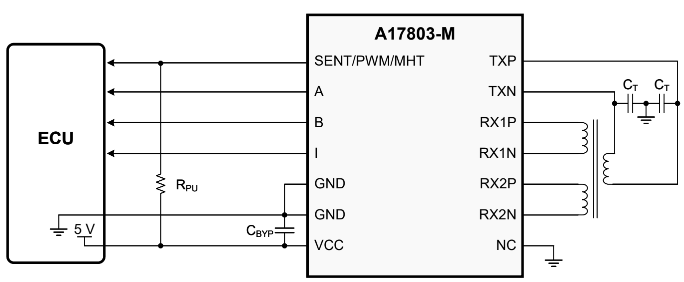


Figure 4: Typical A17803 configuration using ABI interface. Pin 1 should be connected for programming.

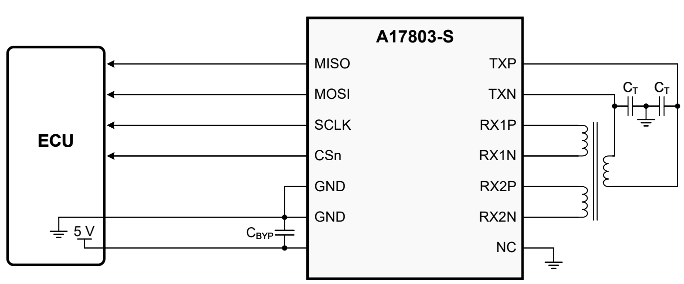


Figure 5: Typical A17803 configuration using SPI interface

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

CHARACTERISTIC PERFORMANCE

OPERATING CHARACTERISTICS: Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	A17803-M (SENT, PWM, motorSENT, and ABI outputs), without coils, load not present	–	–	23	mA
		A17803-S (SPI interface), without coils, load not present	–	–	20	mA
Transmitting Coil Tail Current	I_{TX}	DC equivalent current; over all temperature range; minimum for TXDRV_TRIM = 0 at –40°C; maximum for TXDRV_TRIM = 127 at 160°C; TX_TC = –2	0.047	–	14.95	mA
Undervoltage Flag Threshold [2]	$V_{UVD(HIGH)}$	V_{CC} rising	4	–	4.4	V
	$V_{UVD(LOW)}$	V_{CC} falling	3.9	–	4.3	V
Undervoltage Detection Hysteresis	$V_{UVD(HYS)}$		75	–	150	mV
Overvoltage Flag Threshold [2]	$V_{OVD(HIGH)}$	V_{CC} rising	5.5	–	5.9	V
	$V_{OVD(LOW)}$	V_{CC} falling	5.4	–	5.8	V
Overvoltage Detection Hysteresis	$V_{OVD(HYS)}$		75	–	150	mV
Power-On Time	t_{PO}	Time from $V_{CC} > V_{CC(min)}$ to valid angle information within specified accuracy	–	–	5	ms
TRANSMITTING COIL DRIVING CHARACTERISTICS [4]						
Transmitting Coil Driving Voltage [3]	$V_{TX,PP}$	Peak to peak voltage oscillation between TXP and TXN at f_{TX} frequency.	2	5	5.5	V_{PP}
Coil Driving Frequency [7]	f_{TX}	External LC tank resonant frequency	3	–	4	MHz
Transmitting Coil Inductance	L_{TX}	V_{TX} = 5 V_{PP}	1	–	8	µH
LC Tank Quality Factor	Q	V_{TX} = 5 V_{PP}; external LC tank quality factor over all temperature range.	10	–	–	–
f × Q × LTX product	f × Q × L_{TX}	V_{TX} = 5 V_{PP}; over temperature range	30	–	2080	µH
Equivalent Parallel Resistance	R_P	V_{TX} = 5 V_{PP}; over temperature range	189	–	13069	Ω
Input Signal Voltage [5]	$V_{RX,PP}$		10	–	200	mV_{PP}
Rotational electrical frequency	f_{IN}		–	–	4.16	kHz
Allowed Direct Coupling Amplitude [6]	O_X, O_Y		–10	–	10	mV

[1] Device operates normally up to max supply voltage, provided that V_{CC} has not risen above $V_{OVD(HIGH)}$. In the latter case V_{CC} must go below $V_{OVD(LOW)}$ to exit error condition.
[2] Full functional performance guaranteed within Supply voltage range. Safety limits guaranteed down to $V_{UVD(F)}$ min and up to $V_{OVD(R)}$ max by design.
[3] TX current trim TXDRV_TRIM should be programmed to have Transmitting Coil Driving Voltage within specified range.
[4] Parameter is not measured at final test. Determined by design.
[5] Full performance starting from 20 mV_{PP}; between 10 and 20 mV_{PP}, resolution and accuracy might be lower. Requires adjustment of D_TX_CK_PH_TRIM for correct operation.
[6] Direct coupling causes offset on signals after demodulation. Offset can be compensated using fixed offset compensation (OGT) and with IC offset autocalibration to improve sensor accuracy.
[7] Requires adjustment of D_TX_CK_PH_TRIM for correct operation across frequency range.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ANGLE CHARACTERISTICS						
Number of Angle Bits via SPI	N_{SPI}	Angle message length, SPI output	–	16	–	bits
Response Time [1][2]	$t_{RESPONSE}$	Angular latency	–	0	–	μs
Refresh Rate [3]	t_{ANG}	Angle update	–	1	–	μs
Angle Error [4]	ERR_{ANG}	Ideal input signals; measured in static condition (no latency effect on error) by reading angle register; value is ±3 sigma at 0-hour	–0.25	–	0.25	degrees
Lifetime Start-Up Error Drift [9]		Based on AEC-Q100 grade 0 qualification	–	–	0.15	degrees
Angle Noise [6]	N_{ANG}	Target RPM = 0; 1 sigma	–	0.006	–	degrees
Noise-Free Number of Bits on Angle [6][7]	b_{NOISE_FREE}	Target RPM = 0; 6 sigma	–	13	–	bits

[1] Parameter is not measured at final test. Determined by design.
[2] Response time is measured at the time between the target crossing a given angle and the angle value updating within the IC. No communication delay is considered.
[3] Rate at which a new angle reading is ready.
[4] Angle error and drift are inferred through channel characterization and signal path testing—not directly measured at final test. Error value can be decreased by using IC internal compensations with end-of-line calibration, and dynamic offset auto-calibration algorithm in continuous rotary applications.
[5] Value represents 3-sigma, or three times the standard deviation of the measured samples ($N_{ANG} = 3 \times \sigma$).
[6] Based on characterization data. Not measured at final test.
[7] Noise-free number of bits is defined as: $log_2\left(\frac{360}{6 \times \sigma}\right)$, where σ is the rms angle noise.
[8] Parameter is not measured at final test. Determined by design.
[9] Lifetime error drift can be compensated by dynamic offset auto-calibration algorithm in continuous rotary applications.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SPI GENERAL SPECIFICATIONS [1]						
Load Resistance	R_L		100	–	–	kΩ
Load Capacitance	C_L	Loading on digital output (MISO) pin with frequency up to 5 MHz	–	–	20	pF
SPI INTERFACE VOLTAGE SPECIFICATIONS [1]						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, CSn pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, CSn pins	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO pin, C_L = 20 pF, T_A = 25°C	4	5	5.5	V
Digital Output Low Voltage	V_{OL}	MISO pin, C_L = 20 pF, T_A = 25°C	–	0.3	0.5	V
SPI INTERFACE TIMING SPECIFICATIONS [1]						
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L ≤ 20 pF	0.1	–	5	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	f_{SPI}	SPI message is 32 bits	3	–	140	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from CSn going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time CSn must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge, C_L = 20 pF	–	30	–	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CSn Hold Time	t_{CHD}	Hold SCLK high time before CSn rising edge	5	–	–	ns

[1] Parameter is not measured at final test. Determined by design.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT ELECTRICAL SPECIFICATIONS						
Digital Output Low Saturation Voltage [1]	V_{SAT_LOW}	V_{CC} = 5 V, R_L=1.2 kΩ	–	–	0.35	V
Digital Output High Saturation Voltage [1]	V_{SAT_HIGH}	Push-pull; pull-up source voltage = 5 V	4.3	–	–	V
Output Load Resistance [1]	$R_{L(PULLUP)}$	Pull-up resistor; push-pull, or open-drain mode	1.2	–	55	kΩ
	$R_{L(PULLDOWN)}$	Pull-down resistor; push-pull mode only	10	–	–	kΩ
Pull-Up Source Voltage [1]	V_{S_PWM}	Maximum pull-up source for digital output operation, open-drain output	–	–	5.4	V
		Maximum pull-up source for digital output operation, push-pull mode (5.0 V digital)	4.5	5	5.4	V
Digital Output Leakage Current [1]	$I_{leakage}$	Leakage into pin, FET off, V_{OUT} ≤ 5.5 V	–	–	20	μA
Digital Max Operational Current [1]	$I_{MAX(SINK)}$	Maximum operating digital output sink current	–	–	20	mA
	$I_{MAX(SOURCE)}$	Maximum operating digital output source current	–	–	1	mA
Digital Output Short-Circuit Current Limiter [1]	$I_{SC(SINK)}$	Internally limited	15	–	30	mA
	$I_{SC(SOURCE)}$	Internally limited	10	–	25	mA
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [1]	f_{PWM}	PWM frequency minimum setting, T_A in specification	–	125	–	Hz
		PWM programmable options	–	16	–	steps
		PWM frequency maximum setting, T_A in specification	–	16	–	kHz
PWM Output Low Clamp [1]	$D_{PWM(MIN)}$	2% corresponds to PWM_PORCH_SEL set to 000_2 8% corresponds to PWM_PORCH_SEL set to 110_2	2	–	8	%
PWM Output High Clamp [1]	$D_{PWM(MAX)}$	92% corresponds to PWM_PORCH_SEL set to 110_2 98% corresponds to PWM_PORCH_SEL set to 000_2	92	–	98	%
PWM Output Clamp Step Size	$D_{PWM(step\_size)}$	PWM_PORCH_SEL EEPROM field	–	1	–	%

[1] Parameter is not measured at final test. Determined by design.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SENT SPECIFICATIONS [1]						
SENT Tick Time	t_{TICK}	Programmable; all SENT modes	0.25	–	10	µs
SENT Tick Time Tolerance	TOL_{tTICK}	All SENT Modes	–10	–	10	%
SENT Trigger Signal	$V_{SENTtrig(L)}$	SENT_HYST_CFG = 0, 2; falling edge threshold	1.48	–	1.79	V
	$V_{SENTtrig(H)}$	SENT_HYST_CFG = 0; rising edge threshold	2.21	–	2.49	V
		SENT_HYST_CFG = 2; rising edge threshold	1.92	–	2.19	V
SENT Trigger Threshold Hysteresis	$V_{SENTtrig(HYST)}$	SENT_HYST_CFG = 0	–	0.73	–	V
		SENT_HYST_CFG = 2	–	0.44	–	V
Minimum SENT Trigger Time	$t_{trig(MIN)}$	TRIGGER_CFG = 0	–	2.5	–	µs
		TRIGGER_CFG = 1	–	5	–	µs
		TRIGGER_CFG = 2	–	10	–	µs
		TRIGGER_CFG = 3	–	0.5	–	µs
SENT Output Trigger Edge Filter	$t_{SENTtrig(f)}$	Deglitch filter	–	0.75	–	µs
SENT Trigger Delay Time	T_{dSENT}	Delay from end of trigger pulse to beginning of SENT message frame (for TSENT and shared SENT)	7	–	–	ticks
MOTORSENT INCREMENTAL INTERFACE CHARACTERISTICS [1]						
Pulse Width (Pulse Mode) [1]	T_{PULSE}	Programmable [2]	0.062	–	3	µs
Minimum T_{PULSE} (Pulse Mode) [1]		C_L = 1 nF; R_L= 4.7 kΩ	–	1	–	µs
		C_L = 4.7 nF; R_L= 4.7 kΩ	–	2	–	µs
Maximum output Frequency [1] (Edge Mode)	MAX_f_{INC}	C_L = 1 nF; R_L= 4.7 kΩ	–	500	–	kHz
		C_L = 4.7 nF; R_L= 4.7 kΩ	–	250	–	kHz
Incremental Step [1]	Δθ	Programmable [2]	0.0055	–	180	degrees

[1] Parameter is not measured at final test. Determined by design.
[2] Selected incremental step with RC load determines the maximum supported target speed for the protocol.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The A17803 is an interface IC for position sensors based on electromagnetic induction principle.

The sensing element is constituted by a transmitting coil and two receiving coils, connected to the IC, and a rotating metallic target.

When operating, the IC sustains oscillations in the transmitting coil that is appropriately connected with external capacitors to form an LC tank. The transmitted signal induces eddy currents in the target, which conversely generate an electromagnetic field that induces an electromotive force in the receiving coils. With an appropriate design of the coils and target system, the received signals amplitude is modulated by the target position and the modulation terms of the two received signals are in quadrature, as depicted in Figure 6.

The received signals can be approximately described by the following equations:

$$v_{RX1} = V_Y(\sin(\theta_e) + H_Y(\theta))\sin(2\pi f_{TX}t + \phi) + O_Y\sin(2\pi f_{TX}t)$$

$$v_{RX2} = V_X(\cos(\theta_e) + H_X(\theta))\sin(2\pi f_{TX}t + \phi) + O_X\sin(2\pi f_{TX}t)$$

where:

V_Y, V_X are the peak-to-peak value of target position modulation of input signals,

O_Y, O_X are the direct coupling amplitude,

f_{TX} is the carrier frequency corresponding to the transmitted signal frequency,

t is the time,

ϕ is the phase shift between transmitted signal and target reflected signal,

H_X, H_Y represent all residual distortion terms,

θ is the absolute mechanical position of the target, and

θ_e is the electrical position of the target.

The electrical position and the mechanical position are linked by the number of periods (or teeth) present in the target-receiving coil system:

$$\theta_e = \mathrm{mod}(N\times\theta, 360°)$$

where mod is the modulo function.

The A17803 demodulates the received signals v_{RX1} and v_{RX2} and condition them digitally to accurately extract and output the electrical angle information θ_e.

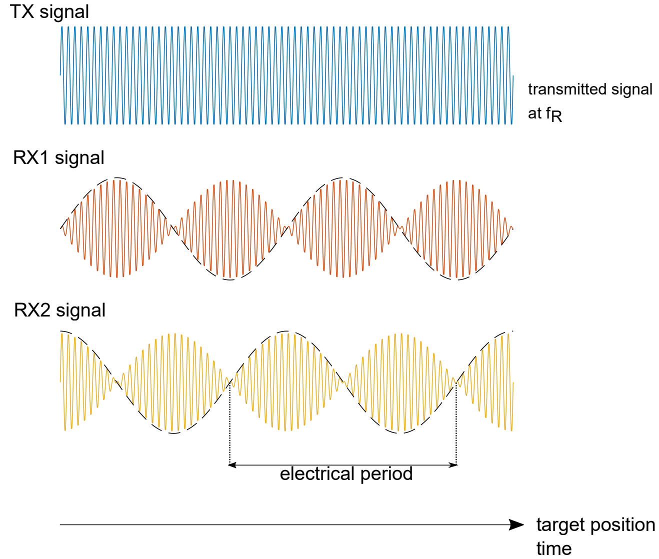


Figure 6: Transmitted and received signals

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Coils and Target Design

The transmitting coil constitutes the inductive part of the external LC tank that must be connected to the IC. The target shape and receiving coil system is chosen depending on the applications to have a single or multiple electrical periods over a single mechanical rotation.

Each receiving coil is composed of at least two loops connected to have the current oriented clockwise (CW) in one loop and counterclockwise (CCW) in the second one in order to cancel the total magnetic flux not reflected by the target. The SIN and COS coils are arranged to have a 90° electrical shift distance between them. The transmitting coil encompasses the set of receiving coils.

For rotary applications, a basic design for the receiving coil loops can be obtained with the following equations in polar coordinate system:

$$R(\theta) = Rin + A\,(1 + \cos(N\theta + \phi))$$

where N is the number of periods, θ is the mechanical angle, and ϕ is the mechanical phase shift. The minimum number of four loops can be obtained by choosing ϕ = 0°, 180° for COS, and ϕ = 90°, 270° for SIN.

The target is designed to match the receiving coils in terms of number of periods and its teeth should extend over the transmitting coil radius.

The number of windings for the coils and the size of coils must be designed according to the application conditions, such as target material and target-to-coils distance, to match the IC operating conditions for the voltage levels of the inputs.

Conceptual layouts for rotary sensor with one and four electrical periods are shown in Figure 7 and Figure 8.

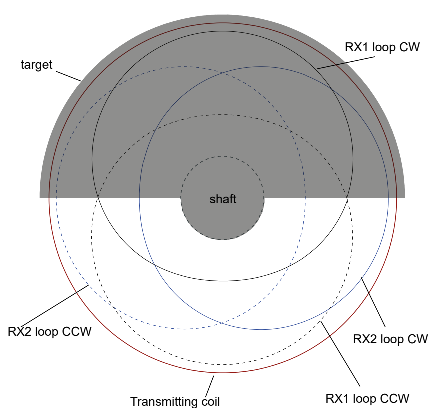


Figure 7: Coil and target design for 1 electrical period

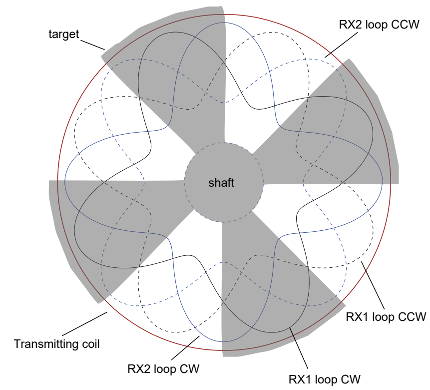


Figure 8: Coil and target design for 4 electrical periods

LC Oscillator

The A17803 integrates an oscillator driver that sustains transmitted signal oscillation in the external LC tank.

The inductance value L_{TX} is the transmitting coil inductance at the specified frequency range and with the target placed in front of the coils system. The value of the shunt capacitances C_T in application circuit is chosen in combination with L_{TX} to have a resonant frequency f_{TX} within the range specified in Operating Characteristics:

$$f_R = \frac{1}{2\pi\sqrt{L_{TX}\frac{C_T}{2}}}$$

$$C_T = \frac{2}{(2\pi f_R)^2 L_{TX}}$$

The LC tank oscillator has non-zero losses due to coil parasitic resistance and electromagnetic interaction with the target. The losses can be represented with an equivalent parallel resistor to the LC tank as in Figure 9.

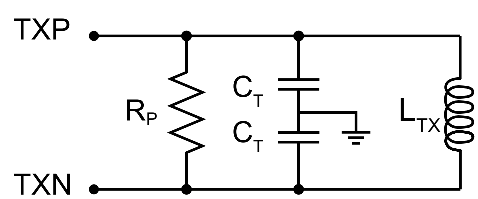


Figure 9: LC tank equivalent circuit. R_P represents losses.

The value of the equivalent parallel resistance is related to the

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

quality factor Q of the circuit with the relation:

$$Q = \frac{R_P}{2\pi f_R L_{TX}}$$

The Q-factor should be evaluated by considering resistive and electromagnetic losses in the coil and in the target in application conditions and must be within the specified range.

The LC-oscillator driver works by injecting a controlled current in the external LC circuit determined by the current trim code in EEPROM field TXDRV_TRIM (see EEPROM section). Given a certain transmitting current value, the corresponding transmitting voltage peak amplitude at the resonant frequency is approximately expressed by the equation:

$$V_{TX} = I_{TX}\, R_P\, \sin(2\pi f_{TX} t)$$

where R_P is the equivalent parallel resistor of the LC tank.

The transmitting current is adjusted with the sensed temperature to limit transmitting voltage variation over temperature due to changes in coil resistivity and losses.

The transmitting current amplitude at each temperature T is approximately given by the equation:

$$I_{TX} = I_{TX,25°C}(1 + \mathrm{TC_{TX}} \times (T - 25\ °\mathrm{C}))$$

where $I_{TX,25°C}$ is the nominal current and TC_{TX} is a temperature coefficient determined by EEPROM field D_TX_TC.

For typical operations D_TX_TC is set to code 14 (default EEPROM value), corresponding to a coefficient nominal value of $2.82 \times 10^{-3}\ °C^{-1}$.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FRONT-END CONFIGURATION

Automatic Gain Selection

The A17803 integrates a power-on automatic gain selection (AGS) to amplify the received signals before the analog-to-digital conversion and improve the overall angle calculation accuracy. The optimal gain value is determined after each device repower. Gain does not change during a power cycle.

AGS can be disabled by setting field AGS_EN to 0; in this case, the front-end gain is determined by the value programmed in FE_SENS_TRIM EEPROM field.

Input Phase Delay Compensation (Steel Target Compensation)

The A17803 integrates a compensation of the phase delay between TX and RX signals in demodulation scheme to maximize the demodulated signal amplitude.

The phase compensation value can be adjusted by modifying memory field D_TX_CK_PH_TRIM[3:0].

DIGITAL COMPENSATIONS

The A17803 integrates several digital compensations on input signals Y (RX1) and X (RX2) to improve output angle accuracy.

Offset and Gain Trimming (OGT)

Post-demodulation offset due to cw and ccw loop imbalances in sensor coil can be digitally removed by programming fields OGT_X_OFFSET_C and OGT_Y_OFFSET_C.

The amplitude mismatch between the two channels can be corrected by programming gain fields OGT_X_GAIN_C and OGT_Y_GAIN_C.

Electrical Harmonic Compensation (EHC)

The A17803 integrates the possibility of digitally compensating for the higher electrical harmonic due to sensor design.

By programming EEPROM fields X_H(i)_AMP, X_H(i)_PHASE, Y_H(i)_AMP, Y_H(i)_PHASE, where (i) = 2,3,4; the 2nd, 3rd, and 4th electrical harmonics can be digitally removed from input x and y signals.

To do so, the A17803 calculates each harmonic component using the programmed fields and calculated angle:

$$Y\_H(i) = Y\_H(i)\_AMP \times \sin(i \times \theta_e + Y\_H(i)\_PHASE)$$

$$X\_H(i) = X\_H(i)\_AMP \times \sin(i \times \theta_e + X\_H(i)\_PHASE),$$
where i = 2 , 3, or 4.

The harmonic components are removed from the signals prior to angle calculation.

Offset Autocalibration

During operation a dynamic offset autocalibration algorithm tracks the signals after electrical harmonic compensation and remove residual offset after static trimming.

The algorithm tracks all maxima and minima over a number of electrical periods determined by the EEPROM field N_AVG_CYCLES_OGA and then calculates a correction offset to be applied to the x and y signals. For optimal operation N_AVG_CYCLES_OGA is typically matched to the largest multiple ≤16 of the number of electrical period over a full mechanical rotation of the target.

For the algorithm to operate correctly, residual offset after OGT and EHC trim should always be smaller than half the amplitude of the corresponding X and Y signals after OGT over the mechanical period.

Quadrature Compensation

The A17803 offers the possibility of removing quadrature error up to ±11.25° between the demodulated input signals by programming EEPROM field QUADRATURE_COMP.

Latency Compensation (Synchronization Compensation)

The A17803 integrates a delay compensation mechanism to reduce the effective path latency of the IC.

An optional compensation for external delays up to ±256 µs is available for customer by programming field DEL_SYS_ABS.

Angle Reference and Rotation Direction

The A17803 offers the possibility of programming a zero degrees angle reference position (EEPROM field DEL_ZERO_ANGLE). Signals rotation direction for output angle signals with respect to input signals can be inverted by setting EEPROM field DEL_ANGLE_POL.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OUTPUT PROTOCOLS

Protocol Selection

The A17803 is available in two versions:

- A17803-S: SPI interface
- A17803-M: Manchester interface

In the SPI version, the device is programmed and used through the SPI interface as described in the Device Programming Interfaces section.

In the Manchester version, the device is programmed through the Manchester interface as described in Device Programming Interfaces section. The A17803-M device is used with one the available output protocols for Manchester devices:

- Pulse-width modulated (PWM) output
- Single edge nibble transmission encoding scheme (SENT, SAEJ2716)
- motorSENT
- Incremental ABI protocol

Table 1 indicates how to program EEPROM to activate a specific protocol.

Table 1: Activating Device Programming Protocols

Device	Output	EEPROM Programming
A17803-S	SPI	–
A17803-M	PWM (pin 1)	PIN1_ PWM1_SENT0 = 1
	SENT (pin 1)	PIN1_ PWM1_SENT0 = 0
	motorSENT (SENT on pin 1, incremental line on pin 3)	PIN1_ PWM1_SENT0 = 0 DIG_OUT_MODE_C = 3 INC_ENABLE = 1
	ABI	DIG_OUT_MODE_C = 0

In addition to these configurations, it is also possible to activate PWM or SENT output on pin 2 by programming DIG_OUTPUT_MODE_C to values 1 or 2.

Table 2: Activating PWM or SENT Protocols

DIG_OUTPUT_MODE_C	Description
0	ABI enabled
1	PWM enabled on pin 2
2	SENT enabled on pin 2
3	No output on pin 2

For motorSENT, incremental output is enabled (INC_ENABLE = 1) and ABI is not enabled (DIG_OUT_MODE_C should not be 0).

Open-Drain and Push-Pull Configurations

When using ABI or motorSENT, incremental protocol corresponding output pins are configured as push-pull output.

For PWM and standard SENT on pin 1 or pin 2, the output mode can be reconfigured by using EEPROM fields PIN1_PUSHPULL_EN and PIN2_PUSHPULL_EN for pin 2 to be in open-drain (0) or push-pull mode (1).

In the case of trigger SENT and shared SENT protocols (SSENT, ASENT), when push-pull mode is configured, the corresponding pin toggles its behavior between open-drain high-impedance configuration when waiting for trigger to push-pull when transmitting a frame.

PWM Output

The A17803 provides a pulse-width-modulated output with a duty cycle proportional to the measured angle. The PWM frame consists of fixed low and high times as well as the linear region (or active period) used to communicate angle data.

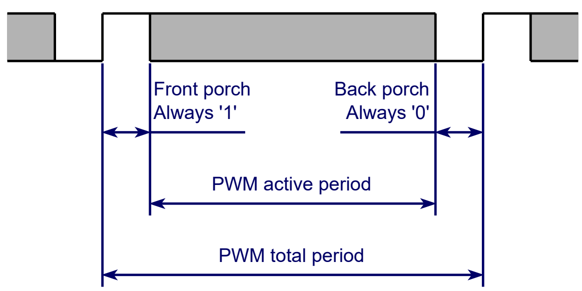


Figure 10: PWM Frame

PWM Carrier Frequency

The PWM carrier frequency is controlled by the PWM_PERIOD EEPROM field. Table 3 indicates corresponding frequency and maximum angle resolution for each code.

Table 3: Frequency and Maximum Angle Resolution

PWM_PERIOD	PWM Frequency (Hz)	Resolution Bits
0	125.0	15
1	166.7	15
2	250.0	14
3	333.3	14
4	500.0	13
5	666.7	13
6	800.0	13
7	1000.0	12
8	1333.3	12
9	1600.0	12
10	2000.0	11
11	2666.7	11
12	4000.0	10
13	5333.3	10
14	8000.0	9
15	16000.0	8

Fixed High and Low Times

The fixed high and low times of the PWM frame are configurable via the EEPROM PWM_PORCH_SEL field. The times are always applied symmetrically, such that a setting of 0 results in a duty cycle range of 2% to 98% (guaranteed 2% for the low and high porch sections).

Table 4

PWM_PORCH_SEL	Fixed Time (% Duty Cycle) (Fixed Time = Front Porch and Back Porch)
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	2

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SENT INTERFACE

SENT Output

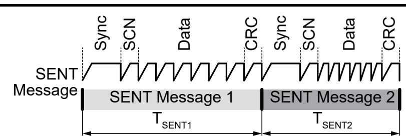
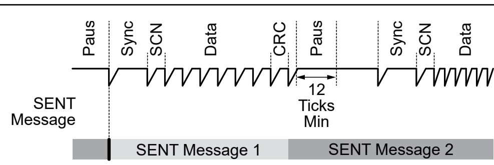
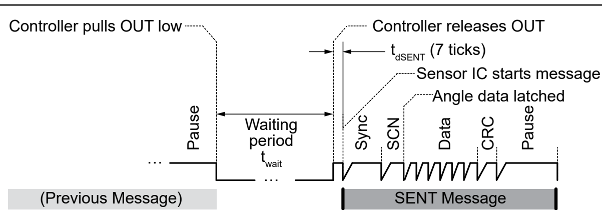
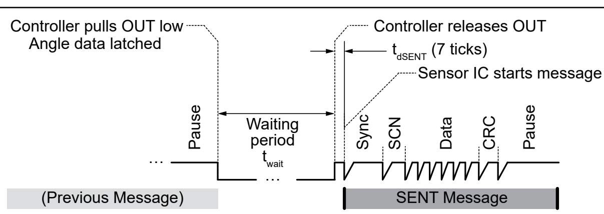
The A17803 features a SENT output conforming to the SENT data transmission specification SAEJ716 JAN2016 and features for enhanced SENT modes beyond the industry standard. The enhanced modes offer greater flexibility for application use.

The timing and method of SENT transmission may be configured using the OUTMSG_MODE field within EEPROM. Methods of SENT transmission are shown in Table 5 and SENT output modes are shown in Table 6.

Table 5: Methods of SENT Transmission

Free-Streaming SENT	Angle information is automatically placed on the SENT line with no prompting from the host. Depending on settings, the SENT message frames may be transmitted back-to-back or synchronized with the angle update. OUTMSG_MODE = 0 and 1 are examples of free-streaming SENT.
Triggered SENT (TSENT)	A SENT message frame occurs only when initiated by the host. Prior to the trigger, the A17803 outputs a continuous pause pulse, during which the host triggers a SENT frame by pulling the SENT line low for a minimum of $T_{Trig(MIN)}$. Once the SENT line is released by the host, the A17803 responds with a SENT message frame. OUTMSG_MODE = 2 and 6 are examples of triggered SENT.
Shared SENT	Two distinct formats—sequential SENT (SSENT) and addressable SENT (ASENT). Shared SENT allows sharing a single SENT line among four compatible devices. OUTMSG_MODE = 3, 4, and 5 are examples of shared SENT.

Table 6: SENT Output Modes (OUTMSG_MODE EEPROM Field)

Code	Visual	Description
0		• Free-streaming SENT. No pause pulse.
1		• Free-streaming SENT synchronized to the angle update. • A pause pulse is inserted between frames. The pause pulse has a minimum length of 12 ticks between SENT messages. • Angle data is sampled near the end of the status and communication nibble (SCN).
2		• Triggered SENT (TSENT). • Data is latched near the end of SCN. • Controller initiates a SENT transmission by pulling the line low during the pause pulse. After the controller releases the output, and after a delay of t_{dSENT}, the SENT message begins.
3	–	• Sequential SENT—Long. • See Shared SENT section.
4	–	• Sequential SENT. • See Shared SENT section.
5	–	• Addressable SENT (ASENT). • See Shared SENT section.
6		• TSENT. • Data is latched on the falling edge of the trigger. • Similar to OUTMSG_MODE = 2, except angle data is latched once the output line is pulled low.
7	–	• Same as OUTMSG_MODE = 0. • Free-streaming SENT. No pause pulse.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Message Structure

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at five ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the rising and falling edge may be adjusted using the rise time and fall time control parameters in EEPROM register 0x10.

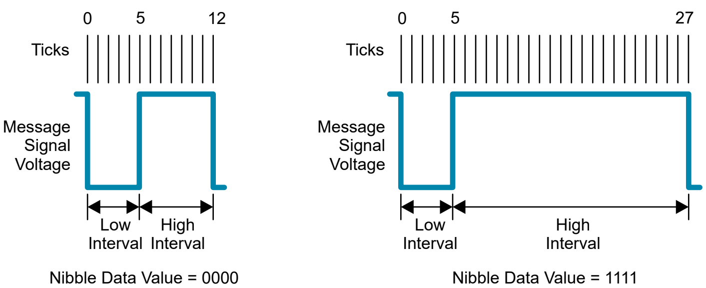


Figure 11: General Value Formation for SENT 0000 (left), 1111 (right)

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_RATE EEPROM field. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence:

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides the status of the A17803 and the optional serial data determined by the setting of the SENT_SCN_CFG parameter.
3. **Data:** Angle information and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

Table 7: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

SENT_ RATE	Tick Time (µs)
0	1
1	0.25
2	0.375
3	0.5
4	0.625
5	0.75
6	0.875
7	1.0
8	1.125
9	1.25
10	1.375

SENT_ RATE	Tick Time (µs)
11	1.5
12	1.625
13	1.75
14	1.875
15	2.0
16	2.125
17	2.25
18	2.375
19	2.5
20	2.625
21	2.75

SENT_ RATE	Tick Time (µs)
22	2.875
23	3.0
24	3.5
25	4.0
26	4.5
27	5.0
28	5.5
29	6.0
30	7.0
31	10.0

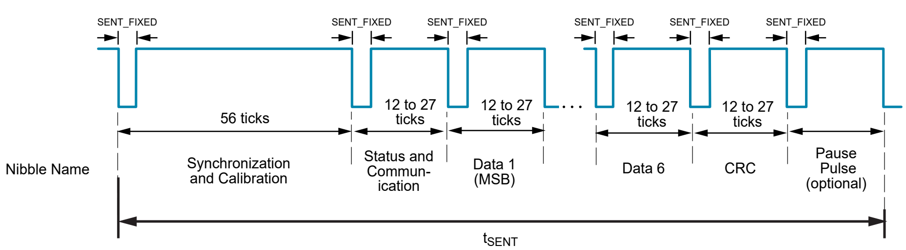


Figure 12: General Format for SENT Message Frame

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SENT Synchronization and Calibration Pulse

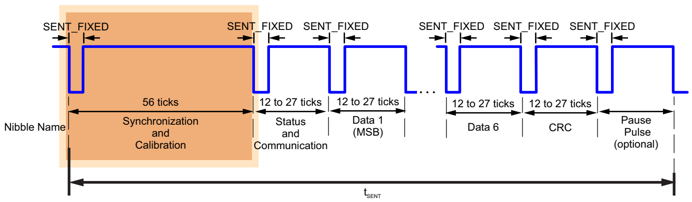


Figure 13: Synchronization and Calibration Pulse in SENT Message

The Synchronization and Calibration pulse is 56 ticks wide, measured from falling-edge to falling edge and delineates the start of a new message frame. The host microcontroller uses this pulse to rescale the subsequent nibble values to correct for clock variation between the controller and the A17803.

SENT Status and Communication Nibble

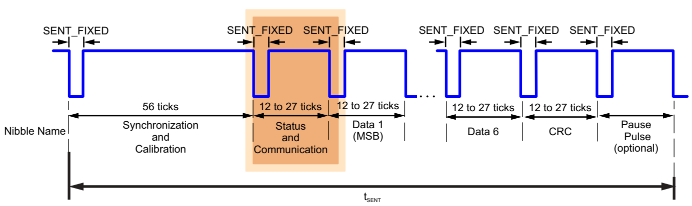


Figure 14: SENT SCN Nibble

The Status and Communication Nibble (SCN) provides diagnostic information along with optional other data from the short serial message. Nibble contents are controlled via the SENT_SCN_MODE field within EEPROM (See Table 8).

By default, contents of the SCN are not included in the 4-bit CRC at the end of each SENT frame. The SENT_CRC_MODE bit within EEPROM enables CRC coverage of the SCN contents. It should be noted that this option is not specified in the SAE J2716 SENT standard.

Table 8: Status and Communication Nibble (SCN) modes

SENT SCN Mode	SCN Nibble Bit			
	Bit 3	Bit 2	Bit 1	Bit 0
0	Serial Sync	Serial Data	S1	S0
1	0	0	S1	S0
2	ID[1]	ID[2]	S1	S0
3	0	0	0	0

The SCN has two different types of bit values which may be present, depending on the SENT_SCN_MODE setting: Fault Flag and Serial Data.

Fault Flag

Fault flags are one-bit representations of an OR logic operation on of all diagnostics faults. Further investigation of which diagnostic fault has occurred requires reading out the diagnostic register or utilizing the serial data messages (if the option is selected). Diagnostic flags are cleared when loaded by the Short Serial Message or individually when transmitted by the Error and Status Code message in the Enhanced Serial Message. In SCN configurations where there is no serial message transmitted, all diagnostic flags are cleared after transmission of a standard SENT frame.

Note that multi-bit EEPROM fault triggers high-impedance output state.

Serial Data

Two data bits consisting of the Serial Sync and Serial Data bits. Together they form the Short Serial Message (per SAE J2716 Section 5.2.4.1).

Optional Slow Serial Mode

The A17803 SENT output supports an optional mode to transmit additional data with the Slow Serial Mode. It enables transmission of additional data by encoding information in the Status and Communication nibbles.

The serial message format can be programmed to follow the Short Serial Message Format (16-bit) or the Enhanced Serial Message Format (18-bit) via the SENT_EMSG_SMSG_N bit within EEPROM (0: Short serial message, 1: Enhanced serial message). For the serial message to be enabled SENT_CRC_CFG should be set to 0.

Short Serial Message Format

For the Short Serial Message, a 16-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 16-bit packet is indicated by a 1 in the Serial Sync bit. The message data is transmitted bit-by-bit via the Serial Data bit. See Table 9 for more information regarding the format.

Table 9: SCN Nibble Short Serial Message Format

Serial Bit	SENT Frame															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SerialSync	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SerialData	MessageID				Data [7:0]								CRC			

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 10: SCN Short Serial Message Output Data

Message Order	Message ID	8-bit Data (MSB→LSB)
0	$0	Diagnostic Error Code [3:0] + Temperature [15:12]
1	$1	Temperature [11:4]
2	$2	Customer Sensor ID #1 [11:4]
3	$3	Customer Sensor ID #1 [3:0] + Customer Sensor ID #2 [11:8]
4	$4	Customer Sensor ID #2 [7:0]
5	$5	Customer Sensor ID #3 [11:4]
6	$6	Customer Sensor ID #3 [3:0] + Customer Sensor ID #4 [11:8]
7	$7	Customer Sensor ID #4 [7:0]

Customer Sensor ID can be programmed in EEPROM at addresses 0x19 and 0x1A.

Definitions for the Diagnostic Error Code are given in Table 11.

Table 11: Diagnostic Error Codes

Diagnostic Error Code (hex)	Error flag
1	EUE
2	SME
3	VCC
4	VCF
5	OFE
6	TSE
7	TDE
8	ICA
9	SPD
A	SAT
B	SPE
C	POR

Enhanced Serial Message Format

For the Enhanced Serial Message Format, an 18-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 18-bit packet is indicated by a series of six consecutive 1's in the Serial Sync bit. Bit numbers 7, 13, and 18 of the Serial Sync bit are always 0. The message data is transmitted bit-by-bit via the Serial Data and Serial Sync bits. See Table 12 for more information regarding the format. Following a reset, the first message transmitted is 0, following in order of the message ID until the final message, at which point the messages are repeated. The CRC field is calculated for the Message ID, the Data field and 0 bits 7, 8, 13 and 18 by using the polynomial $x^6 + x^4 + x^3 + x$, initialized to 010101. For purposes of the CRC calculation, the bits order is indicated in Table 13. Message order, ID and corresponding data content for Short Serial Message are reported in Table 14.

Table 12: SCN Nibble Enhanced Serial Message Format

Serial Bit	SENT Frame																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SerialSync	1	1	1	1	1	1	0	0	Message ID [7:4]				0	Message ID [3:0]				0
SerialData	CRC						Data [11:0]											

Table 13: Enhanced Serial Message Format – CRC Message Order

Frame	Bit	Order
7	Serial Data	0
	Serial Sync	1
8	Serial Data	2
	Serial Sync	3
9	Serial Data	4
	Serial Sync	5
…	…	…
18	Serial Data	22
	Serial Sync	23

Table 14: SCN Enhanced Serial Message Output Data

Message Order	Message ID	12-bit Data (MSB→LSB)
0	$01	Diagnostic Error Code [3:0], repeated 3 times
1	$03	Channel 1 / 2 Sensor type
2	$05	Manufacturer code [1]
3	$06	Protocol standard revision ($04)
4	$23	Temperature [11:0]
5	$29	Customer Sensor ID #1 [11:0]
6	$2A	Customer Sensor ID #2 [11:0]
7	$2B	Customer Sensor ID #3 [11:0]
8	$2C	Customer Sensor ID #4 [11:0]

[1] The Manufacturer Code is determined by the MANUFACTURE_CODE field in EEPROM.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SENT Data Nibble

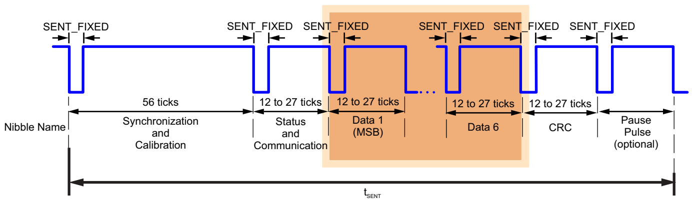


Figure 15: SENT Data Nibble

The A17803 SENT output supports options for the message data nibble format. The data nibble format is determined by the EEPROM parameter SENT_DATA_CFG. The options for either a minimum 3 or maximum 6 nibbles of data are defined in Table 15.

Where:

- ANGLE_OUT: [15:4] 12-bit, [15:0] 16-bit, angle digital output data.
- Y_EHC, X_EHC: [15:0] 16-bit signed digital channel values after compensations.
- SENT_FRAME_COUNT: [3:0] 4-bit SENT frame count. The counter increments once for every frame that is sent up to the maximum count. At the next count, after the maximum, the counter starts again at 0.
- TEMP_OUT: [15:4] 12-bit, [15:8] 8-bit signed output from the internal temperature sensor. Ambient temperature (°C) = 12-bit signed temperature value / 8 (LSB / °C) + 25.
- SPEED: [15:8] first 8-bits of speed register representing angular velocity in 16-bit signed integer.
- DIAGNOSTIC ERROR CODE: [3:0] as described in in Table 15.

Table 15: SENT Data Nibble Options

SENT_DATA_CFG	Data Nibble #1	Data Nibble #2	Data Nibble #3	Data Nibble #4	Data Nibble #5	Data Nibble #6	# of Nibbles	Sensor Type
0	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	ANGLE_OUT[3:0]	NA	NA	4	$66
1	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	NA	NA	NA	3	$67
2	ANGLE_OUT[15:13] (MSB=0)	ANGLE_OUT[12:10] (MSB=0)	ANGLE_OUT[9:7] (MSB=0)	ANGLE_OUT[6:4] (MSB=0)	NA	NA	3	$67
3 [1]	Y_EHC[15:12]	Y_EHC[11:8]	Y_EHC[7:4]	Y_EHC[3:0]	SENT_FRAME_ COUNT[3:0]	NA	6	$69
	X_EHC[15:12]	X_EHC[11:8]	X_EHC[7:4]	X_EHC[3:0]				
4	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	ANGLE_OUT[3:0]	SPEED[15:12]	SPEED[11:8]	6	$6A
5	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	ANGLE_OUT[3:0]	TEMP_OUT[15:12]	TEMP_OUT[11:8]	6	$6B
6	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	TEMP_OUT[15:12]	TEMP_OUT[11:8]	SENT_FRAME_ COUNT[3:0]	6	$6B
7	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	DIAGNOSTIC ERROR CODE [3:0]	NA	NA	4	$6D
8	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	DIAGNOSTIC ERROR CODE [3:0]	TEMP_OUT[15:12]	TEMP_OUT[11:8]	6	$6E
9	ANGLE_OUT[15:12] [2]	ANGLE_OUT[11:8] [2]	ANGLE_OUT[7:4] [2]	NA	NA	NA	3	$67
10	ANGLE_OUT[15:12] [2]	ANGLE_OUT[11:8] [2]	ANGLE_OUT[7:4] [2]	DIAGNOSTIC ERROR CODE [3:0]	NA	NA	4	$6D
11	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	TEMP_OUT[15:12]	TEMP_OUT[11:8]	TEMP_OUT[7:4]	6	$6B
12	ANGLE_OUT[15:12]	ANGLE_OUT[11:8]	ANGLE_OUT[7:4]	SENT_FRAME_ COUNT[7:4]	SENT_FRAME_ COUNT[3:0]	INVERSE OF DATA NIBBLE 1 (15-NIBBLE1)	6	$68
13	Reserved							
14	Reserved							
15	Reserved							

[1] Y_EHC and X_EHC are alternated in the SENT Data Nibbles: Y_EHC is transmitted in odd frames and X_EHC in even frames.

[2] In configuration 9 and 10, in case of error flags reporting, ANGLE_OUT nibbles are set to all ones (FFF). To distinguish error reporting state from normal operation values all zeros and all ones values are skipped in sent transmission in normal operation: when internal ANGLE_OUT[7:4] value is 0, sent data nibbles are set to 001, when internal value is FFF , data nibbles are set to FFE.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SENT CRC Nibble

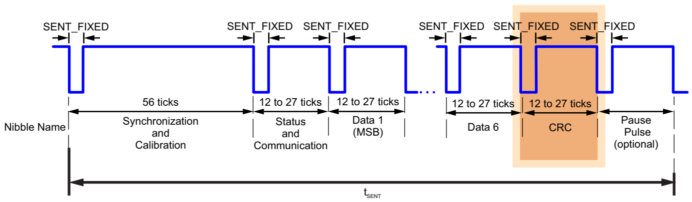


Figure 16: CRC Nibble in SENT message

The CRC nibble is a 4-bit error checking code, implemented per the SAE J2716 SENT recommended specification.

The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$, initialized to 0101.

By default, the checksum covers only the contents of the data nibbles (3-6 nibbles). The SCN nibble can be included into the CRC calculation by setting SENT_CRC_CFG to 1.

SENT Pause Pulse

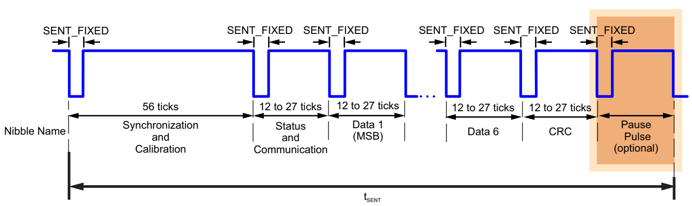


Figure 17: SENT Pause Pulse

The SENT Pause Pulse is an optional addition to the SENT message frame, transmitted following the CRC nibble. It acts to fill-in the frame until the beginning of the next SENT transmission in order to have constant output rate. The inserted Pause Pulse is a minimum of 12 ticks in length.

The frame duration is calculated by the following equation:

$$TICK_{FRAME} = TICK_{SYNC(MAX)} + TICK_{SCN(MAX)} + TICK_{DATA(MAX)} + TICK_{CRC(MAX)} + TICK_{PAUSE(MIN)}$$

$$TICK_{FRAME} = 56 + 27 + (27 \times N_{DATA}) + 25 + 12 = 120 + (27 \times N_{DATA})$$

where N is the number of data nibbles in the frame.

TSENT

When SENT is configured for Free Running Mode with no Pause Pulse (OUTMSG_MODE = 0, 7), or Free Running Mode with Variable Pause Pulse (OUTMSG_MODE = 1), the SENT output transmits continuously while in normal operating condition. The output data is latched at the falling edge of SCN Nibble (Internal Synchronous Mode).

When configured for External Trigger Mode, OUTMSG_MODE = 2, 6, the SENT output transmits when requested by the external controller. The pause pulse is extended until the next trigger pulse; see Figure 18 and Figure 19.

The external controller initiates a trigger pulse by holding the output pin low. The minimum duration of the trigger pulse is set by the parameter TRIGGER_CFG; see Table 16. The SENT frame is transmitted when the external controller releases the output, the rising edge of the trigger pulse. After the rising edge of the trigger pulse, the output remains high for a minimum of seven SENT tick times before going low to initiate the start of the SENT synchronization pulse.

For TSENT Synchronous Mode, OUTMSG_MODE = 6, the data sample is latched at the falling edge of the trigger pulse. For TSENT Asynchronous Mode, OUTMSG_MODE = 2, the data sample is latched at end of the SCN nibble.

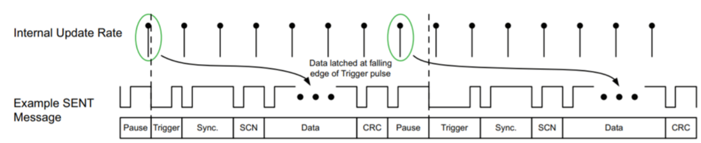


Figure 18: TSENT Data Synchronization and External Trigger Synchronous Mode

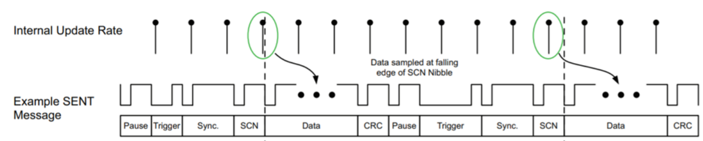


Figure 19: TSENT Data Synchronization and External Trigger Asynchronous Mode

Table 16: Diagnostic Error Codes

TRIGGER_CFG	Duration
0	2.5 µs
1	5 µs
2	10 µs
3	0.5 µs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 17: Trigger SENT Characteristics

Parameter [1]	Symbol	Test Conditions	Min	Typ	Max	Unit
Trigger Signal Falling Edge Threshold	$V_{SENTtrig(L)}$	SENT_HYST_CFG = 0, 2	1.38	–	1.89	V
		SENT_HYST_CFG = 1, 3	0.87	–	1.28	V
Trigger Signal Falling Rising Threshold	$V_{SENTtrig(H)}$	SENT_HYST_CFG = 0, 1	2.07	–	2.58	V
		SENT_HYST_CFG = 2, 3	1.84	–	2.22	V
SENT Trigger Threshold Hysteresis	$V_{SENTtrig(HYST)}$	SENT_HYST_CFG = 0	0.51	–	0.87	V
		SENT_HYST_CFG = 1	1	–	1.5	V
		SENT_HYST_CFG = 2	0.21	–	0.6	V
		SENT_HYST_CFG = 3	0.74	–	1.19	V
SENT Output Trigger Edge Filter	$V_{SENTtrig(f)}$		–	0.35	–	µs
SENT Trigger Delay Time	T_{dSENT}	Delay from end of trigger pulse to beginning of SENT	7			ticks

[1] Parameter value is not guaranteed at final test. Determined by design.

SSENT ADDRESSING PROTOCOL

The SSENT protocol requires sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by SensorID starting with SensorID 0. The slot for a sensor is the time at which that sensor is expected to respond to an AddressingPulse and other sensors are expected not to respond.

Each sensor independently maintains a SlotCounter that is incremented each time the sensor detects an AddressingPulse of either an F_OUTPUT or F_SAMPLE pulse. This SlotCounter becomes the SlotNumber, which is used by the sensor to decide which sensor is being polled by the host. The SlotCounter is compared to the SensorID, and if they match, that sensor responds if it is a FrameReqPulse such as an F_OUTPUT or addressed F_SAMPLE pulse with the SENT Frame, and all other sensors do not respond, although they increment their own SlotCounter. If the SlotCounter is incremented past the total number of sensors on the bus (CFG_MAX_SENSOR (0x14 [17:16])), the SlotCounter is returned to 0. Each sensor must be programmed consistently with the total number of sensors so they all roll over to 0 at the same count. Sensors do not increment their SlotCounter on a BroadcastPulse.

The SSENT protocol relies on each sensor maintaining the exact same SlotNumber by counting the AddressingPulses. In order to synchronize all sensors to the same SlotNumber, the SSENT protocol has a broadcast F_SYNC pulse that is used by the host to force all sensors to reset their SlotCounter to 0.

To reduce the burden on the host, and also to improve detection and recovery from BusContention or system errors affecting the SENT bus, the SSENT protocol has the following Configuration options that can be selected.

- When the SENT configuration parameter slot marking is enabled, CFG_SLOT_MARKING (0x14 [23] = 1), each sensor waits a different length of time following an AddressingPulse, based on their SensorID. This leaves the SENT bus in a high state for a varying duration before the sensor pulls the line low to begin the SENT Frame. All sensors on the bus (including the addressed sensor) measure this time to interpret the SensorID of the transmitting sensor. By comparing this to the SlotCounter, each sensor can recognize if an unexpected sensor responded to the AddressingPulse. By default, the sensor would then drop offline, since it cannot

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

be known which sensor is out of sync. This option increases the overhead on the bus and therefore reduces the maximum rate at which sensors can be polled. SlotMarking increases the polling time of a sensor by the SlotMarking time for that sensor. All sensors on a bus must be configured with the same choice for this option.

Table 18: Slot Marking Delay Times for SSENT

SensorID	Delay Time Ticks (Nominal)
0	7
1	18
2	36
3	62

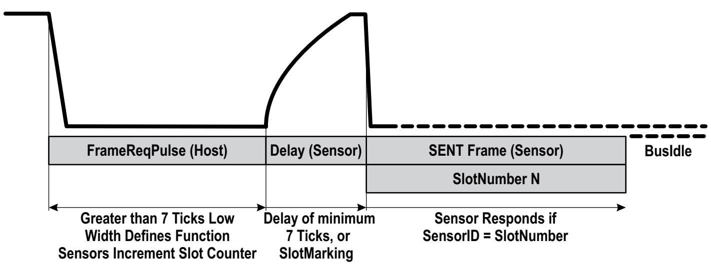


Figure 20: SSENT Sensor Addressing

- When the SENT configuration parameter slot synchronization is enabled, CFG_SLOT_SYNC, (0x14 [24]) = 1, in conjunction with slot marking, CFG_SLOT_MARKING (0x14 [23]), a sensor that is in BusSync for a reason other than BusContention loads its SlotCounter with the measured SlotNumber from the first AddressingPulse that does not have a timeout. A sensor would normally be offline as a result of powering up, reset, or diagnostics. As long as any sensor is online and responding, this allows all other sensors that are offline to automatically synchronize their SlotCounter and begin responding correctly to future AddressingPulses targeting that sensor. If all sensors are offline, though, the host must detect that no sensor responds and issue the F_SYNC function.
- SENT Bus Idle Configuration: When the SENT configuration parameter, CFG_SLOT_SYNC (0x14 [21]), is enabled, a sensor monitors the bus for a long high (BusIdle) period greater than 510 ticks and reset its SlotCounter to 0. This option could be used if sensor polling is expected to always be periodic and continuous, such that the only extended BusIdle time would be after power-up.
- SENT Bus Offline Configuration: When the SENT configuration parameter CFG_POR_OFFLINE (0x14 [22]) is enabled, a sensor stays offline until the host issues F_SYNC, or one of the other synchronization options takes effect (CFG_SLOT_SYNC 0x14 [24] or CFG_IDLE_SYNC (0x14 [21]). If disabled, a sensor powers up with its SlotCounter set to 0 and goes directly online. This allows the sensors to initialize without any host interaction. However, if a sensor experiences a reset event after the bus is in operation, its counter may be out of sync with other sensors, and this could result in bus contention.

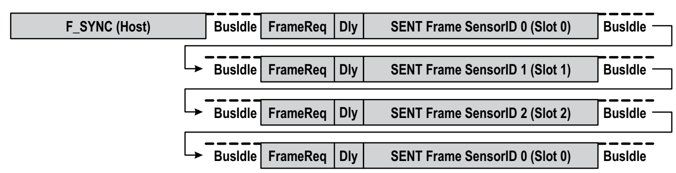


Figure 21: SSENT Sensor Addressing – No Slot Marking (3 Sensors on Bus)

SSENT FUNCTION PULSES

SSENT has a set of function pulses where the host controller must hold the output low. The duration of the low pulse provided by the host controller defines the function, as described in Table 19 and Table 20. Following the low pulse, if the part is addressed to respond and the slot number matches the device slot counter, the device delays the output SENT frame with a minimum of 7-ticks high period to differentiate between the host trigger and the device response. For the fast tick times, the 7-tick high period may be extended to preserve a minimum time of 70.4 µs from the rising edge of the function pulse to the end of the sync pulse required for internal processing. Whether the device responds to a function pulse is defined by the purpose of each pulse.

- F_OUTPUT: Addressed sensor returns a SENT frame with sampled magnetic data. If there is data from a sample-and-hold operation available (F_SAMPLE or via CFG_ZERO_SAMPLE (0x14 [25]) = 1, then that data is returned, otherwise current data is sampled and returned. A sensor configured with CFG_ZERO_SAMPLE (0x14 [25]) = 1 will sample-and-hold on the rising edge of the F_OUTPUT pulse for Slot 0. A sensor configured with CFG_NO_SAMPLE (0x14 [19]) = 1 and CFG_ZERO_SAMPLE (0x14 [25]) = 0 will never sample-and-hold, thus always returns current data in response to F_OUTPUT.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

- CFG_NO_SAMPLE (0x14 [19]) = 1 will sample-and-hold their data at the rising edge of the pulse. If CFG_FSAMPLE_ADR (0x14 [20]) = 0, this is a BroadcastPulse to a sensor, and that sensor will not respond. If CFG_FSAMPLE_ADR (0x14 [20] = 1, this is also an AddressingPulse to a sensor, and the addressed sensor returns a SENT frame with either the sampled or current data. It is recommended, but not required, that all sensors on the bus be configured the same.
- F_SYNC: All sensors synchronize their SlotNumbers by setting their SlotCounters such that the next AddressingPulse is for Slot 0.

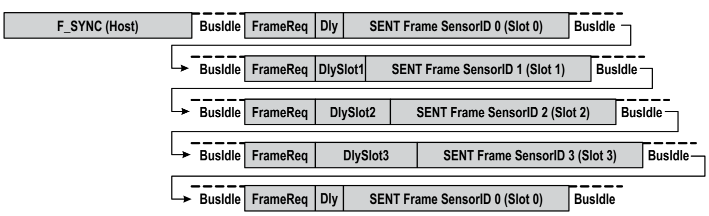


Figure 22: SSENT Sensor Addressing – with Slot Marking (4 Sensors on Bus)

Table 19: SSENT Function Pulses in SHORT_TRIGGER Mode, OUTMSG_MODE = 4

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39
F_SYNC	Broadcast	93	104	115

Table 20: SSENT Function Pulses in LONG_TRIGGER Mode, OUTMSG_MODE = 3

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	9	–	81
F_SYNC	Broadcast	105	140	171

ASENT ADDRESSING PROTOCOL

The ASENT protocol allows sensors to be polled in an arbitrary order. The SensorID is transmitted by the host following any AddressingPulse as a series of 0, 1, 2, or 3 IncAdrPulses. After this sequence, the SENT line is left in a high state, and each sensor recognizes after a time period of about 18 nominal ticks that there are no more IncAdrPulses coming. The sensor whose ID matches the number of IncAdrPulses received responds.

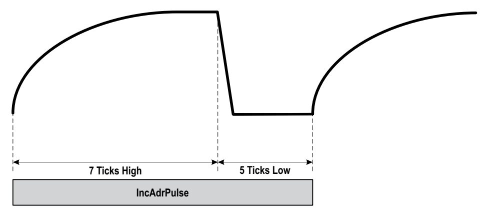


Figure 23: ASENT IncAdrPulse (output by Host)

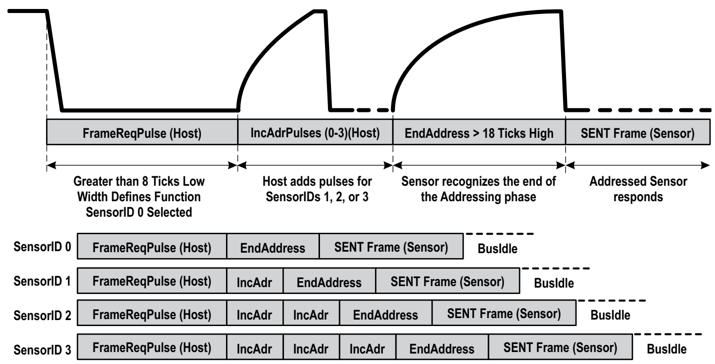


Figure 24: ASENT Sensor Addressing

ASENT FUNCTION PULSES

- F_OUTPUT: Addressed sensor returns a SENT frame with sampled magnetic data. If there is data available from a sample-and-hold operation (F_SAMPLE), then that data is returned; otherwise, current data is sampled and returned. A sensor configured with CFG_NO_SAMPLE (0x14 [19]) = 1 does not sample-and-hold, so it always returns current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for CFG_NO_SAMPLE (0x14 [19]) = 1 will sample-and-hold their data at the rising edge of the pulse. If CFG_FSAMPLE_ADR (0x14 [20] = 0, this is a BroadcastPulse to a sensor, and that sensor will not respond. If CFG_FSAMPLE_ADR (0x14 [20] = 1, this is also an AddressingPulse to a Sensor, and the addressed sensor returns a SENT frame with either the sampled or current data. It is recommended, but not required, that all sensors on the bus be configured the same.

Table 21: ASENT Function Pulses

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

motorSENT INCREMENTAL PROTOCOL

The A17803 integrates an enhancement of SENT and TSENT modes by including a high-speed incremental output line to have fast updates on the angle.

The protocol can be configured in two modes (see Figure 25), selectable with field INC_MODE_PLS0_EDG1:

- Pulse mode (INC_MODE_PLS0_EDG1 = 0): increments are communicated in form of pulses on the increment line. The pulse width is selectable by programming the field ABI_SLEW_INC_PULSE in EEPROM (see Table 22).
- Edge mode (INC_MODE_PLS0_EDG1 = 1): the incremental line voltage is pulled-up or down the voltage of the line depending on previous status when the detected position is increased of a certain Δθ value, so that each rising or falling edge corresponds to an increment Δθ on the position.

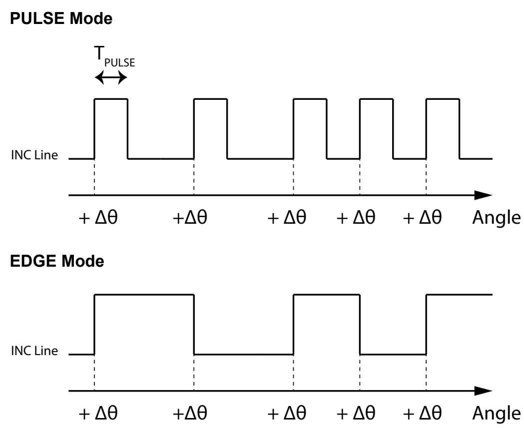


Figure 25: motorSENT Incremental Protocol Modes

Table 22: motorSENT incremental pulse width options

ABI_SLEW_INC_PULSE[11:9]	T_{PULSE}
0	62.5 ns
1	125 ns
2	250 ns
3	500 ns
4	1 µs
5	1.5 µs
6	2 µs
7	3 µs

The Δθ increment size can be selected by programming the field INC_RESOLUTION in EEPROM. Options are reported in Table 16. As for ABI output, a hysteresis window can be programmed to prevent increments due to noise or vibrations, by using INC_HYST field in EEPROM (see Angle Hysteresis section).

Table 24: motorSENT incremental resolution options.

ABI_INC_RESOLUTION	Δθ (degrees)	Angular resolution (bit)
0 [1]	0.005	16
1 [1]	0.011	15
2 [1]	0.022	14
3	0.044	13
4	0.088	12
5	0.176	11
6	0.352	10
7	0.703	9
8	1.406	8
9	2.813	7
10	5.625	6
11	11.25	5
12	22.5	4
13	45	3
14	90	2
15	180	1

[1] In configurations 0,1, and 2, incremental output can be affected by angle noise floor.

Pulse mode supports change of direction communication. A direction and the corresponding Δθ change is signaled by a pulse of width 3 T_{PULSE}. A direction event also counts as an increment or decrement depending on the previous rotation direction. Pulses that follow correspond to the increment in the new direction.

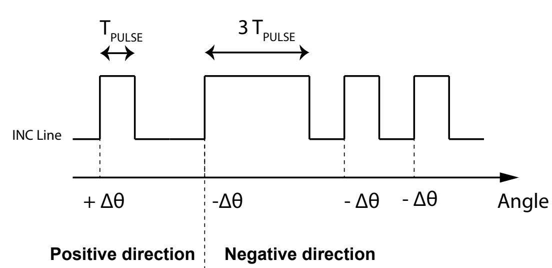


Figure 26: motorSENT Pulse Mode Direction Change

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

motorSENT SPEED LIMITATION

The maximum electrical target speed correctly supported by motorSENT incremental protocol is determined by:

- Maximum possible frequency for incremental line. MAX_f_{INC}, which is dependent on output load. This determines the minimum pulse width that can be selected for Pulse mode and the maximum frequency for the Edge mode.
- Selected incremental resolution.

For Edge mode, the maximum speed can be calculated with the equation:

$$MAX\_SPEED\ [\text{electrical RPM}] = 2 \times MAX\_f_{INC}\ [\text{Hz}] \times \Delta\theta\ [\text{degrees}] / 6$$

For Pulse mode, the maximum speed is dictated by the minimum viable pulse width (load dependent):

$$MAX\_SPEED\ [\text{electrical RPM}] = 1/(2 \times T_{PULSE}\ [\text{s}]) \times \Delta\theta\ [\text{degrees}] / 6$$

When the speed exceeds these limits, the incremental signal is not able to track the changing angle correctly. The host must solely rely on SENT frame angle information.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Incremental Output Interface (ABI)

The A17803 offers an incremental output mode in the form of quadrature A/B and Index outputs to emulate an optical or mechanical encoder. The ABI output is enabled by setting DIG_OUT_MODE_C field in EEPROM to 0, A signal is set on pin 2, B on pin 3, I on pin 4. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per electrical revolution, giving a cycle resolution of ($360 / 2^N$) degrees per cycle. B is offset from A by ¼ of the cycle period. The I signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown in Figure 8.

Since A and B are offset by ¼ of a cycle, they are in quadrature and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

Table 26: Quadrature States

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a Gray coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4
Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2→ Q1

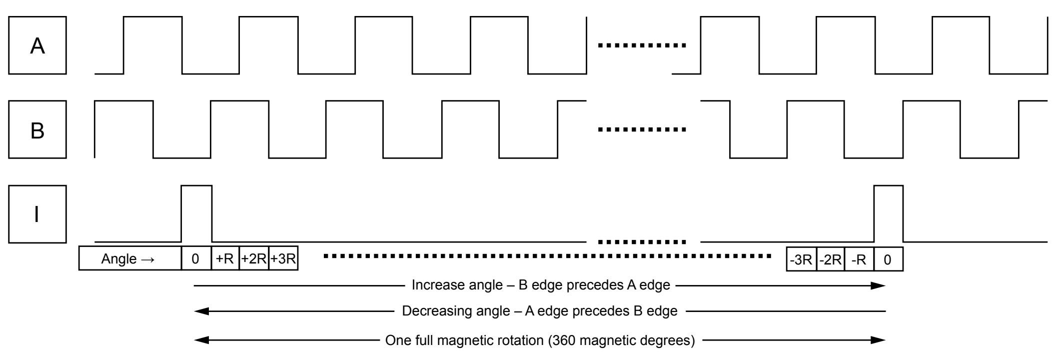


Figure 27: One Full Electrical Revolution

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The duration of one cycle is referred to as 360 electrical degrees, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior.

Ideally, the A and B cycle would be as shown below for a constant velocity:

Practically, the edge rate of the A and B signals and the switching threshold of the receiver I/Os affects the quadrature periods. Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

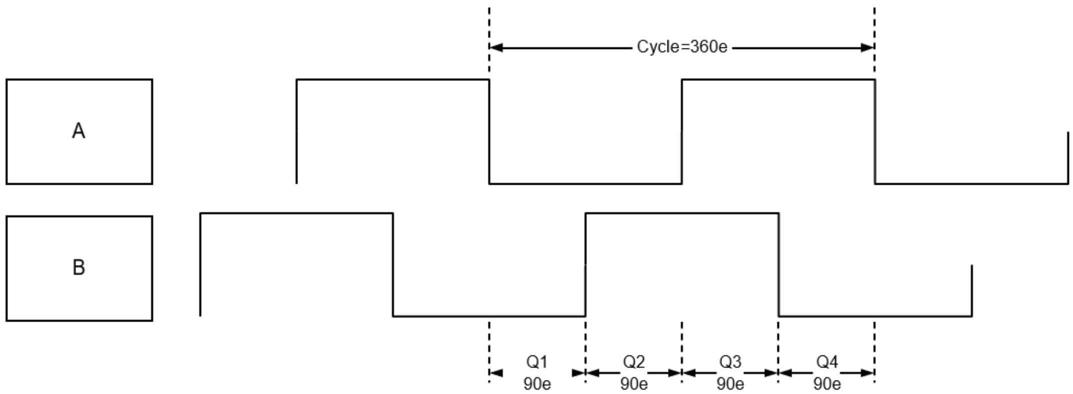


Figure 28: Electrical Cycle

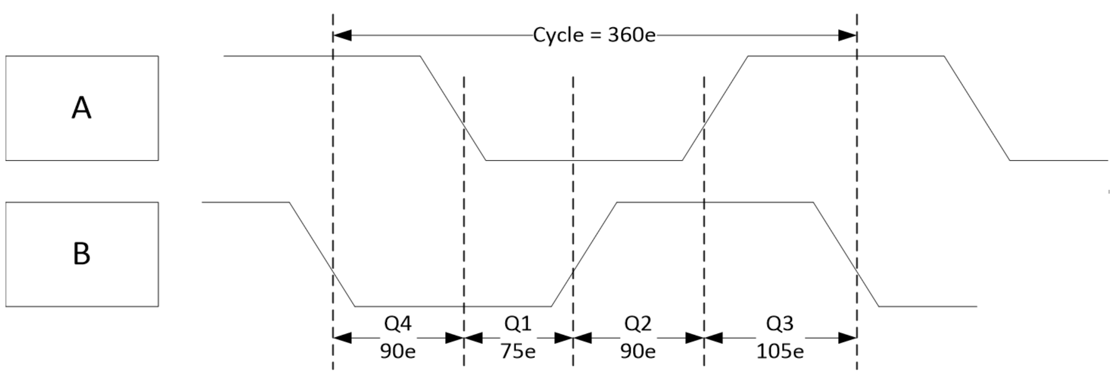


Figure 29: Electrical Cycle

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABI OUTPUT CONFIGURATION

The A17803 ABI output resolution is configurable by setting the parameter ABI_INC_RESOLUTION. The options for ABI Cycle Resolution and Quadrature State Resolution and are shown in Table 27.

Figure 30 shows the maximum rpm for a given ABI resolution and update rate. A rotation rate faster than that shown in the figure results in a skipped ABI step. In this case slew rate limiting (see Slew Rate Limiting for ABI section) is required to maintain absolute angle position via ABI.

Table 27: ABI Cycle Resolution and Quadrature State Resolution

ABI_INC_ RESOLUTION	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = N+2)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0 [1]	14	16	16384	65536	0.0220	0.0055
1 [1]	13	15	8192	32768	0.0439	0.0110
2 [1]	12	14	4096	16384	0.0879	0.0220
3	11	13	2048	8192	0.1758	0.0439
4	10	12	1024	4096	0.3516	0.0879
5	9	11	512	2048	0.7031	0.1758
6	8	10	256	1024	1.4063	0.3516
7	7	9	128	512	2.8125	0.7031
8	6	8	64	256	5.6250	1.4063
9	5	7	32	128	11.2500	2.8125
10	4	6	16	64	22.5000	5.6250
11	3	5	8	32	45.0000	11.2500
12	2	4	4	16	90.0000	22.5000
13	1	3	2	8	180.0000	45.000
14	0	2	1	4	360.0000	90.000
15	n/a	n/a	n/a	n/a	n/a	n/a

[1] Not recommended for use with ABI.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

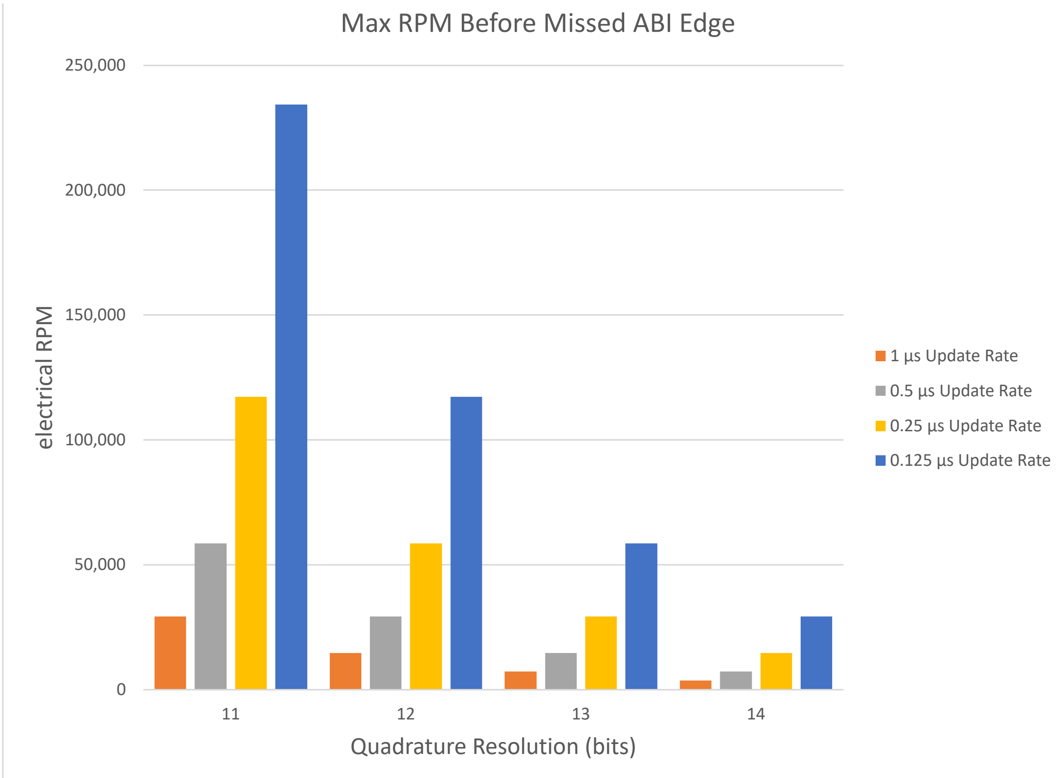


Figure 30: A17803 Resolution Selection for ABI

ABI INVERSION

The logic levels of the ABI pins may be inverted by setting the ABI_INVERT_OUT_EN bit within EEPROM.

INDEX PULSE

The index pulse I (or Z in some descriptions) marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/electrical position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the I pulse has four widths, defined by the ABI_INDEX_MODE EEPROM field:

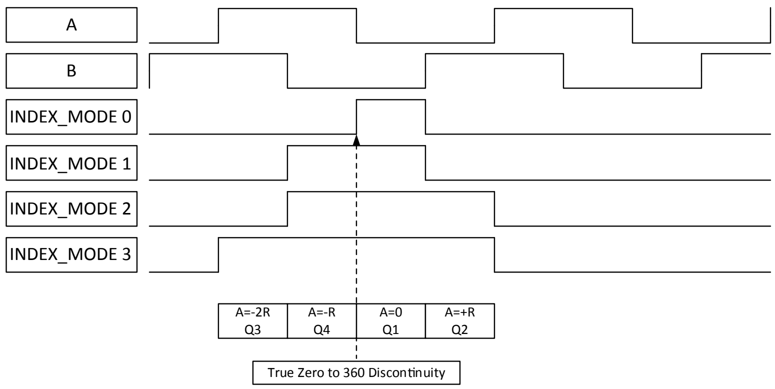


Figure 31: Index Pulse

ABI Count-Up Behavior at Power-Up

ABI interface can be configured to communicate the current absolute angle position at power-on. The behavior at start-up is the following.

- The interface catches up with the actual measured angle by moving in a positive or negative direction, whichever is faster. The time for catching up is at most:

$$t_{catch\text{-}up} = \frac{180°}{R} \times \text{ABI\_SLEW\_TIME}$$

- After catching up with the measured angle, the sensor operates normally.

If ABI_SLEW_RATE is set to 0, there is no catch-up phase. The ABI lines simply output the current electrical angle following device power-on.

When ABI_SLEW_RATE is non-zero, the ABI output automatically counts up to the current angle following any power-cycle.

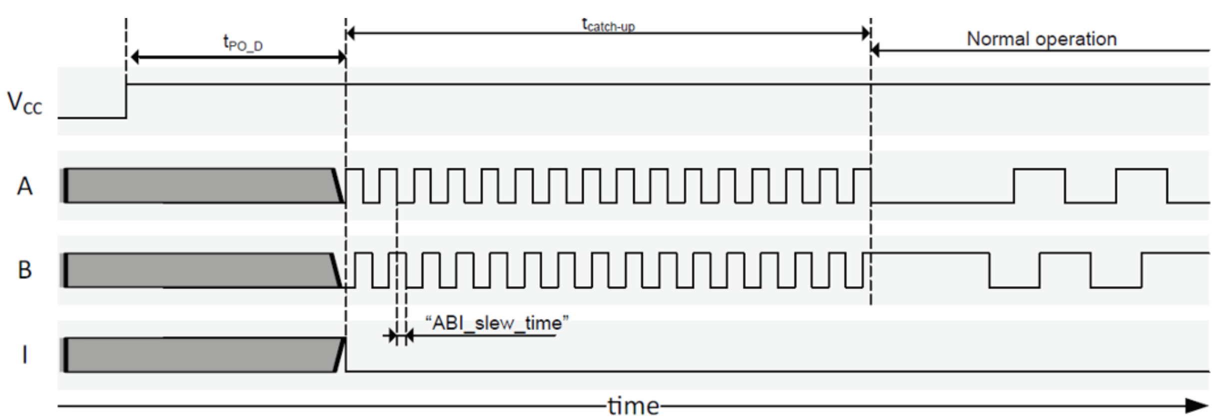


Figure 32: ABI Startup Behavior

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Zero-Degree Position Indication

The edge of the index pulse corresponding to the zero position, as observed by the sensor, changes based on rotation direction, as shown in Figure 33.

With the target rotating such that the observed angle is increasing, the 0° position is indicated by the rising edge of the Index pulse. If the target is rotated in the opposite direction (or if DEL_ANGLE_POL is changed) to produce a decreasing angle value, the 0° position is represented by the falling edge of the Index pulse.

The ABI resolution and I pulse mode selection (described above in Figure 32) determine the width of the Index pulse and the corresponding shift zero position indication.

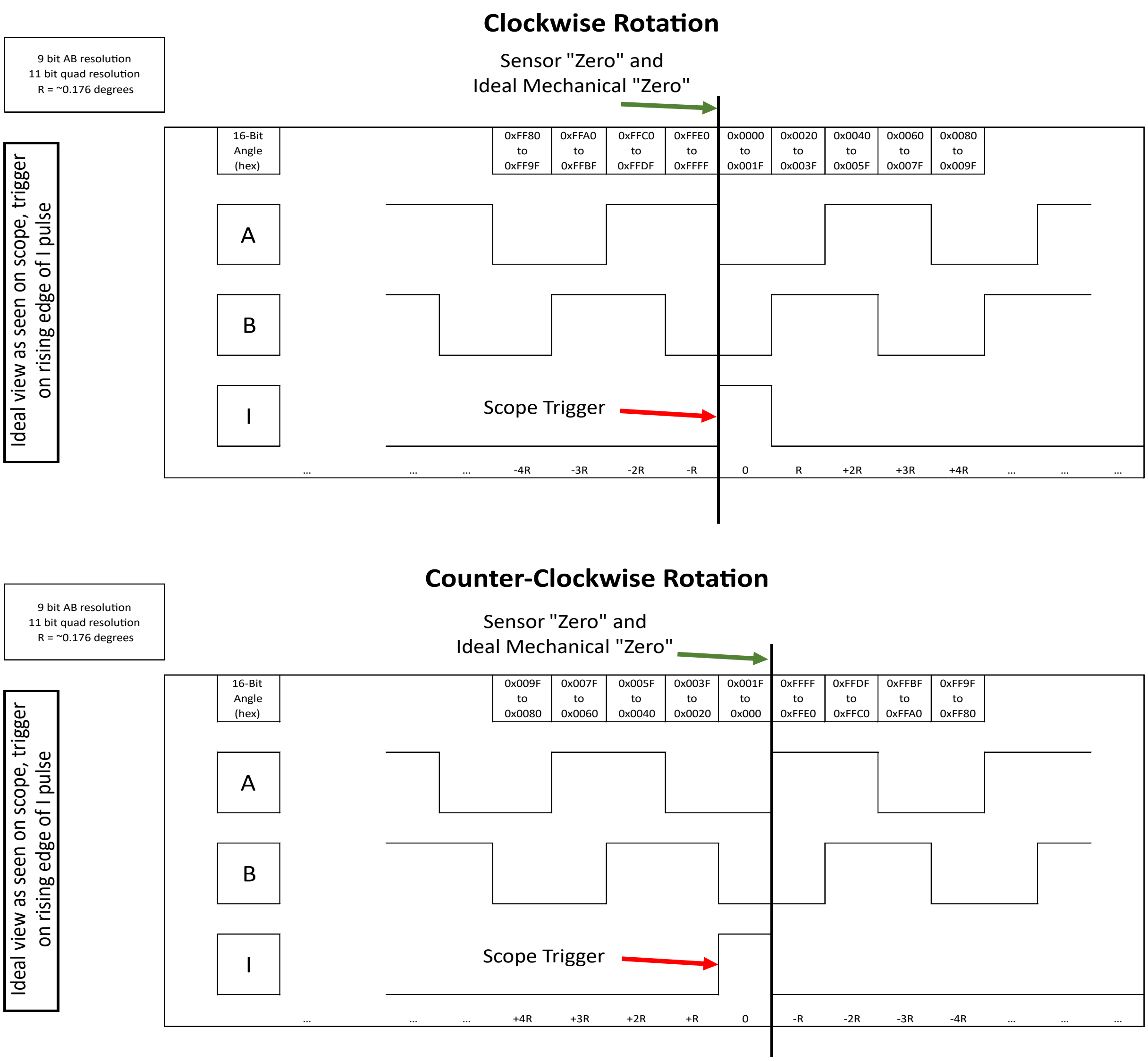


Figure 33: Index Pulse Corresponding to Zero Position

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Slew Rate Limiting for ABI

Slew rate limiting feature may be used to reduce quadrature state errors. The feature is enabled by setting a non-zero value to the parameter ABI_SLEW_RATE. The slew time sets the minimum amount of time that the output must remain in its current state before changing to the next state. This prevents the output from skipping states and can ensure controllers are able to read the state before it changes. This option separates the sensor's observed angle change from the ABI output rate and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby skipping one or more quadrature states. In this case, the slew rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output catches up with the angle samples, at which point the normal sample rate output resumes. This skipping most likely occurs either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs (default refresh rate for ABI). The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation would not on average require ABI transitions greater than the angle sample rate.

In both cases, the ABI output correctly tracks the rotation position; however, the speed of the ABI edges are accomplished at the slew rate limit set in EEPROM.

Figure 34 illustrates the difference between a bad ABI without slew rate limiting and the corrected output via slew rate limiting.

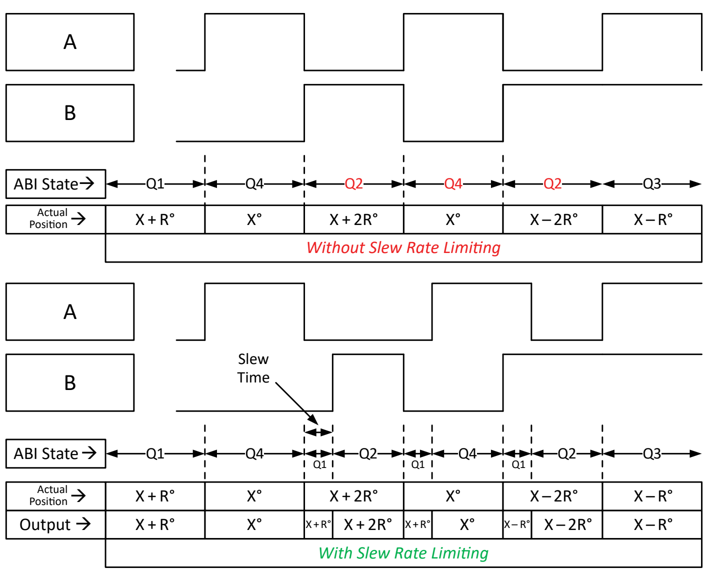


Figure 34: Slew Rate Limiting

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Effective Speed of Slew Time

When slew rate limiting occurs, the ABI update rate is no longer dependent on the observed rotation rate, but instead occurs at a period set by the following EEPROM parameters. This change in the edge rate is observed as a change in the target velocity, and this perceived velocity depends on the following parameters:

- ABI_SLEW_RATE
- ABI_INC_RESOLUTION

Table 28 shows the equivalent rpm for select combinations of slew time and ABI resolution.

When designing a system, it is important to note these RPMs occur for any change in rotation direction (i.e., motor transitioning from CW to CCW rotation), when both hysteresis and ABI slew rate limiting are enabled, as the IC back fills the ABI edges for the programmed hysteresis window INC_HYST.

Table 28: Equivalent RPMs for select combinations of slew time and ABI resolution

EEPROM Setting		Equivalent Velocity (RPM) based on AB Quadrature Resolution		
ABI_SLEW_RATE (Decimal)	Slew Time (µs)	12-Bit Quadrature	11-Bit Quadrature	10-Bit Quadrature
1	0.25	58,593.8	117,187.5	234,375.0
2	0.375	39,062.5	78,125.0	156,250.0
3	0.5	29,296.9	58,593.8	117,187.5
4	0.625	23,437.5	46,875.0	93,750.0
5	0.75	19,531.3	39,062.5	78,125.0
6	0.875	16,741.1	33,482.1	66,964.3
7	1	14,648.4	29,296.9	58,593.8
8	1.125	13,020.8	26,041.7	52,083.3
…	…	…	…	…
62	7.875	1,860.1	3,720.2	7,440.5
63	8	1,831.1	3,662.1	7,324.2

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. The parameter INC_HYST defines the width of an angle window at 16 bits. Mathematically, the width of this window in degrees is:

$$Angle\ Hysteresis = \frac{360}{2^{16}} \times 2^{(INC\_HYST+1)}$$

The parameter INC_HYST is a 3-bit EEPROM field, allowing a range of ≈0.01° to ≈1.41° of hysteresis to be applied. The hysteresis compensated angle is applied to the ABI and motorSENT incremental outputs. This same angle populates the ANGLE_HYST field (primary: 0x12 [15:0]) within the primary serial register space.

The effect of the hysteresis is shown in Figure 35. The current angle position as measured by the sensor is at the head of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the hysteresis-compensated angle is equal to the channel angle output, minimizing latency. If the sensor angle reverses direction, the hysteresis-compensated angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the head was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle skips consecutive resolution steps.
   A. To prevent skipped ABI steps, a non-zero slew rate should be set whenever hysteresis is applied.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle tends to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current head) rather than to the average position of the jitter.

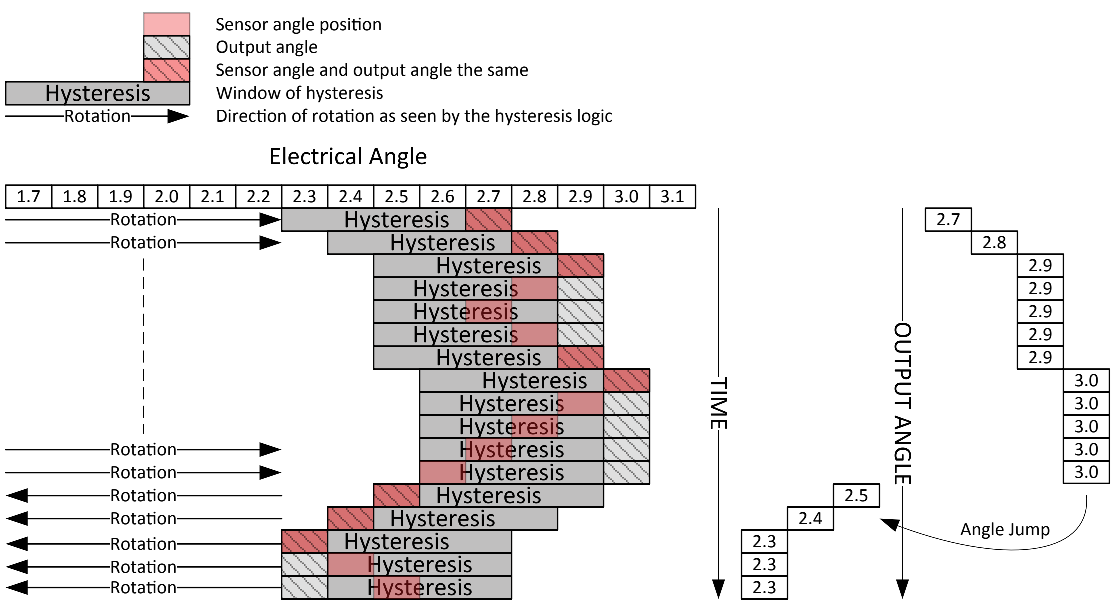


Figure 35: Effect of Hysteresis

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEVICE PROGRAMMING INTERFACES

The A17803 can be programmed in two ways:

- Using the SPI interface for input and output
- Using a Manchester protocol on the PWM/SENT pin to send and receive data

The A17803 does not require special supply voltages to write to the EEPROM.

All accessible fields of the IC may be read and written using both protocols. If EEPROM locking is used, write access using either protocol may be limited.

Interface Structure

The A17803 consists of two memory blocks: direct memory (primary serial registers); and extended memory (EEPROM, shadow memory, volatile registers). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information (for example, angle data, warning flags, field strength, and temperature). All forms of communication (including the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers provide data and address location for accessing extended memory locations. Accessing these extended locations is done in an indirect fashion: The controller writes into the primary interface to give a command to the sensor to access the extended locations. Read/Write is executed, and the result is again presented in the primary interface. This concept is shown in Figure 36.

For writing extended locations, the primary interface registers INDIRECT_WR_ADDRESS (primary: 0x1), INDIRECT_WR_DATA_MSB (primary: 0x2), and INDIRECT_WR_DATA_LSB (primary 0x3) are used for writing extended memory locations. INDIRECT_WR_ADDRESS holds the address of the target extended memory location to be written. INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB, contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_WR_STATUS (primary: 0x4) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For reading extended locations, the primary interface registers INDIRECT_RD_ADDRESS (primary: 0x5), INDIRECT_RD_DATA_MSB (primary: 0x7), and INDIRECT_RD_DATA_LSB (primary 0x8) are used for reading extended memory locations. INDIRECT_RD_ADDRESS holds the address of the target extended memory location to be read. INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_RD_STATUS (primary: 0x6) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For more information on EEPROM and shadow memory read and write access, see EEPROM and Shadow Memory Usage.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the following sections.

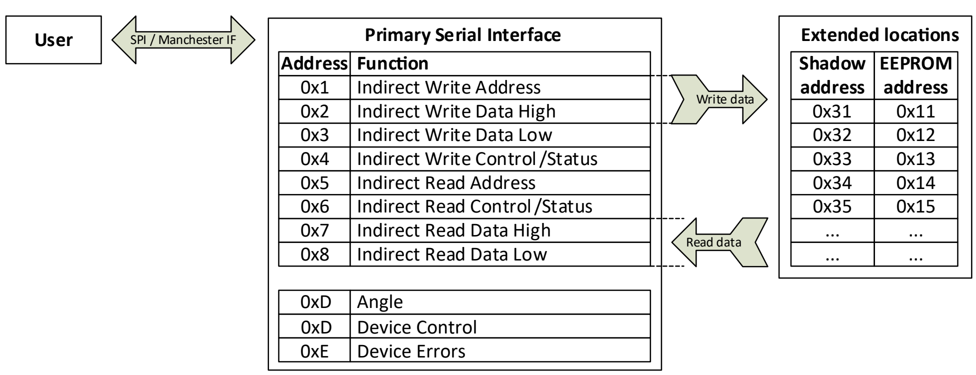


Figure 36: Serial registers allow access to extended memory (EEPROM and shadow)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPI

The A17803 provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1).

The sensor responds to commands received on the MOSI (controller-out/peripheral in), SCLK (serial clock), and CSn (chip-select) pins, and outputs data on the MISO (controller in/peripheral out) pin. SPI may operate at either 3.3 V or 5 V, depending on the interface voltage specified for the part number.

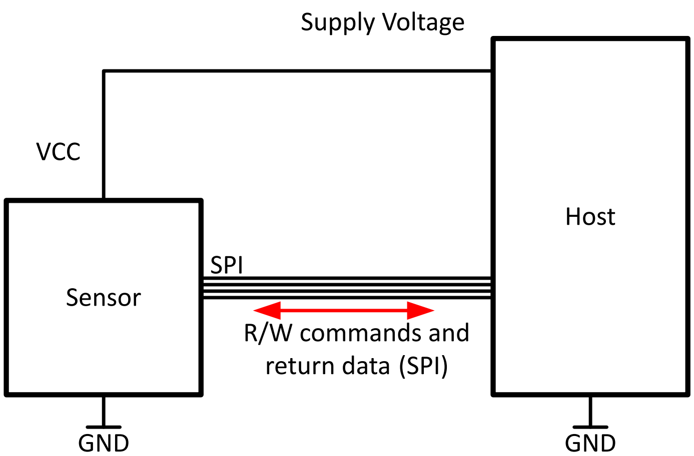


Figure 37: SPI Interface Programming Setup

TIMING

The SPI interface timing parameters are displayed in Figure 38 and Figure 39.

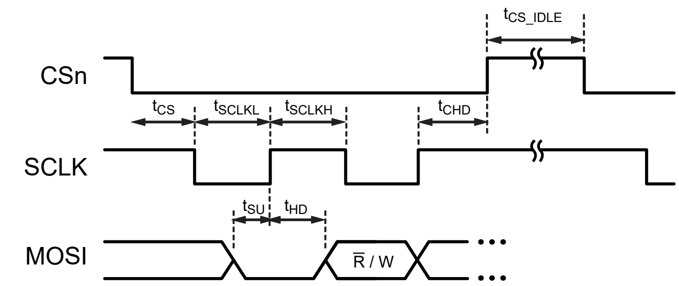


Figure 38: SPI Interface Timings Input

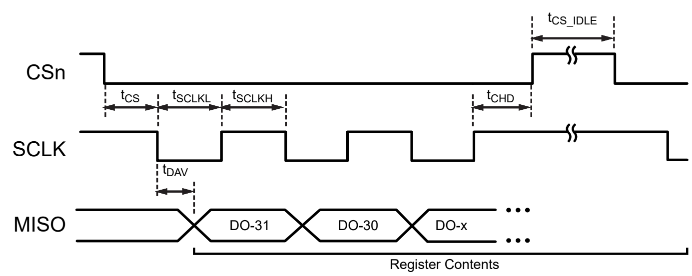


Figure 39: SPI Interface Timings Output

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MESSAGE FRAME

The SPI interface uses a 32-bit packet and is designed to provide a high level of confidence in data integrity. Three SPI transactions are possible: write cycle, read request (from the controller), and read response (from the peripheral).

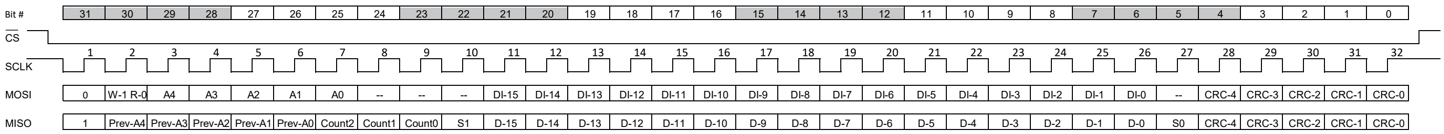


Figure 40: 32-Bit SPI Frame

Write Cycle or Read Request Cycle

The frame structures of the write cycle and read request are shown in Figure 41 and Figure 42, respectively. The frames consist of:

- Start Bit [31]: Static bit with logic = 0. This bit is not used in the CRC calculation.
- R/W [30]: Read/Write bit set to logic = 1 indicates a write cycle; logic = 0 indicates a read request.
- Address [29:25]: Address bits for accessing primary registers.
- Data [21:6]: Data bit for writing primary registers. Considered immaterial for a read request.
- CRC [4:0]: CRC bits calculated on the frame bits [30:5].
- Immaterial bits [24:22, 5]: Can be set to logic = 1 or logic = 0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	Address [4:0]					—			Data [15:0]																—	CRC [4:0]				

Figure 41: Write Cycle SPI Frame

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	Address [4:0]					—			Data [15:0] (Immaterial for a read request)																—	CRC [4:0]				

Figure 42: Read Request Cycle Frame

Read Response Cycle

The read response cycle frame is sent from the IC, as shown in Figure 43. The frame consists of the following:

- Start bit [31]: This bit is set to logic = 1. This bit is not used in the CRC calculation.
- Previous address [30:26]: Register address corresponding to the read request data.
- Frame count [25:23]. Frame counter increments with each SPI frame.
- S1 [22]: Status/Error Flag
  - □ Logical OR of all unmasked error flags.
  - □ Clears once presented following a read (assuming condition has cleared).
- S0 [5]: Status/Error Flag
  - □ Logical OR of all unmasked error flags.
  - □ Clears once presented following a read (assuming condition has cleared).
- Data [21:6]: Data contents from primary register.
- CRC [4:0]: CRC bits calculated over the frame [30:5].

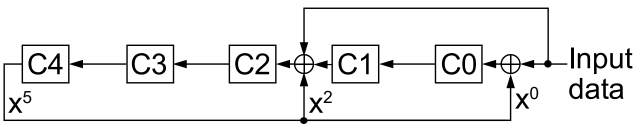
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Previous Address [4:0]					Frame Count [2:0]			S1	Data [15:0]																S0	CRC [4:0]				

Figure 43: Read Response Cycle Frame

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPI CRC

Each SPI frame includes a 5-bit CRC, calculated using the polynomial: $x^5 + x^2 + 1$ with a seed value of 11111_2.



$g(x) = x^5 + x^2 + 1$

Seed: "11111"

Figure 44: CRC Calculation with Left Shift Register

The outgoing CRC is calculated by the A17803 and transmitted on the MISO pin. The incoming CRC must be calculated by the controller and included on the MOSI pin. The A17803 checks the CRC on every incoming frame, and any invalid frame is ignored. The CRC achieves a Hamming distance of 3 for secure data transmission.

The CRC may be calculated with the following Python code:

```python
def spi_crc(data_frame):
    """
    SPI CRC: Takes 27 bit input and generates 5 bit CRC.
    Polynomial = x^5 + x^2 + 1
    Initial CRC value set to all 1s

    Input:
    data_frame: a string representing 27 bit binary data

    Example:
    data_frame= '000111000000000000000000000' #error register read
    print(spi_crc(data_frame))
    Output:  [1, 1, 0, 1, 1]
    """
    crc = list('11111') #CRC seed = 11111
    # MSB of SPI frame is not used during CRC calculation.
    for j in range(1, 27):
        old_crc = crc
        aux_crc_1 = crc[1]
        aux_crc_4 = crc[4]
        crc[4] = int(old_crc[3])
        crc[3] = int(old_crc[2])
        crc[2] = int(aux_crc_1) ^ int(aux_crc_4) ^ int(data_frame[j])
        crc[1] = int(old_crc[0])
        crc[0] = int(aux_crc_4) ^ int(data_frame[j])
    #flips calculated CRC around to obtain value in proper order
    crc = crc[::-1]
    return crc
```


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MISO RESPONSE ON RECEIPT OF BAD CRC

When the A17803 detects an incorrect incoming CRC, the IER flag (direct address 0x0F, bit 15) asserts. A special SPI packet from the A17803 is returned on the next SPI frame. The contents of this special SPI packet are:

- Previous Address [30:26]: Set to 0x0E.
- Data [21:6]: Contains the contents of the error register (primary: 0xE).
  - □ Note: The IER flag is not set on this first SPI packet; however, a read of the error register (address 0x0E) shows the IER flag asserted.

This packet is shown in Figure 45.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	0	1	1	1	0	Frame Count [2:0]			0	IER	XEE	BSY	EUE	ESE	SME	TSE	VCF	TDE	POR	VCC	OFE	ICA	SPD	SAT	SPE	0	CRC [4:0]				

Figure 45: First MISO Response Following a Bad Incoming CRC

MISO RESPONSE FOLLOWING A WRITE

Following a write operation, the MISO packet contains predetermined values within the Previous Address and Data fields:

- Previous Address [30:26]: Set 0x9
- Data [21:6]: Angle value (ANGLE from primary 0x9).

This packet is shown in Figure 46.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	0	Frame Count [2:0]			S1	ANGLE																S0	CRC [4:0]				

Figure 46: MISO Response Following a Write Operation

SPI POWER-ON RESPONSE

After a power-cycle, in the first MISO message S1 and S0 are set to logic 1 when ASIL_EN=1. The full content of the first SPI return packet following a power-on is 0xB840103B:

- S0/S1 = 0
- Address = 0x0E
- FrameCount = 0
- Data = 0x0040
- CRC = 11011

This packet is shown in Figure 47.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1	Address					Frame Cnt			S1	Data																S0	CRC				
Binary	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1

Figure 47: Initial SPI Response Frame Following Power-On

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The second SPI MISO frame always has S0 and S1 set to 1, with POR and IER flags asserted when reading ERROR register. The third SPI frame always has S0 and S1 set to 1 when ASIL_EN=1. In the absence of error conditions, starting from the fourth MISO frame, S0 and S1 are clear.

The MOSI and MISO packets content when reading error register (0x0E) for the first four SPI frames is detailed below.

Frame Number	MOSI Packet Content	MISO Packet Content
1	Read ERROR register 0x1C00001B	Startup frame: 0xB840103B S0=1, S1=1, IER=0, POR=1, no other flag high in absence of error conditions.
2	Read ERROR register 0x1C00001B	Response to frame 1: 0xB8E0102C S0=1, S1=1, IER=1, POR=1, no other flag high in absence of error conditions.
3	Read ERROR register 0x1C00001B	Response to frame 2: 0xB940002B S0=1, S1=1, IER=0, POR=0, no other flag high in absence of error conditions.
4	Read ERROR register 0x1C00001B	Response to frame 3: 0xB9800014 S0=0, S1=0, IER=0, POR=0, no other flag high in absence of error conditions.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Manchester Interface

The A17803-M incorporates a serial interface shared with the PWM/SENT pin. This interface allows an external controller to read and write registers in the A17803 EEPROM and volatile memory. The point-to-point communication protocol is based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first.

The setup for communication using the Manchester interface is given in Figure 48.

The Manchester interface allows programming and readout with a minimal number of pins involved. A valid auxiliary request command recognized by the sensor places the device into communications mode. In this mode, serial data is transmitted or received on the MHT pin. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate requested by the Controller. The high and low logic level for the Manchester serial data is determined by the Manchester High and Low Voltage parameters.

The MHT output consists of an open drain type circuit. A sufficient pull-up resistor and external supply voltage are required.

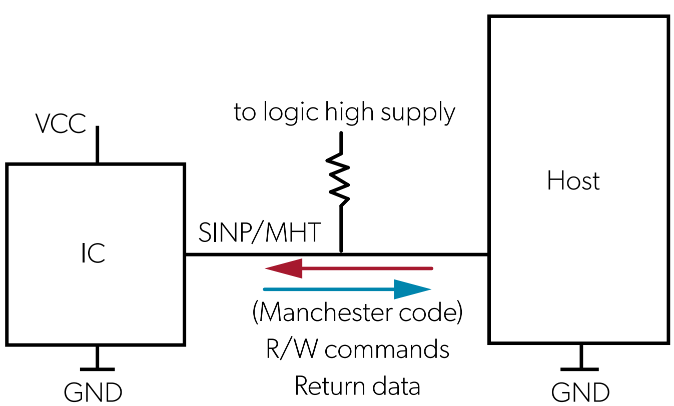


Figure 48: Manchester Programming Interface Setup

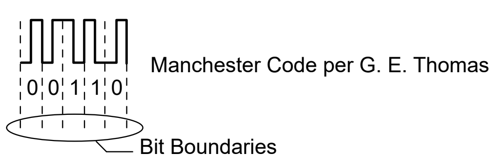


Figure 49: Manchester Code

The general format of the Manchester message frame is shown in Table 29. Serial binary data is encoded using a Manchester encoding scheme, where logic = 1 is indicated by a falling edge within the bit boundary, and logic = 0 is indicated by a rising edge within the bit boundary. The time period T_{BIT} for the bit boundary is determined by the baud rate initiated by the external controller. The A17803 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 29.

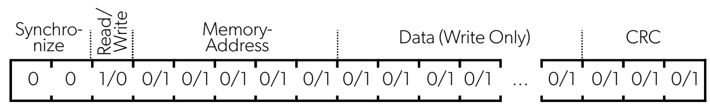


Figure 50: Manchester Message Structure

Table 29: Manchester Message Structure

Quantity of Bits	Name	Values	Description
2	Synchro-nization	0	Used to identify the beginning of a serial interface command and communication bit time
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
5	Address	0x-0x1F	[Read/Write] Register address (of primary serial interface)
16	Data	0/1	Write only
3	CRC	0/1	Bits to check the validity of frame

Programming Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
Bit Rate	Communication Rate	1	–	100	kbps
Manchester Low Voltage	Data pulses on pin 1	0	–	1.27	V
Manchester HighVoltage	Data pulses on pin 1	2.15	–	V_{CC}	V

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

READ COMMAND

The Read command is 11 bits in length, composed of 2 synchronization bits, 1 R/W bit, 5 memory address bits and 3 CRC bits.

READ ACKNOWLEDGE

The Read Acknowledge frame is composed of the synchronization bits, 16 data bits, and 3 CRC bits.

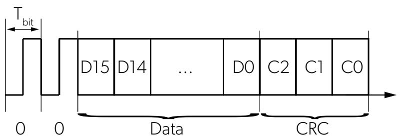


Figure 51: Manchester Read Acknowledge Command

WRITE COMMAND

The Write command is 27 bits in length, composed of 2 synchronization bits, 1 R/W bit, 5 memory address bits, 16 data bits, and 3 CRC bits.

The 5-bit memory address corresponds to the serial register address to which the 16 bits is written.

TIMING DURING A MANCHESTER READ RESPONSE

The A17803 never initiates communication. The A17803 recognizes four transactions: write access, write to EEPROM, write to volatile, and read. Only the read transaction prompts the A17803 to respond with data. When responding to a read command, the A17803 does not check for line contention; it is the responsibility of the controller to release the line in time and to be ready to read the data sent by the A17803.

After a read command is received, there is a delay between when the last bit of the command is sent to the device and when the device begins to respond on the line. This delay has two parts:

- The first part of the delay (t_d) occurs between the time the last bit of the read command is received and the time the device begins to pull the line low in preparation to send data; t_d is typically equal to 1 T_{BIT}.
- The second part of the delay (t_b) occurs between the time the device pulls the line low to the time the device begins outputting data; t_b is typically equal to 1 T_{BIT}. The output is fully readable as long as the controller releases control before $t_d + t_b$; however, it is recommended that the line be released before t_d.

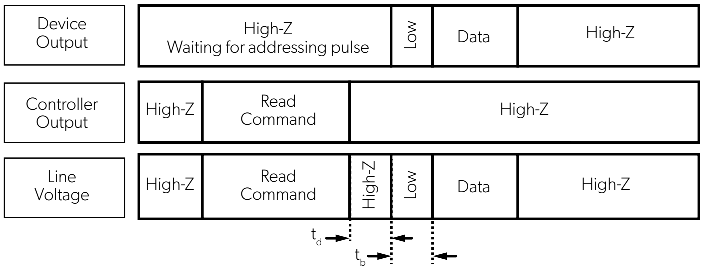


Figure 52: Manchester Read Response Timing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MANCHESTER CRC

The Manchester serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored by the check). The CRC algorithm is based on the following polynomial and the CRC calculation is represented graphically in Figure 53. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 0b111.

$$g(x) = x^3 + x + 1$$

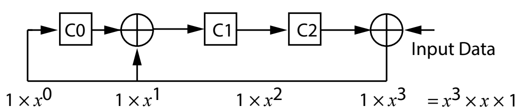


Figure 53: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the Manchester command, right justified, does not include the space for the CRC
// numberOfBits: number of bits in the command not including the 2 zero sync bits at the start of the command and the three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
 bool C0 = false;
 bool C1 = false;
 bool C2 = false;
 bool C0p = true;
 bool C1p = true;
 bool C2p = true;
 uint64_t bitMask = 1;

 bitMask <<= numberOfBits - 1;

 // Calculate the state machine
 for (; bitMask != 0; bitMask >>= 1)
 {
 C2 = C1p;
 C0 = C2p ^ ((data & bitMask) != 0);
 C1 = C0 ^ C0p;

 C0p = C0;
 C1p = C1;
 C2p = C2;
 }

 return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```

DEFAULT MANCHESTER DRIVE OPERATION

When in Manchester mode, the device communicates via an open-drain driver. This applies even when the device has been configured with push/pull or assisted SENT/PWM.

ENTERING MANCHESTER COMMUNICATION MODE

The method of Manchester entry is determined by the PWM/SENT configuration of the IC. The specific entry requirements are controlled by OUTMSG_MODE, SENT_RATE and PWM_PERIOD EEPROM fields.

1. If the IC is configured for PWM, the output line must be held low for at least 2 PWM periods prior to sending the Manchester entry code (as shown in Figure 54)
2. If using a form of free-streaming or Triggered SENT (OUTMSG_MODE = 1, 2, 6, or 7) the SENT frame must be interrupted by an Auxiliary Interrupt Pulse followed by the Manchester entry code (as shown in Figure 55 and Figure 56).
3. If using a version of Shared SENT (OUTMSG_MODE = 3, 4, OR 5), a specific F_AUX pulse is required, followed by the Manchester entry code (Figure 57). A summary is shown in Table 30.

The A17803 is shipped with the following configurations set by the Allegro factory:

- PIN1_PWM1_SENT0 = 0
- OUTMSG_MODE = 1
- SENT_RATE = 0
- PWM_PERIOD = 0

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 30: Auxiliary Command Parameters [1]

Parameter	Symbol	Description		Min	Typ.	Max	Units
Hold Time	t_{hold}	PWM	Auxiliary Command	2 × PWM period	–	–	μs
		SSENT—Short	F_AUX	56	63	70	ticks
		SSENT—Long	F_AUX	216	240	264	ticks
		ASENT	F_AUX	56	63	70	ticks
		SENT	Aux. Interrupt Pulse	30	–	–	ticks
		TSENT	Aux. Interrupt Pulse	30	–	–	ticks
Edge Detection Time	t_{gate}			0.7	–	–	μs
Access Code Window	t_{msgRX}			1.4	–	300	μs

[1] Parameter is not measured at final test. Determined by design.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Manchester Auxiliary Interrupt Pulse for PWM Output Mode

To initialize communication using the Manchester Auxiliary command when the A17803 is configured with PWM output, the auxiliary interrupt pulse can be applied at any time. The auxiliary pulse must have a minimum width of t_{HOLD}, after which the pulse is released for t_{GATE} plus the rise time to allow the line to pull high and the device to register a rising edge. After this, the controller must pull low for t_{GATE} before beginning to send the Manchester access code. If the device does not recognize the first rising edge of the Manchester access code before t_{msgRX}, after the hold time, a timeout of the device occurs, Manchester initialization aborts, and PWM functionality returns. The Manchester Auxiliary command for PWM output is shown in Figure 54.

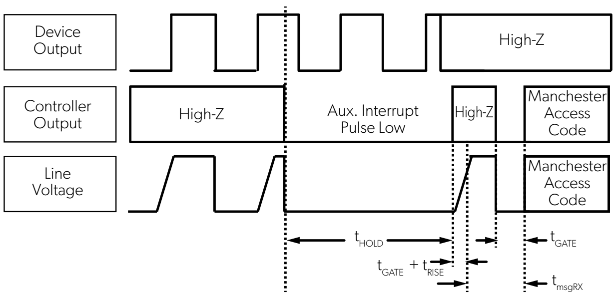


Figure 54: Entering Manchester from PWM

Manchester Auxiliary Command for SENT Output Mode

To initialize communication using the Manchester auxiliary command when the A17803 is configured with free-streaming SENT (OUTMSG_MODE = 1 or 7), the auxiliary interrupt pulse can begin at any time. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to pull high, followed by a low period of t_{GATE} before sending the Manchester access code. If the first rising edge of the Manchester access code is not observed before t_{msgRX}, a timeout of the the device occurs, Manchester initialization aborts, and the device returns to normal functionality. The Manchester auxiliary command is shown in Figure 55.

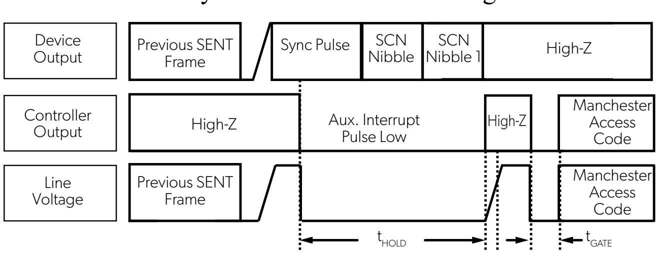


Figure 55: Entering Manchester using SENT

Manchester Auxiliary Command for TSENT Output Mode

To initiate Manchester communication when the A17803 is configured with the TSENT output (OUTMSG_MODE = 2 or 6), the auxiliary interrupt pulse must be transmitted during the SENT message frame, requiring a trigger pulse to begin a SENT frame. The auxiliary interrupt pulse must begin between 8 and 56 ticks following the completion of the trigger pulse. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to return high, followed by a low period of t_{GATE} before sending the Manchester access code. If the first rising edge of the Manchester access code is not observed before t_{msgRX}, a timeout of the device occurs, Manchester initiation aborts, and the device returns to normal functionality. The Manchester Auxiliary command is shown in Figure 56.

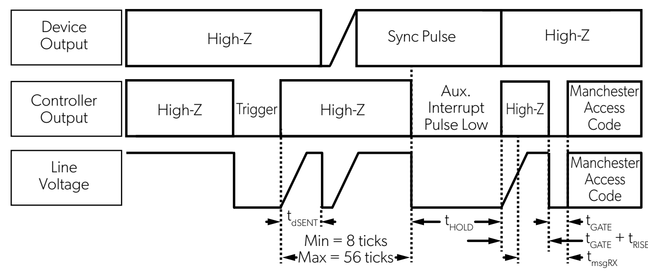


Figure 56: Entering Manchester using TSENT

Manchester Auxiliary Command for Shared SENT (SSENT and ASENT)

To initialize communication using the Manchester Auxiliary command when the A17803 is configured with SSENT or ASENT output, the auxiliary function pulse, F_AUX, is applied as the frame request pulse. The auxiliary pulse must have a minimum width of t_{HOLD}. After the pulse is released, the output line is required to go high-Z for t_{GATE} plus the rise time. The controller must then pull the output line low for t_{GATE} before sending the Manchester access code. If the first rising edge of the access code is not recognized before t_{msgRX}, a timeout occurs, the Manchester initialization aborts, and the output returns to normal functionality.

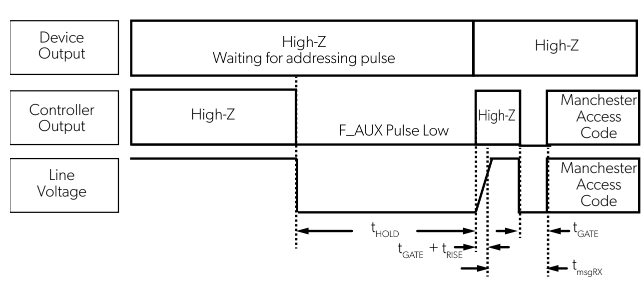


Figure 57: Entering Manchester using Shared SENT

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

EEPROM AND SHADOW MEMORY USAGE

The A17803 device features include integrated EEPROM to permanently store configuration parameters for operation. EEPROM is customer programmable and retains data, or parameter values, to configure the device for the application requirements. After a reset or EEPROM write operation, parameter data is copied from EEPROM to shadow (volatile) memory. Parameter data in shadow memory can be overwritten by performing an extended write to the shadow addresses. Access of device parameters through shadow memory is faster than access through EEPROM. In situations where it is desired to test many parameters quickly before permanently programming, use of shadow memory is recommended. The shadow memory registers have the same format as EEPROM and are accessed at extended addresses 0x20 higher than the equivalent EEPROM address. Some bits do not impact device operation and are not copied into shadow memory. Shadow registers do not contain the ECC bits and may have read or write protection restrictions similar to EEPROM.

Enabling EEPROM Access

Reads and writes to indirect memory, EEPROM, and shadow memory are restricted and require an unlock code. The unlock code must be written to the primary serial register access (primary: 0x1E [15:0]) within 20 ms from power-on. This involves two write commands, which should be executed one after the other.

The last bit of unlock code sets or clears field COMM_EN (extended 0xA5 [15]), determining if output is disabled or not. When COMM_EN is set, it allows continuous R/W commands with the output being disabled without needing to overdriving the output pin.

Sequence to enable memory access while keeping output enabled (COMM_EN=0):

Write 0xC418 to register primary 0x1E [15:0].

Write 0x0E80 to register primary 0x1E [15:0].

Sequence to enable memory access and disable output (COMM_EN=1):

Write 0xC418 to register primary 0x1E [15:0].

Write 0x0E81 to register primary 0x1E [15:0].

When the COMM_EN is written with logic = 0, or when a reset event occurs, the outputs are enabled again.

The access status is indicated by the direct serial register access. A read of primary 0x1E [1] set to logic = 1 indicates the customer unlock code is set.

When using SPI interface customer unlock code is not required for write and read operations to all direct serial registers.

Following an EEPROM write, EEPROM margin checking should be performed. The device must be unlocked when performing margin checks.

EEPROM and Shadow Access Protections

The A17802 contains features to protect against unwanted EEPROM access.

- Setting the EEPROM parameter MEM_LOCK (extended: 0x1F [23:20]) to a value of 0xC (1100 binary) restricts write access to prevent changes to the EEPROM registers. Temporary changes to device configuration settings are still possible by writing to the indirect volatile and shadow memory. Note, any changes to the indirect volatile memory are reset after a device reset event. Read access of the EEPROM is still possible.
- Setting the EEPROM parameter MEM_LOCK (extended: 0x1F [23:20]) to a value of 0x3 (0011 binary) restricts write access to prevent changes to EEPROM, indirect volatile, and shadow memory. Once set, the parameter settings in indirect memory are read only. Read access is still possible.
- Writes to MEM_LOCK with the above values are one-time access only and are not erasable through subsequent write commands.

Write Transactions to Extended Memory: EEPROM, Shadow, and Volatile

Invoking an extended write access is a three-step process:

1. Write the target extended address to the primary register INDIRECT_WR_ADDRESS (primary: 0x1 [7:0]).
2. Write the desired data, for the target extended register, to the primary registers INDIRECT_WR_DATA_MSB (primary: 0x2 [15:0]) and INDIRECT_WR_DATA_LSB (primary: 0x3 [15:0]). The register INDIRECT_WR_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_WR_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.
3. Execute the extended memory write by setting the extended memory execute write bit (EXW; primary: 0x4 [15]), to logic = 1.

   A. EEPROM writes require ≈ 6.5 ms to complete.

When EXW is set, the 32 bits of data contained in INDIRECT_WR_DATA_LSB and INDIRECT_WR_DATA_LSB are written to the indirect memory address specified by INDIRECT_WR_ADDRESS. The status of the write operation may be interrogated

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

by polling the primary register INDIRECT_WR_STATUS (primary: 0x4). The write-in-progress bit (WIP; primary: 0x4 [8]), when set, indicates the write transaction in progress. The write operation done bit (WDN; primary: 0x4 [0]), when set, indicates the write transaction is done or complete. The extended execute error status bit (XEE; primary: 0x0F [14]), when set, indicates an error occurred when executing the write. For example, if a write is attempted without the proper access enabled, XEE indicates an error.

READ TRANSACTION FROM EEPROM AND OTHER EXTENDED LOCATIONS

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the INDIRECT_RD_ADDRESS (primary: 0x5) register (using SPI or Manchester direct access). The 8-bit extended address that determines which extended memory address to access is INDIRECT_RD_ADDRESS.
2. Invoke the extended access by writing the extended read bit (EXR; primary: 0x6 [15]) with a value of 1. The address specified in INDIRECT_RD_ADDRESS is then read, and the data is loaded into the registers INDIRECT_RD_DATA_MSB (primary: 0x7) and INDIRECT_RD_DATA_LSB (primary: 0x8).
3. Read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB (using SPI or Manchester direct access) to get the full data contents of the extended read address. The register INDIRECT_RD_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_RD_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.

EEPROM read accesses may take up to 2 µs to complete. The read operation done bit (RDN; primary: 0x6 [0]) can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB if the read access is in process (RIP; primary: 0x6 [8] = 1), as it could change during the serial access, which would result in inconsistent data. It is also possible that an SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, the shadow extended addresses must be addressed. Shadow extended addresses are located at an offset of 0x20 above the EEPROM. For all addresses, refer to the EEPROM section, Table 3 and Table 4.

EEPROM Margin Check

The A17803 contains a test mode, EEPROM margining, to check the logic levels of the EEPROM bits. EEPROM margining is customer accessible. EEPROM margining is selectable to check all logic = 1 values, logic = 0 values, or both. The results of the test are reported back in extended memory registers 0x42, 0x43, and 0x44. Note that a fail of the margin test does not force the outputs to a diagnostic state or trigger a diagnostic error flag. The following is a step-by-step procedure to verify EEPROM programming:

1. Enable EEPROM access by sending the unlock code to primary address 0x1E
2. Write a 1 to the MARGIN_START field (volatile 0x44 [0])
   A. Once started the device automatically checks high/low thresholds for all EEPROM addresses.
3. Read MARGIN_STATUS (volatile 0x44[4:3])
   0 = No result from margin testing (margin testing not run)
   1 = Pass. Margin checking completed with no errors.
   2 = Failure detected during margin testing
   3 = Running. Margin testing is still running.
4. If a margin failure is detected additional information can be retrieved.
   MARGIN_MIN_MAX_FAIL [volatile 0x44 [5]
   0 = Margin low threshold failure
   1 = Margin high threshold failure
   EE_ADDR [volatile 0x42 [11:7] contains the failing address.
5. EEPROM should not be considered valid unless margin testing passes. If the margin failure occurs on a previously modified address space, EEPROM can be rewritten and margin checking repeated in an attempt to clear the issue.

For more information about EEPROM margining, refer to the Volatile Memory Map section (addresses 0x42, 0x43, and 0x44). Time required to verify margin levels across all EEPROM is ≈100 µs

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 31: Direct Serial Interface Registers Bits Map

ADDRESS (0x00)	REGISTER SYMBOL	ACCESS	PRIMARY ADDRESSED BYTE (MSB)								PRIMARY ADDRESSED BYTE (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	NULL_REG	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x01	INDIRECT_WR_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
0x02	INDIRECT_WR_DATA_MSB	RW	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
0x03	INDIRECT_WR_DATA_LSB	RW	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
0x04	INDIRECT_WR_STATUS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x05	INDIRECT_RD_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_READ_ADDR							
0x06	INDIRECT_RD_STATUS	RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x07	INDIRECT_RD_DATA_MSB	RO	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
0x08	INDIRECT_RD_DATA_LSB	RO	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
0x09	ANGLE_ROW	RO	ANGLE															
0x0A	SPEED_ROW	RO	SPEED															
0x0B	TURNS_COUNTER	RW	0	0	TCW_ERROR	TCO_ERROR	0	TURNS_COUNT										
0x0C	TURNS_COUNTER_ LATCH	RO	0	0	TCW_ERROR_LATCH	TCO_ERROR_LATCH	0	STURNS_COUNT_LATCH										
0x0D	CTRL	RO	0	0	0	0	0	0	0	0	0	0	0	0	COMM_EN	TC_RST	TC_WR_EN	SOFT_RST
0x0E	ERROR	ROC	IER	XEE	BSY	EUE	ESE	SME	TSE	VCF	TDE	POR	VCC	OFE	ICA	SPD	SAT	SPE
0x0F	TEMPERATURE_ROW	RO	TEMPERATURE															
0x10	X_EHC_ROW	RO	X_EHC															
0x11	Y_EHC_ROW	RO	Y_EHC															
0x12	ANGLE_HYST_ROW	RO	ANGLE_HYST															
0x1E	ACCESS	RO/WO	ACCESS_KEY		FREE_ REG_ LOCK_RD	FREE_ REG_ LOCK_WR	FACT	FACT	CUST_ REG_ LOCK_RD	CUST_ REG_ LOCK_ WR	FACT	FACT	CUST_ EE_ LOCK_RD	CUST_ EE_ LOCK_WR	FACT	FACT	CUST_ ACCESS	FACT
0x1F	LOOPBACK_REG	RW	LOOPBACK															

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x00 (NOP) – Null Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Address 0x01 (INDIRECT_WR_ADDRESS) Extended Write Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_ADDR [7:0]

Target address to be used for an extended memory write. Address ranges:

Extended 0x00 - 0x1F: EEPROM (requires ≈ 6 ms following execution of a write)

Extended 0x24 - 0x3F: Shadow (Volatile)

Extended 0x40 - 0x71: Miscellaneous (Volatile)

Address 0x02 (INDIRECT_WR_DATA_MSB) Extended Write Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_3 [15:8]

Upper fourth byte of data for an extended write operation, corresponds to bit [31:24] of the extended write address.

INDIRECT_WR_DATA_2 [7:0]

Third byte of data for an extended write operation, corresponds to bit [23:16] of the extended write address.

Address 0x03 (INDIRECT_WR_DATA_LSB) Extended Write Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_1 [15:8]

Second byte of data for an extended write operation, corresponds to bit [15:8] of the extended write address.

INDIRECT_WR_DATA_0 [7:0]

Lower first byte of data for an extended write operation, corresponds to bit [7:0] of the extended write address.

Address 0x04 (INDIRECT_WR_STATUS) Extended Write Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXW [15]

Initiates extended write by writing 1. Sets WIP, clears WDN. Write-only, always reads back 0.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

WIP [8]

Indicates write in progress when set to 1.

WDN [0]

Write operation complete when to a value of 1, clears when EXW is set to 1.

Address 0x05 (INDIRECT_RD_ADDRESS) Extended Read Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_RD_ADDR [7:0]

Address to be used for an extended read. Address ranges:

Extended 0x00 - 0x1F: EEPROM (requires ≈ 2µs)

Extended 0x24 - 0x3F: Shadow (Volatile)

Extended 0x40 - 0x71: Miscellaneous (Volatile)

Address 0x06 (INDIRECT_RD_STATUS) Extended Read Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXR [15]

Initiates extended read by writing 1. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP [8]

Indicates read in progress when set to 1.

RDN [0]

Read operation complete when to a value of 1, clears when EXR is set to 1.

Address 0x07 (INDIRECT_RD_DATA_MSB) Extended Read Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

INDIRECT_RD_DATA_3 [15:8]

Upper fourth byte of data for an extended read operation, corresponds to bit [31:24] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_2 [7:0]

Third byte of data for an extended read operation, corresponds to bit [23:16] of the extended read address after execution of a read operation.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x08 (INDIRECT_RD_DATA_LSB) Extended Read Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

INDIRECT_RD_DATA_1 [15:8]

Second byte of data for an extended read operation, corresponds to bit [15:8] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_0 [7:0]

Lower first byte of data for an extended read operation, corresponds to bit [7:0] of the extended read address after execution of a read operation.

Address 0x09 (ANGLE_ROW) Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE [15:0]:

Register indicates the calculated angle from the RX1 (sin or Y channel) and the RX2 (cos or X channel) inputs. The parameter is a 16-bit unsigned integer with value of angle x 360/2^16 in degrees.

Address 0x0A (SPEED_ROW) Speed Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPEED															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

SPEED [15:0]:

Register indicates the calculated angular velocity. The parameter is a 16-bit signed integer.
Velocity in revolutions per minute can be calculated as:
Velocity[RPM] = uncomplement(speed[15:0]) × 14.3051
Accuracy of the velocity measurement is not quantified at final test and is not guaranteed by Allegro.

Address 0x0B (TURNS_COUNTER) Turns Counter Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ ERROR	TCO_ ERROR	0	TURNS_COUNT										
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

TCW_ERROR [13]:

Turns counter warning. The bit is set on a condition that may compromise the accuracy of the turns count value. The bit is redundant with TCW_ERROR and TCW_ERROR_LATCH.

Value	Description
0	No turns count warning
1	Turns count value may be incorrect

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TCO_ERROR [12]:

Turns Counter Overflow Error. Indicates the turns counter surpassed its allowable range of –1024 to 1023 (approximately ±256 rotations). Must be cleared with a turns-count reset (See special commands in the CTRL register description, primary: 0xF).

Value	Description
0	No turns count overflow error
1	Primary Turns count overflow error

TURNS_COUNT [10:0]:

Turns count. Value represents the primary channel turns count Indicates total number of turns relative to initial value at power-on. The parameter has a resolution of 90° and represented as an 11-bit signed integer.

Decimal Value	Binary Bit Value	Turns Count 90° resolution (Actual electrical full rotations)
0	000 0000 0000	0 (0)
1	000 0000 0001	+1 (+0.25)
511	0001 1111 1111	+511 (127.75)
512	010 0000 0000	+512 (128)
1023	011 1111 1111	+1023(+255.75)
–1	111 1111 1111	–1 (–0.25)
–512	110 0000 0000	–512 (–128)
–1024	1000 0000 0000	–1024 (–256)

Address 0x0C (TURNS_COUNTER_LATCH) Latched Turns Counter

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ERROR_LATCH	TCO_ERROR_LATCH	0	TURNS_COUNT_LATCH										
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

TCW_ERROR_LATCH [13]:

Latched Turns Counter Warning. The bit has the same definition as TCW_ERROR and is latched on the read of angle.

TCO_ERROR_LATCH [12]:

Latched Turns Counter Overflow Error. The bit has the same definition as TCO_ERROR and is latched on the read of angle.

TURNS_COUNT_LATCH [10:0]:

Latched Turns Count. The parameter has the same definition as TURNS_COUNT and is latched on the read of angle.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x0D (CTRL) Control register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	COMM_EN	TC_RST	TC_WR_EN	SOFT_RST
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

COMM_EN [3]:
Allows continuous R/W commands with the output being disabled without needing to overdriving the output pin.
TC_RST [2]:
Turns count reset for signal path. Generates a one clock pulse reset signal.
TC_WR_EN [1]:
Turns count write enable.
SOFT_RST [0]:
Soft Reset. Writing at value of one to this bit triggers a full reset of the device logic, reset of all the status and error registers, reset of the signal processing, and reset of the outputs and communication protocols.

Address 0x0E (ERROR) Device Error Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	XEE	BSY	EUE	ESE	SME	TSE	VCF	TDE	POR	VCC	OFE	ICA	SPD	SAT	SPE
Access	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC

All errors in the register are latched, meaning they remain in a high logic state after they occurred until they are cleared. Errors clear after a read of the register and the error conditions no longer persist. An example is after a power on event the POR error flag is asserted a read of this register resets the POR error flag.

IER [15]: Interface Error Condition

XEE [14]: Extended Execute Error Condition

BSY [13]: Extended Access Busy Condition

EUE [12]: EEPROM Double Bit Error Flag

ESE [11]: EEPROM Single Bit Error Flag

SME [10]: Shadow Memory Error (multiple-input shift register signature error)

TSE [9]: Temperature Error

VCF [8]: Voltage Check Failure Error

TDE [7]: Transmitting Signal/Driver Error

POR [6]: Power On Reset Event

VCC [5]: Overvoltage/Undervoltage Error

OFE [4]: Oscillator Frequency Error

ICA [3]: Input Signal Out of Range Error

SPD [2]: Maximum Speed Error

SAT [1]: Saturation Error

SPE [0]: Angle error

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x0F (TEMPERATURE_ROW) Temperature

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPERATURE												UNUSED			
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TEMPERATURE [15:4]:
Current ambient temperature from the internal temperature sensor.
Temperature is coded as a 12-bit signed integer on the first 12 MSB (TEMPERATURE[15:4]).
To obtain the temperature reading in degrees Celsius the following equation is used:
Temperature (°C) ≈ uncomplemented(TEMPERATURE[15:4]) / 13.3226 + 25

Address 0x10 (X_EHC_ROW) X_EHC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	X_EHC															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

X_EHC [15:0]:
Digital x channel register, corresponding to RX2 input (cosine input), after OGT, offset autocalibration compensation, and electrical harmonic compensation. Value is used by the IC to calculate angle.

Address 0x11 (Y_EHC_ROW) Y_EHC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y_EHC															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Y_EHC [15:0]:
Digital y channel register, corresponding to RX1 input (sine input), after OGT, offset autocalibration compensation, and electrical harmonic compensation. Value is used by the IC to calculate angle.

Address 0x12 (ANGLE_HYST _ROW) Hysteresis Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_HYST															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_HYST [15:0]:
Register indicates the angle with hysteresis applied. The parameter is a 16-bit unsigned integer with value of angle × 360 / 2^{16} in degrees.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1E (ACCESS) Access Register

Writing to register 0x1E is special command to enable access to the extended memory space, EEPROM and Volatile. See section Enabling EEPROM Access for more information.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														CUSTOMER_ ACCESS	RESERVED
Access	WO	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CUSTOMER_ACCESS [1]

Bit indicates access to customer registers within the extended memory space. A logic value of 1 indicates access to the customer registers within the extended memory space is enabled.

Address 0x1F (LOOPBACK_REG) Loopback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOOPBACK															
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

LOOPBACK [15:0]

Customer loopback register. The registers allow the external controller to perform a loopback test of the SPI communication between the controller and the peripheral A17803.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

EXTENDED MEMORY TABLE

EEPROM (NONVOLATILE), SHADOW (VOLATILE), AND MISCELLANEOUS (VOLATILE)

The EEPROM/Shadow register bitmap is shown below. All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires a device unlock. The shadow memory is a copy of the EEPROM in the address range 0x24 to 0x3F.

Table 32: EEPROM/Shadow Memory Map

<table>
<tr><th rowspan="2">EEPROM Address</th><th rowspan="2">Shadow Address</th><th colspan="27">Bits</th></tr>
<tr><th>31:26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x00</td><td>N/A</td><td>ECC</td><td colspan="4">factory reserved</td><td colspan="16">FACTORY_DIE_ID</td><td colspan="6">factory reserved</td></tr>
<tr><td>0x01</td><td>N/A</td><td>ECC</td><td colspan="4">factory reserved</td><td colspan="16">FACTORY_LOT</td><td colspan="6">FACTORY_WAFER</td></tr>
<tr><td>0x02</td><td>N/A</td><td>ECC</td><td colspan="16">CAS_ID</td><td colspan="10">factory reserved</td></tr>
<tr><td>0x03</td><td>N/A</td><td>ECC</td><td colspan="26">CUSTOMER_ID</td></tr>
<tr><td>0x04 to 0x0F</td><td>N/A</td><td colspan="27">factory reserved</td></tr>
<tr><td>0x10</td><td>0x30</td><td>ECC</td><td colspan="4">D_TX_TC</td><td colspan="6">N/A</td><td>D_SLP_OSHT_RISE</td><td>D_SLP_OSHT_FALL</td><td>D_OUT_RTC_EN_PIN2</td><td>D_OUT_RTC_EN_PIN1</td><td>D_OUT_RTC_EN_PIN4</td><td>D_OUT_RTC_EN_PIN3</td><td>D_OUT_FTC_EN_PIN2</td><td>D_OUT_FTC_EN_PIN1</td><td>D_OUT_FTC_EN_PIN4</td><td>D_OUT_FTC_EN_PIN3</td><td colspan="3">D_OUT_RTC_SEL</td><td colspan="3">D_OUT_FTC_SEL</td></tr>
<tr><td>0x11</td><td>0x31</td><td>ECC</td><td>OGA_FILT_DIS</td><td colspan="12">OGT_X_GAIN_C</td><td colspan="13">OGT_X_OFFSET_C</td></tr>
<tr><td>0x12</td><td>0x32</td><td>ECC</td><td>OGA_ALL_DIS</td><td colspan="12">OGT_Y_GAIN_C</td><td colspan="13">OGT_Y_OFFSET_C</td></tr>
<tr><td>0x13</td><td>0x33</td><td>ECC</td><td>N/A</td><td colspan="4">N_AVG_CYCLES_OGA</td><td colspan="11">EHC_X_H2_PHASE</td><td colspan="10">EHC_X_H2_AMP</td></tr>
<tr><td>0x14</td><td>0x34</td><td>ECC</td><td>N/A</td><td colspan="2">N/A</td><td colspan="2">ASC_BW</td><td colspan="11">EHC_X_H3_PHASE</td><td colspan="10">EHC_X_H3_AMP</td></tr>
<tr><td>0x15</td><td>0x35</td><td>ECC</td><td colspan="4">FE_SENS_TRIM</td><td>AGS_EN</td><td colspan="11">EHC_X_H4_PHASE</td><td colspan="10">EHC_X_H4_AMP</td></tr>
<tr><td>0x16</td><td>0x36</td><td>ECC</td><td>SET_TO_ZERO</td><td colspan="2">AGS_ MAX_ ROOM</td><td colspan="2">AGS_ RANGE_ ROOM</td><td colspan="11">EHC_Y_H2_PHASE</td><td colspan="10">EHC_Y_H2_AMP</td></tr>
<tr><td>0x17</td><td>0x37</td><td>ECC</td><td>N/A</td><td>PIN2_PUSHPULL_EN</td><td>PIN1_PUSHPULL_EN</td><td colspan="2">SENT_ HYST_ CFG</td><td colspan="11">EHC_Y_H3_PHASE</td><td colspan="10">EHC_Y_H3_AMP</td></tr>
</table>

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

<table>
<tr><th rowspan="2">EEPROM Address</th><th rowspan="2">Shadow Address</th><th colspan="27">Bits</th></tr>
<tr><th>31:26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x18</td><td>0x38</td><td>ECC</td><td colspan="4">D_TX_CK_PH_TRIM</td><td>EHC_HARM_WEIGHT_EN</td><td colspan="11">EHC_Y_H4_PHASE</td><td colspan="10">EHC_Y_H4_AMP</td></tr>
<tr><td>0x19</td><td>0x39</td><td>ECC</td><td>OGA_OFF_DIS</td><td>OGA_AMP_DIS</td><td colspan="24">CUSTOMER_SCRATCH_0</td></tr>
<tr><td>0x1a</td><td>0x3a</td><td>ECC</td><td colspan="2">N/A</td><td colspan="24">CUSTOMER_SCRATCH_1</td></tr>
<tr><td>0x1b</td><td>0x3B</td><td>ECC</td><td>N/A</td><td colspan="10">ASC_QUAD_COMP</td><td colspan="3">INC_HYST</td><td colspan="2">INC_INTERPOL_RATE</td><td colspan="10">DEL_SYS_ABS</td></tr>
<tr><td>0x1c</td><td>0x3C</td><td>ECC</td><td colspan="7">TXDRV_TRIM</td><td>TCN_HYST_DIS</td><td>TCN_INIT</td><td colspan="16">DEL_ZERO_ANGLE</td><td>DEL_ANGLE_POL</td></tr>
<tr><td>0x1d</td><td>0x3D</td><td>ECC</td><td>CFG_NO_SAMPLE</td><td colspan="2">CFG_DEV_ID</td><td colspan="2">CFG_MAX_SENSOR</td><td colspan="2">TRIGGER_CFG</td><td>CFG_ZERO_SAMPLE</td><td>CFG_SLOT_SYNC</td><td>CFG_SLOT_MARKING</td><td>CFG_POR_OFFLINE</td><td>SENT_CRC_CFG</td><td colspan="2">SENT_ SCN_ CFG</td><td colspan="4">SENT_DATA_CFG</td><td colspan="5">SENT_RATE</td><td colspan="3">OUTMSG_MODE</td></tr>
<tr><td>0x1e</td><td>0x3E</td><td>ECC</td><td>SENT_EMSG_SMSG_N</td><td>INC_COUNTUP_EN</td><td colspan="3">PWM_PORCH_ SEL</td><td colspan="4">PWM_PERIOD</td><td colspan="2">ABI_ INDEX_ MODE</td><td colspan="6">ABI_SLEW_INC_PULSE</td><td colspan="4">ABI_INC_RESOLU- TION</td><td>ABI_INVERT_OUT_EN</td><td colspan="2">CFG_SPCMIN_ADJ</td><td>CFG_FSAMPLE_ADR</td><td>CFG_IDLE_SYNC</td></tr>
<tr><td>0x1f</td><td>0x3F</td><td>ECC</td><td>N/A</td><td>BLOCK_VOLATILE_OUTPUT</td><td colspan="4">MEM_LOCK</td><td>ASIL_EN</td><td>INC_MODE_PLS0_EDG1</td><td>INC_ENABLE</td><td colspan="12">MANUFACTURER_CODE</td><td colspan="2">N/A</td><td colspan="2">DIG_OUT_MODE_C</td><td>PIN1_PWM1_SENT0</td></tr>
</table>

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

EEPROM

Address 0x0

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				FACTORY_DIE_ID																factory reserved					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FACTORY_ID [21:6]:
Identification number. When used in combination with FACTORY_LOT and FACTORY_WAFER create a unique identification for device traceability. The register access is customer read only.

Address 0x1

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				FACTORY_LOT																FACTORY_WAFER					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FACTORY_LOT [21:6]:
Identification number. When used in combination with FACTORY_ID and FACTORY_WAFER create a unique identification for device traceability. The register access is customer read only.

FACTORY_WAFER [5:0]:
Identification number. When used in combination with FACTORY_ID and FACTORY_LOT create a unique identification for device traceability. The register access is customer read only.

Address 0x2

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAS_ID																factory reserved									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CAS_ID [25:10]:
Type identification number. May contain an identification number to distinguish a specific device configuration. The register access is customer read only.

Address 0x3

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOMER_ID																									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CUSTOMER_ID [25:0]:
Customer identification number. The register space is open for customer write access. The contents of the register have no effect on the device operating modes. A common use for the register is to store a unique identification number written by the customer. The register access is customer read and write.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x10

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D_TX_TC				N/A						D_SLP_OSHT_RISE	D_SLP_OSHT_FALL	D_OUT_RTC_EN_PIN2	D_OUT_RTC_EN_PIN1	D_OUT_RTC_EN_PIN4	D_OUT_RTC_EN_PIN3	D_OUT_FTC_EN_PIN2	D_OUT_FTC_EN_PIN1	D_OUT_FTC_EN_PIN4	D_OUT_FTC_EN_PIN3	D_OUT_RTC_SEL			D_OUT_FTC_SEL		
Default	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

D_TX_TC [25:22]:
Determines temperature coefficient for transmitting current adjustment.

D_TX_TC (CODE)	TX_{TC} (°C^{-1})
8	5.70×10^{-5}
9	5.46×10^{-4}
10	1.02×10^{-3}
11	1.49×10^{-3}
12	1.94×10^{-3}
13	2.39×10^{-3}
14	2.82×10^{-3}
15	3.24×10^{-3}
0	3.66×10^{-3}
1	4.06×10^{-3}
2	4.46×10^{-3}
3	4.85×10^{-3}
4	5.23×10^{-3}
5	5.60×10^{-3}
6	5.96×10^{-3}
7	6.32×10^{-3}

D_SLP_OSHT_RISE [15]:
Disables (0) or enables (1) one shot rise time control.

D_SLP_OSHT_FALL [14]:
Disables (0) or enables (1) one shot fall time control.

D_OUT_RTC_EN_PIN2 [13]:
Disables (0) or enables (1) rise time control on pin 2.

D_OUT_RTC_EN_PIN1 [12]:
Disables (0) or enables (1) rise time control on pin 1.

D_OUT_RTC_EN_PIN4 [11]:
Disables (0) or enables (1) rise time control on pin 4.

D_OUT_RTC_EN_PIN3 [10]:
Disables (0) or enables (1) rise time control on pin 3.

D_OUT_FTC_EN_PIN2 [9]:
Disables (0) or enables (1) fall time control on pin 2.

D_OUT_FTC_EN_PIN1 [8]:
Disables (0) or enables (1) fall time control on pin 1.

D_OUT_FTC_EN_PIN4 [7]:
Disables (0) or enables (1) fall time control on pin 4.

D_OUT_FTC_EN_PIN3 [6]:
Disables (0) or enables (1) fall time control on pin 3.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x11

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OGA_FILT_DIS	OGT_X_GAIN_C												OGT_X_OFFSET_C												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

OGA_FILT_DIS [25]:
Disables filtering in OGA correction update.

OGT_X_GAIN_C [24:13]:
Gain correction coefficient for x digital channel (RX2), represented in 12-bit signed fixed-point number with 13-bit fractional length. It can compensate ±25% gain mismatch with steps of 0.0122%.

OGT_X_OFFSET_C [12:0]:
Offset correction for x digital channel (RX2), represented in 13-bit signed fixed-point number with 16-bit fractional length. It can compensate ±6.25% ADC range at minimum AGS gain with steps of 0.001526%.

Address 0x12

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OGA_ALL_DIS	OGT_Y_GAIN_C												OGT_Y_OFFSET_C												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

OGA_ALL_DIS [25]:
Disable Offset Autocalibration algorithm.

OGT_Y_GAIN_C [24:13]:
Gain correction coefficient for y digital channel (RX1), represented in 12-bit signed fixed-point number with 13-bit fractional length. It can compensate ±25% gain mismatch with step of 0.0122%.

OGT_Y_OFFSET_C [12:0]:
Offset correction for y digital channel (RX1), represented in 13-bit signed fixed-point number with 16-bit fractional length. It can compensate ±6.25% ADC range at minimum AGS gain with steps of 0.001526%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x13

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A	N_AVG_CYCLES_OGA				EHC_X_H2_PHASE											EHC_X_H2_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

N_AVG_CYCLES_OGA [24:21]:
Number of electrical cycles for offset autocalibration algorithm. Code 0 corresponds to value of 16. Value shall be set to be largest multiple of number of target teeth and sensor periods ≤ 16, according to table below.

Number of target teeth/ sensor electrical periods	N_AVG_CYCLES_OGA (code)
1	0
2	0
3	15
4	0
5	15
6	12
7	14
8	0
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	0

EHC_X_H2_PHASE [20:10]:
Phase value of 2nd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H2_AMP [9:0]:
Amplitude value of 2nd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x14

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	n/a	n/a		ASC_BW		EHC_X_H3_PHASE											EHC_X_H3_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ASC_BW [22:21]:
Sets bandwidth for angle and speed calculation control loop. It should be set to 0 for all ASIL applications.

ASC_BW	–3 dB BW (kHz)
0	1.19
1	1.95
2	4.97
3	8.54

EHC_X_H3_PHASE [20:10]:
Phase value of 3^{rd} electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H3_AMP [9:0]:
Amplitude value of 3^{rd} electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Address 0x15

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_SENS_TRIM				AGS_EN	EHC_X_H4_PHASE											EHC_X_H4_AMP									
Default	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

FE_SENS_TRIM [25:22]:
It sets the gain of front-end amplifier if automatic gain adjustment is disabled (AGS_EN = 0).

Value	FE Amplifier Gain (V/V)
0	8
1	16
2	24
3	32
4	40
5	48
6	56
7	64
8	72
9	80
10	88
11	96
12	104
13	112
14	120
15	128

AGS_EN [21]:
Enables automatic gain control (AGS) algorithm to determine optimal front-end gain at start-up. When clear, front-end gain is determined by FE_SENS_TRIM value.

EHC_X_H4_PHASE [20:10]:
Phase value of 4th electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H4_AMP [9:0]:
Amplitude value of 4th electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x16

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SET_TO_ZERO	AGS_MAX_ROOM		AGS_RANGE_ROOM		EHC_Y_H2_PHASE											EHC_Y_H2_AMP									
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

SET_TO_ZERO [25]:

Should always be set to 0 for correct TX drive operations.

AGS_MAX_ROOM [24:23]:

Reduces the used input range for the front-end ADC to give room for offset or mechanical input modulation. Value is used in AGS algorithm to determine optimal FE gain.

Value	ADC input room
0	0 mV
1	5 mV
2	15 mV
3	20 mV

AGS_RANGE_ROOM [22:21]:

Reduces the used input range of the front-end ADC. Value is used in AGS algorithm to determine optimal FE gain.

Value	ADC input range reduction
0	0%
1	10%
2	15%
3	20%

EHC_Y_H2_PHASE [20:10]:

Phase value of 2^{nd} electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H2_AMP [9:0]:

Amplitude value of 2^{nd} electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x17

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED	PIN2_PUSHPULL_EN	PIN1_PUSHPULL_EN	SENT_HYST_CFG		EHC_Y_H3_PHASE											EHC_Y_H3_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PIN2_PUSHPULL_EN [24]:
Sets the output type for pin-2. 0: open-drain; 1: push-pull.

PIN1_PUSHPULL_EN [23]:
Sets the output type for pin-1. 0: open-drain; 1: push-pull.

SENT_HYST_CFG [22:21]:
SENT Trigger Threshold Hysteresis configuration. Corresponding threshold values are indicated in SENT description.

EHC_Y_H3_PHASE [20:10]:
Phase value of 3rd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H3_AMP [9:0]:
Amplitude value of 3rd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x18

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D_TX_CK_PH_TRIM				EHC_HARM_WEIGHT_EN	EHC_Y_H4_PHASE											EHC_Y_H4_AMP									
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

D_TX_CK_PH_TRIM [25:22]:
Modifies demodulation clock phase. Value is represented as signed integer on 4 bits, coded in 2's complement. Code 8 corresponds to minimum value (–8), and code 7 corresponds to maximum value (+7). Value shall be adjusted according to the operating coil drive frequency to maximize input signal amplitude after demodulation scheme. Figure 58 indicates nominal value for optimal trim depending on frequency and input phase delay of RX signals with respect to TX signal.

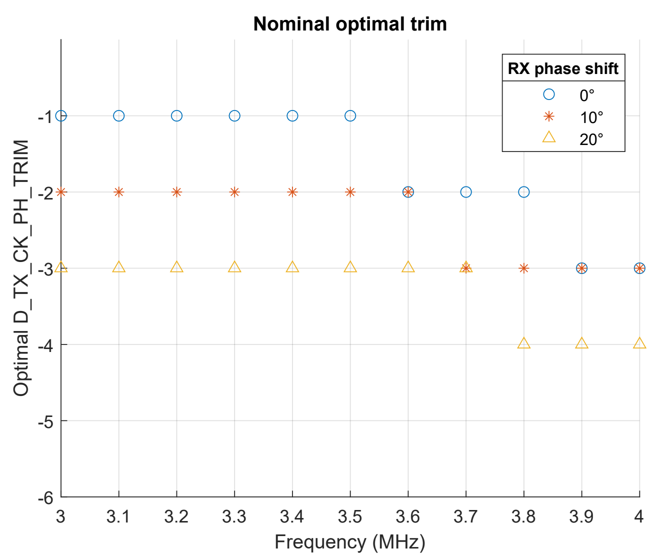


Figure 58

Oscillator frequency check (OFE) safety mechanism will flag error depending on coil drive frequency and demodulation clock trim in use. A safe operating area with no OFE flag is illustrated in Figure 59. For safety operations, it is recommended to select the trim considering the maximum coil drive frequency that might occur in sensor operations considering components and mechanical tolerances.

Coil Drive Frequency	Maximum D_TX_CK_PH_TRIM code with no OFE flag
3.0 MHz	2
3.5 MHz	–1
4.0 MHz	–3

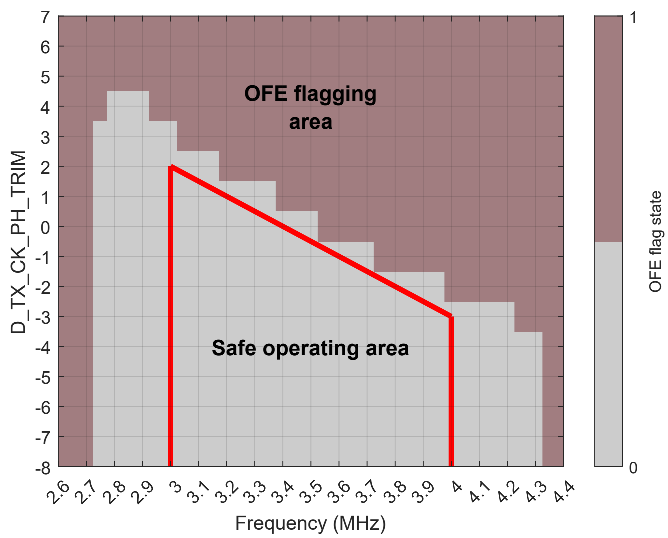


Figure 59

EHC_HARM_WEIGHT_EN [21]:

Enables electrical harmonic compensations term scaling with input amplitude. Should be kept to 1 for normal operation.

EHC_Y_H4_PHASE [20:10]:

Phase value of 4th electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H4_AMP [9:0]:

Amplitude value of 4th electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x19

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OGA_OFF_DIS	OGA_AMP_DIS	CUSTOMER SENSOR ID #1												CUSTOMER SENSOR ID #2											
Default	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

OGA_OFF_DIS [25]:

If set, disables Offset compensation in Offset Autocalibration algorithm. It shall be kept to 0 for correct operation.

OGA_AMP_DIS [24]:

Bit shall be set to 1 for correct operation.

CUSTOMER SENSOR ID #1 [23:12]:

CUSTOMER SENSOR ID #2 [11:0]:

Available fields for customer identification purposes.

In SENT output mode, when short serial message or enhanced serial message are enabled, the content of the fields is streamed in message data.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1A

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED		CUSTOMER SENSOR ID #3												CUSTOMER SENSOR ID #4											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CUSTOMER SENSOR ID #3 [23:12]:
CUSTOMER SENSOR ID #4 [11:0]:
Available fields for customer identification purposes.
In SENT output mode, when short serial message or enhanced serial message are enabled, the content of the fields is streamed in message data.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1B

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED	ASC_QUAD_COMP										INC_HYST			INC_INTERPOL_RATE		DEL_SYS_ABS									
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ASC_QUAD_COMP [24:15]:
Compensates deviation from quadrature between y (RX1) and x (RX2) digital channels before angle calculation. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate ±11.25 degrees with steps of 0.022 degrees.

INC_HYST [14:12]:
Angle Hysteresis threshold applied to the angle for ABI and motorSENT incremental output protocols. Value is 16-bit resolution. Provides ≈0.01 to 1.41° of hysteresis. Hysteresis behavior is described in ABI section. Default EEPROM value is 4, corresponding to 0.176° of hysteresis.

$\text{Hysteresis} = 360° / 2^{(15\text{-INC\_HYST})}$

Code	Value
0	0.01° of Hysteresis
1	0.02° of Hysteresis
…	…
7	1.41° of Hysteresis

INC_INTERPOL_RATE [11:10]:
Configure interpolation rate for motorSENT incremental output and ABI. 1st order or linear interpolation of the angle is performed between actual and previous angle samples, and resulting output has an update rate of 1 MHz × Interpolation rate. Interpolation rate is configured as $2^{\text{INC\_INTERPOL\_RATE}}$, so 1, 2, 4, and 8 MHz outputs are possible (with 1 MHz case being no interpolation).

Interpolation does not apply to SENT frame angle data.

Value	Description
0	1 MHz (no interpolation)
1	2 MHz interpolation
2	4 MHz interpolation
3	8 MHz interpolation

DEL_SYS_ABS [9:0]:
Additional system delay to be used for delay compensation when calculating angle. Value is represented in 10-bit signed number. It can compensate ± 256 µs with steps of 0.5 µs.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1C

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXDRV_TRIM							TCN_HYST_DIS	TCN_INIT	DEL_ZERO_ANGLE																DEL_ANGLE_POL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

TXDRV_TRIM [25:19]:
Sets tail current for transmitting oscillator according to table below. Resulting oscillation amplitude depends on external LC tank circuit characteristics: amplitude increasing from value 0 (minimum amplitude) to 127 (maximum amplitude).

TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)	TXDRV_ TRIM	I_{TX} (mA)
0	0.125	20	0.280	40	0.552	60	1.010	80	2.203	100	4.078	120	8.116
1	0.131	21	0.287	41	0.571	61	1.029	81	2.257	101	4.240	121	8.276
2	0.137	22	0.293	42	0.589	62	1.047	82	2.312	102	4.402	122	8.438
3	0.144	23	0.299	43	0.607	63	1.065	83	2.366	103	4.564	123	8.598
4	0.156	24	0.311	44	0.644	64	1.104	84	2.476	104	4.888	124	8.919
5	0.162	25	0.318	45	0.662	65	1.159	85	2.531	105	5.050	125	9.079
6	0.169	26	0.324	46	0.681	66	1.214	86	2.586	106	5.212	126	9.240
7	0.175	27	0.330	47	0.699	67	1.269	87	2.641	107	5.374	127	9.400
8	0.187	28	0.343	48	0.736	68	1.379	88	2.750	108	5.697		
9	0.193	29	0.349	49	0.754	69	1.434	89	2.805	109	5.859		
10	0.200	30	0.355	50	0.772	70	1.488	90	2.859	110	6.021		
11	0.206	31	0.361	51	0.791	71	1.543	91	2.914	111	6.182		
12	0.218	32	0.369	52	0.827	72	1.653	92	3.023	112	6.505		
13	0.225	33	0.387	53	0.846	73	1.708	93	3.078	113	6.666		
14	0.231	34	0.405	54	0.864	74	1.763	94	3.133	114	6.827		
15	0.237	35	0.424	55	0.882	75	1.818	95	3.188	115	6.989		
16	0.249	36	0.461	56	0.919	76	1.928	96	3.266	116	7.311		
17	0.256	37	0.479	57	0.937	77	1.983	97	3.428	117	7.472		
18	0.262	38	0.497	58	0.955	78	2.038	98	3.591	118	7.634		
19	0.268	39	0.516	59	0.974	79	2.093	99	3.753	119	7.794		

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TCN_HYST_DIS [18]:
Disables Turns count hysteresis.

TCN_INIT [17]:
Turns count initialization selection. Defines the initial value of the Turns count after a power reset event.

Value	Description
0	Turns count initialized to a value of 0.
1	Turns count initialized to a value based on the initial angle reading. 0 ≤ angle < 90 degrees = 0 90 ≤ angle < 180 degrees = 1 180 ≤ angle < 270 degrees = 2 270 ≤ angle < 360 degrees = 3

DEL_ZERO_ANGLE [16:1]:
Offsets the output angle of a value between 0 and 360 degrees in 65536 steps. Angle output is equal to calculated angle plus DEL_ZERO_ANGLE × 360/65536.

DEL_ANGLE_POL [0]:
Defines the angle polarity. 0: Forward, increasing angle when x (RX2 envelop) leads y (RX1 envelop). 1. Reversed polarity, angle decreasing when x (RX2 envelop) leads y (RX1 envelop).

Address 0x1D

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_NO_SAMPLE	CFG_DEV_ID		CFG_MAX_SENSOR		TRIGGER_CFG		CFG_ZERO_SAMPLE	CFG_SLOT_SYNC	CFG_SLOT_MARKING	CFG_POR_OFFLINE	SENT_CRC_CFG	SENT_SCN_CFG		SENT_DATA_CFG				SENT_RATE					OUTMSG_MODE		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CFG_NO_SAMPLE [25]:
If 1, the F_SAMPLE does not create a SSQ_SAMPLE_HOLD request.

CFG_DEV_ID [24:23]:
Device ID for SSENT and ASENT.

CFG_MAX_SENSOR [22:21]:
Highest device number on the bus for SSENT

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TRIGGER_CFG [20:19]:
Defines the minimum duration of the pulse to trigger a SENT frame from the IC in TSENT mode. The external controller initiates a trigger pulse by holding the output pin low.

TRIGGER_CFG	Duration
0	2.5 µs
1	5 µs
2	10 µs
3	0.5 µs

CFG_ZERO_SAMPLE [18]:
If 1 for SSENT, a SAMPLE_AND_HOLD is requested when the slot counter is 0.

CFG_SLOT_SYNC [17]:
If 1 for SSENT and CFG_SLOT_MARKING = 1, then the sequencer uses the slot marking to synchronize the slot counter.

CFG_SLOT_MARKING [16]:
If 1 for SSENT, the slot marking times is applied prior to the start of a frame.

NOTE: If this is enabled for SSENT, the SEN_DELAY input has no effect on delaying the SSQ_GO.

CFG_POR_OFFLINE [15]:
If 1, the sensor is in OFFLINE mode following a power-on-reset (but not a reset that is not also power-on).

SENT_CRC_CFG [14]:
Includes the SCN nibble in the CRC calculations when set.

SENT_SCN_CFG [13:12]:
Configure the content of Status and Communication Nibble (SCN).

SENT_SCN_CFG	Bit 3	Bit 2	Bit 1	Bit 0
0	SerialSync	SerialData	S1	S0
1	0	0	S1	S0
2	ID[1]	ID[0]	S1	S0
3	0	0	0	0

SENT_DATA_CFG [11:8]:
Determines the data nibble format and content as described in SENT description.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SENT_RATE [7:3]:
Defines Tick Time for SENT protocol.

Value	Tick Time (μs)
0	1
1	0.25
2	0.375
3	0.5
4	0.625
5	0.75
6	0.875
7	1.0
8	1.125
9	1.25
10	1.375
11	1.5
12	1.625
13	1.75
14	1.875
15	2.0
16	2.125
17	2.25
18	2.375
19	2.5
20	2.625
21	2.75
22	2.875
23	3.0
24	3.5
25	4.0
26	4.5
27	5.0
28	5.5
29	6.0
30	7.0
31	10.0

OUTMSG_MODE [2:0]:
Defines the SENT mode.

Value	Description
0	SENT Free Running Mode with no Pause Pulse
1	SENT Free Running Mode with Variable Pause Pulse
2	Trigger SENT External Asynchronous SCN Sampling
3	Sequential SENT Long Trigger Mode
4	Sequential SENT Short Trigger Mode
5	Addressable SENT
6	TSENT External Synchronous Falling Edge Sampling
7	SENT Free Running Mode with no Pause Pulse (same as 0)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1E

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENT_EMSG_SMSG_N	INC_COUNTUP_EN	PWM_PORCH_SEL			PWM_PERIOD				ABI_INDEX_MODE		ABI_SLEW_INC_PULSE						ABI_INC_RESOLUTION				ABI_INVERT_OUT_EN	CFG_SPCMIN_ADJ		CFG_FSAMPLE_ADR	CFG_IDLE_SYNC
Default A17803-S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Default A17803-M	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

SENT_EMSG_SMSG_N [25]:
Configures the serial message type for SENT protocol. 0**:** Short serial message, 1**:** Enhanced serial message.

INC_COUNTUP_EN [24]:
If set, when incremental motor SENT output is enabled, at startup the IC sends increments to count from zero to current angle.

PWM_PORCH_SEL [23:21]:
PWM output fixed low and high time selection. This parameter configures the fixed low and high time of the PWM output.

Value	PWM Low Clamp (% Duty Cycle)	PWM High Clamp (% Duty Cycle)
0	2	98
1	3	97
2	4	96
3	5	95
4	6	94
5	7	93
6	8	92
7	2	98

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PWM_PERIOD [20:17]:

PWM output period. Controls the period, or frequency, of the PWM output.

Value	Frequency (Hz)
0	125
1	167
2	250
3	333
4	500
5	667
6	800
7	1000
8	1333
9	1600
10	2000
11	2667
12	4000
13	5333
14	8000
15	16000

ABI_INDEX_MODE [16:15]:

Defines the width and placement of the “I” pulse in ABI.

Value	Description
0	“I” pulse is set only at 0° to +R
1	“I” pulse set between –R to +R
2	“I” pulse set between –R to +2R
3	“I” pulse set between –2R and +2R

ABI_SLEW_INC_PULSE [14:9]:

When ABI is enabled, it controls the slew rate of the ABI output.

ABI_SLEW_RATE	Slew Time (μs)
1	0.25
2	0.375
3	0.5
4	0.625
5	0.75
6	0.875
7	1
8	1.125
…	…
62	7.875
63	8

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

When incremental motorSENT output is enabled and pulse mode is selected, ABI_SLEW_INC_PULSE[11:9] controls the width of the pulse in CLOCK_CYCLES. Corresponding nominal duration values are reported in the table below.

ABI_SLEW_INC_PULSE[11:9]	T_{PULSE} (t_{clk})	T_{PULSE}
0	1	62.5 ns
1	2	125 ns
2	4	250 ns
3	8	500 ns
4	16	1 µs
5	24	1.5 µs
6	32	2 µs
7	48	3 µs

ABI_INC_RESOLUTION [8:5]:

When ABI is enabled, it defines the angle resolution for the ABI protocol as described in the table below.

ABI_INC_ RESOLUTION	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0	Reserved					
1	Reserved					
2 [1]	12	14	4096	16384	0.088	0.022
3 [1]	11	13	2048	8192	0.176	0.044
4 [1]	10	12	1024	4096	0.352	0.088
5 [1]	9	11	512	2048	0.703	0.176
6	8	10	256	1024	1.406	0.352
7	7	9	128	512	2.813	0.703
8	6	8	64	256	5.625	1.406
9	5	7	32	128	11.250	2.813
10	4	6	16	64	22.500	5.625
11	3	5	8	32	45.000	11.250
12	2	4	4	16	90.000	22.5
13	1	3	2	8	180.0	45.0
14	0	2	1	4	360.0	90.0
15	n/a	n/a	n/a	n/a	n/a	n/a

[1] Codes 2-5 could be affected by IC noise.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

When incremental motorSENT output is enabled, it defines the angle resolution for the incremental protocol as described in the table below.

Angular Resolution = 16 – ABI_INC_RESOLUTION.

$\Delta\theta = 360° / 2^{(16 - ABI\_INC\_RESOLUTION)}$.

ABI_INC_RESOLUTION	Δθ (degrees)	Angular resolution (bit)
0 [1]	0.005	16
1 [1]	0.011	15
2 [1]	0.022	14
3	0.044	13
4	0.088	12
5	0.176	11
6	0.352	10
7	0.703	9
8	1.406	8
9	2.813	7
10	5.625	6
11	11.25	5
12	22.5	4
13	45	3
14	90	2
15	180	1

[1] Code 0-2 could be affected by IC noise.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABI_INVERT_OUT_EN [4]:

Inverts ABI signals.

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0</td><td>ABI signals behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.
<table>
<tr><th>State Name</th><th>A</th><th>B</th></tr>
<tr><td>Q1</td><td>0</td><td>0</td></tr>
<tr><td>Q2</td><td>0</td><td>1</td></tr>
<tr><td>Q3</td><td>1</td><td>1</td></tr>
<tr><td>Q4</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>1</td><td>ABI signals are inverted and behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at ABI resolution.
<table>
<tr><th>State Name</th><th>A</th><th>B</th></tr>
<tr><td>Q1</td><td>1</td><td>1</td></tr>
<tr><td>Q2</td><td>1</td><td>0</td></tr>
<tr><td>Q3</td><td>0</td><td>0</td></tr>
<tr><td>Q4</td><td>0</td><td>1</td></tr>
</table></td></tr>
</table>

CFG_SPCMIN_ADJ [3:2]:

Determines minimum low time for detecting an SSENT SPC F_OUTPUT command. **0:** 7 ticks **1:** 8 ticks **2:** 9 ticks **3:** 10 ticks.

CFG_FSAMPLE_ADR [1]:

If 1, the F_SAMPLE is an addressing (frame request) as well as a SAMPLE_AND_HOLD request.

CFG_IDLE_SYNC [0]:

If 1 for SSENT, a bus idle time of > 510 ticks acts as an F_SYNC.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x1F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	n/a	BLOCK_VOLATILE_OUTPUT	MEM_LOCK				ASIL_EN	INC_MODE_PLS0_EDG1	INC_ENABLE	MANUFACTURER_CODE												n/a		DIG_OUT_MODE_C		PIN1_PWM1_SENT0
Default A17803-S	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Default A17803-M	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BLOCK_VOLATILE_OUTPUT [24]:

Controls write access to volatile memory. When set, write operations to volatile memory are disabled.

MEM_LOCK [23:20]:

Defines protection for memory access as described in EEPROM and Shadow Memory Usage.

ASIL_EN [19]:

Enables error reporting. It should be set for ASIL applications.

INC_MODE_PLS0_EDG1 [18]:

Defines incremental output type for motorSENT.

Value	Description
0	Pulse mode
1	Edge mode

INC_ENABLE [17]:

Enables incremental output for motorSENT on pin-3. For incremental output to be enabled, ABI should not be enabled (DIG_OUT_MODE_C should not be 0).

MANUFACTURER_CODE [16:5]:

Bits available for customer purposes.

DIG_OUT_MODE_C [2:1]:

Configures digital output protocols.

Value	Description
0	ABI enabled. A on pin 2, B on pin 3, I on pin 4.
1	PWM enabled on pin 2.
2	SENT enabled on pin 2.
3	No output on pin 2.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PIN1_ PWM1_SENT0 [0]:
Selects output protocol for pin-1. 0: SENT; 1: PWM.

VOLATILE MEMORY MAP

Address 0x42

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EE_DBE_FLAG	EE_SBE_FLAG	EE_ECC						EE_ADDR					EE_ERR_STATUS					CP_ERR	EE_ERR
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RC

EE_DBE_FLAG [19]:

Error flag indicates detection of an EEPROM dual-bit error. The EEPROM ECC logic detects an address with a dual-bit error. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM dual bit error detected
1	EEPROM dual bit error detected

EE_SBE_FLAG [18]:

Error flag indicates detection of an EEPROM single-bit error. The EEPROM ECC logic detects an address with a single-bit error. The ECC logic automatically corrects the faulty bit in the volatile region of memory. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM single-bit error detected
1	EEPROM single-bit error detected

EE_ECC [17:12]:

EEPROM ECC data. After the internal margin test is complete, this parameter contains the ECC data bits of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

EE_ADDR [11:7]:

EEPROM address data. After the internal margin test is complete, this parameter contains the address of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

EE_ERR_STATUS [6:2]:

Indicates the error status of the last EEPROM write. If logic > 0, an error was detected during the last EEPROM write.

CP_ERR [1]:

Indicates the error status of the EEPROM write charge pump during the last EEPROM write. If logic = 1, an error is detected, and the error is set in EE_ERR_STATUS (extended: 0x42 [6:2]).

EE_ERR [0]:

Indicates detection of an EEPROM write error. If logic = 1, an EEPROM write error is detected. The bit clears after read.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Address 0x43

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EE_DATA																									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EE_DATA [25:0]:
EEPROM field data. After the internal margin test is complete, this parameter contains information from the data fields of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

Address 0x44

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	EE_LOOP	EE_TEST_ADDR					EE_USE_TEST_ADDR	MARGIN_MIN_MAX_FAIL	MARGIN_STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RW	RW	RW

EE_LOOP [12]:
Continuously loops the margin test. When bit logic = 1, the margin test loops continuously. If an error is detected or if MARGIN_START (extended: 0x44 [0]) is cleared, the margin test stops.

Value	Description
0	Margin test runs once
1	Margin test loops continuously until an error is detected

EE_TEST_ADDR [11:7]:
Optional start address for margin test. Defines the starting address for the margin test when EE_USE_TEST_ADDR (extended: 0x44[6]) is set to logic = 1.

EE_USE_TEST_ADDR [6]:
When set to logic = 1, the margin test starts at the address defined by EE_TEST_ADDR (extended: 0x44 [12:7]).

Value	Description
0	Margin test starts at address 0x0
1	Margin test starts at address defined by EE_TEST_ADDR

MARGIN_MIN_MAX_FAIL [5]:
If a margin failure is detected, this bit indicates if the failure was detected at the minimum or maximum reference level.

Value	Description
0	Margin test failure detected at minimum threshold
1	Margin test failure detected at maximum threshold

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MARGIN_STATUS [4:3]:

Indicates the status of the margin test. The bits clear after a read or reset event.

Value	Description
0	Reset condition: No result from margin test
1	Pass: No errors detected during margin test
2	Fail: Error detected during margin test
3	In progress: Margin test still running

MARGIN_NO_MIN [2]:

Disables the minimum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the low reference level.

Value	Description
0	Margin test includes check at the low reference level
1	Margin test does not include check at the low reference level

MARGIN_NO_MAX [1]:

Disables the maximum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the high reference level.

Value	Description
0	Margin test includes check at the high reference level
1	Margin test does not include check at the high reference level

MARGIN_START [0]:

Triggers start of margin test. When set to LOGIC = 1, the margin test begins. The bit clears when the margin test completes and EE_LOOP (extended: 0x44 [13]) = 0; if EE_LOOP = 1, the margin test runs until MARGIN_START = 0. If the margin test detects an error, the MARGIN_START bit clears.

Address 0x44

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																								LBIST_ PASS1_FAIL0	BIST_DONE	BIST_START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RO	RW

LBIST_PASS1_FAIL0 [2]:

Indicates pass or fail result of LBIST (logic built-in self test).

Value	Description
0	Indicates a fail result from the LBIST
1	Indicates a pass result from the LBIST

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

BIST_DONE [1]:

Indicates BIST (built-in self test) is complete.

Value	Description
0	Indicates BIST is in progress, BIST did not execute, or BIST was aborted.
1	Indicates BIST is complete.

BIST_START [1]:

Initiates start of BIST. Bit is set to a logic value of one to initiate the start of LBIST. The bit self clears when LBIST is started. LBIST requires ≈105 ms to run. Angle is not available during LBIST.

Value	Description
0	Indicates LBIST is in progress or result not available.
1	Indicates BIST is complete.

Address 0x51

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																D_TX_AMP_TRIM							D_FE_SENS			
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

D_TX_AMP_TRIM [10:4]:

In use current trim code for oscillator driver.

D_FE_SENS [3:0]:

In use front-end gain code.

Address 0x5C

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_Y_OFFSET_COEFF																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_OFFSET_COEFF [17:0]:

Offset correction applied on y channel by offset autocalibration algorithm. Value is signed on 18 bit, with 18-bit fractional length.

Address 0x5E

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_X_OFFSET_COEFF																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_OFFSET_COEFF [17:0]:

Offset correction applied on x channel by offset autocalibration algorithm. Value is signed on 18 bit, with 18-bit fractional length.

Address 0x5F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_X_REF_AMPLITUDE																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_REF_AMPLITUDE [16:0]:
Calculated reference amplitude for y channel. Value is an unsigned integer on 17 bits, with 17-bit fractional length.

Address 0x60

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_X_REF_OFFSET																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_REF_OFFSET [17:0]:
Calculated reference offset for x channel. Value is a signed integer on 18 bits, with 17-bit fractional length.

Address 0x61

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_Y_REF_AMPLITUDE																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_REF_AMPLITUDE [16:0]:
Calculated reference amplitude for y channel. Value is an unsigned integer on 17 bits, with 17-bit fractional length.

Address 0x62

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_Y_REF_OFFSET																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_REF_OFFSET [17:0]:
Calculated reference offset for x channel. Value is a signed integer on 18 bits, with 17-bit fractional length.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

POWER DERATING

The A17803 must operate below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the A17803 to dissipate heat from the junction (die) through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 5$ V, $I_{CC} = 25$ mA, and $R_{\theta JA} = 82°C/W$, then:

$$P_D = V_{CC} \times I_{CC} = 125 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 125 \text{ mW} \times 82°C/W = 10.25°C$$

$$T_J = T_A + \Delta T = 25°C + 10.25°C = 35.25°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)} \times I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 160°C$, package LE.

Observe the case with a total current $I_{CC(tot)} = I_{CC(max)} + I_{CC(TX)} =$ 23 mA + 9 mA = 32 mA and the worst-case ratings for the device, specifically: $R_{\theta JA} = 82°C/W$, $T_{J(max)} = 175°C$, $V_{CC(max)} = 5.5$ V.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 175°C - 160°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 82°C/W = 183 \text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 183 \text{ mW} \div 32 \text{ mA} = 5.72 \text{ V}$$

The result indicates that, at T_A, the application and A17803 with a TX equivalent DC current of 9 mA can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$. TX currents larger than 9 mA might require power derating.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then a reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these condition.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

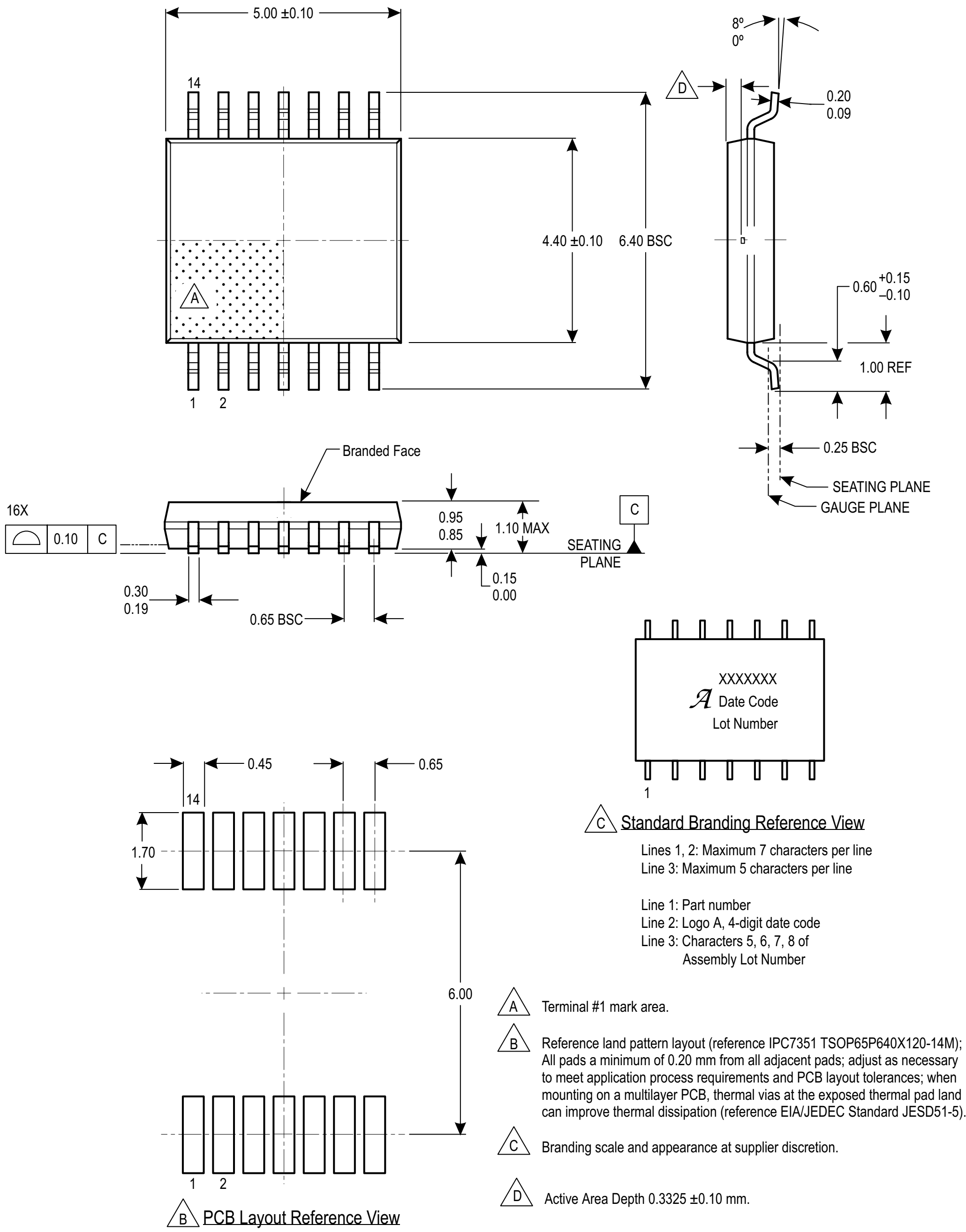


Figure 60: 14-Pin TSSOP Package

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	March 13, 2025	Initial release
1	April 22, 2025	Updated ASIL logo (page 1), Created short-form datasheet
2	January 9, 2026	Updated Functional Block Diagram (page 1), Operating Characteristics table (page 7, page 11), updated motorSENT table name (page 27), removed SPI Interface Timings Output table and updated Timing section (page 39), (pages 42, 43), added Programming Characteristics table (page 44), updated Read Command section (page 46), updated memory addresses (pages 49, 50), updated Address 0xF Temperature table and Temperature bit range (page 57), updated addresses and descriptions (page 87, 88)
3	February 6, 2026	Updated Supply Current characteristic (page 7); corrected OGA to offset autocalibration throughout; updated CRC Python code example (page 41); clarified t_d, t_b, and T_{BIT} references (pages 44-45); updated OGA_AMP_DIS default to 1 (page 70); and removed Address 0x5B and 0x5D (pages 87-88).
4	March 5, 2026	Updated footnote 5 and added footnote 7 (page 7); updated address bits EUE [12], ESE [11], and SME [10] descriptions (page 56); updated D_TX_CK_PH_TRIM [25:22] descriptions (pages 69-70); minor editorial updates.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com