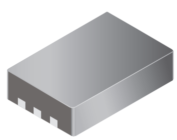
Low-Power Unidirectional Linear Hall-Effect Sensor IC
with User-Controlled Sleep Feature in Compact 2 mm × 3 mm Footprint

FEATURES AND BENEFITS

- User-controlled sleep mode with fast (< 60 µs) wakeup time for lag-free power savings
- 3.2 mA active and 25 µA sleep current reduces total power consumption and extends battery life
- Operates down to 2.5 V supply for battery applications
- Low quiescent voltage output (QVO) maximizes output range and resolution at ADC input
- Ambient temperature range from –20°C to 85°C suited for personal electronics and gaming applications

PACKAGE: 6-pin MLP/DFN (suffix EH)



Not to scale

DESCRIPTION

The A31010 family of linear Hall-effect sensor ICs provides a voltage output that is proportional to the applied magnetic field.

The user-controlled sleep pin and rapid wakeup time allows the A31010 to consume minimal power and provide magnetic data quickly after waking up. These features coupled with a low supply voltage rating of 2.5 V and non-ratiometric output make this IC ideal for battery-powered applications.

Many human machine interface (HMI) applications such as gaming controller joysticks, triggers, and keyboards will benefit from the sensor's unidirectional output.

These devices are available in a small 2 mm × 3 mm, 0.75 mm nominal height micro-leaded package (MLP/DFN). It is lead (Pb) free with 100% matte tin leadframe plating.

APPLICATIONS

- Game controllers
- Joysticks
- Triggers
- Personal electronics
- Keyboards
- Virtual and augmented reality devices
- Human-machine interfaces

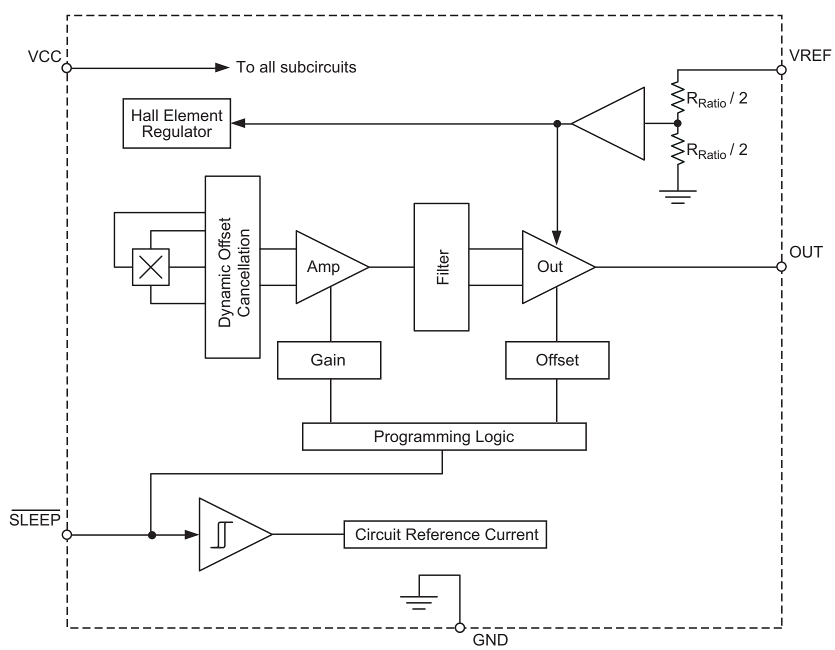


Figure 1: Functional Block Diagram

SELECTION GUIDE

Part Number	Typical Sensitivity (mV/G) [1]	QVO (% V_{REF})	Output Polarity	Full Scale Field (G) [1]	Package	Packing [2]
A31010SEHALT-4	3.78	6.47	Unidirectional	+650	DFN/MLP 2 mm × 3 mm; 0.75 mm nominal height	7-in. reel, 3000 pieces/reel
A31010SEHALT-10	10.0	6.47	Unidirectional	+250		

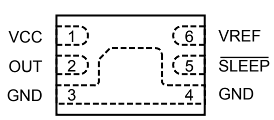
[1] At V_{CC} = V_{REF} = 3.0 V
[2] Contact Allegro for other packing options.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		7	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Reference Voltage	V_{REF}		7	V
Reverse Reference Voltage	V_{RREF}		–0.1	V
Logic Supply Voltage	V_{SLEEP}	V_{CC} > 2.5 V	32	V
Output Voltage	V_{OUT}		V_{CC} + 0.1	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

*All ratings with reference to ground

PINOUT DIAGRAM



TERMINAL LIST TABLE

Pin	Name	Function
1	VCC	Supply
2	OUT	Output
3	GND	Ground
4	GND	Ground
5	$\overline{\text{SLEEP}}$	Toggle sleep mode
6	VREF	Supply for ratiometric reference

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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

COMMON ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{CC} = 3.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}		2.5	3.0	3.5	V
Supply Current	I_{CC}	Active Mode	–	3.2	3.6	mA
Sleep Current	I_{CCS}	Sleep Mode	–	25	–	µA
Supply Zener Clamp Voltage	V_{CCZ}	I_{CC} = 7 mA	6	8.3	–	V
Supply Bypass Capacitor	C_{VCC}	Optional	–	100	–	nF
Output Capacitive Load	C_L		–	–	10	nF
Output Resistive Load	R_L		15	–	–	kΩ
Ratiometric Reference Voltage	V_{REF}		2.5	–	V_{CC}	V
Ratiometric Reference Zener Clamp Voltage	V_{REFZ}	I_{VREF} = 3 mA	6	8.3	–	V
Ratiometric Reference Input Resistance	R_{REF}	$V_{SLEEP} > V_{SH}$, $V_{CC} = V_{CC(TYP)}$	200	–	–	kΩ
		$V_{SLEEP} < V_{SL}$, $V_{CC} = V_{CC(TYP)}$	–	5	–	MΩ
$\overline{\text{SLEEP}}$ Input Voltage Range	V_{SLEEP}		–0.1	–	V_{CC} + 0.5	V
Power-On Time	t_{PO}	$V_{CC} > V_{CC(MIN)}$, $V_{SLEEP} > V_{SH}$, V_{CC} slew rate = 1 V/µs, C_L ≤ 10 nF, R_L ≥ 15 kΩ	–	40	60	µs
Internal Bandwidth	BW	Small signal –3 dB; $C_L \le C_{L(MAX)}$	–	10	–	kHz
Response Time	t_R		–	35	–	µs
Propagation Delay Time	t_P		–	5	–	µs
Rise Time	t_{RISE}		–	10	–	µs
Noise Density	B_{ND}	V_{CC} = 3.0 V Input Referred, T_A = 25°C	–	2.5	–	mG/√(Hz)
Noise	B_N	V_{CC} = 3.0 V Input Referred, T_A = 25°C	–	0.3	–	G_{RMS}
Linearity Sensitivity Error	E_{LIN}	Through Optimized Sensing Range (B_R)	–	1	–	%
Output Saturation Voltage	V_{SATH}	$V_{REF} \le V_{CC}$	–	V_{CC} – 0.1	–	V
	V_{SATL}	$V_{REF} \le V_{CC}$	–	0.1	–	V
Sensitivity Ratiometry Error	E_{SENSR}		–	0	–	%
QVO Ratiometry Error	E_{QVOR}		–	0	–	mV

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SLEEP MODE CHARACTERISTICS: Valid at T_A = 25°C, V_{CC} = 3.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
$\overline{SLEEP}$ Input Thresholds [1]	V_{SH}	$V_{SLEEP} > V_{SH}$ = Active Mode	–	0.45 × V_{CC}	–	V
	V_{SL}	$V_{SLEEP} < V_{SL}$ = Sleep Mode	–	0.2 × V_{CC}	–	V
$\overline{SLEEP}$ Input Current	I_{SLEEP}	$V_{SLEEP} < V_{SL}$ = Sleep Mode	–	10	–	nA
$\overline{SLEEP}$ Wakeup Time [2]	t_{WU}	$V_{SLEEP} > V_{SH}$, $V_{CC} > V_{CC(MIN)}$, $C_L \leq$ 10 nF, $R_L \geq$ 15 kΩ	–	40	60	µs
$\overline{SLEEP}$ Power Off Time [3]	t_{SLEEP}	$V_{SLEEP} < V_{SL}$, $V_{CC} > V_{CC(MIN)}$, $C_L \leq$ 10 nF, $R_L \geq$ 15 kΩ	–	1	–	µs

[1] Sleep mode is active low. When $\overline{SLEEP}$ pin is pulled below V_{SL}, the device will enter sleep mode and not respond to magnetic input.
[2] Includes sensor's response time. Device's output will be stable within $t_{WU(MAX)}$ after $V_{SLEEP} > V_{SH}$.
[3] $\overline{SLEEP}$ Power Off Time is the time between when $V_{SLEEP} < V_{SL}$ and I_{CC} < 100 µA.

A31010SEHALT-4 PERFORMANCE CHARACTERISTICS: Valid at T_A = 25°C, $V_{CC} = V_{REF}$ = 3.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Sensing Range [1]	B_R		0	–	650	G
Sensitivity	Sens		–	3.78	–	mV/G
Quiescent Output Voltage	QVO	B_{IN} = 0 G	–	6.47	–	%V_{REF}

[1] Parameter not measured at final test. Determined by design and characterization.

A31010SEHALT-10 PERFORMANCE CHARACTERISTICS: Valid at T_A = 25°C, $V_{CC} = V_{REF}$ = 3.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Sensing Range [1]	B_R		0	–	250	G
Sensitivity	Sens		–	10	–	mV/G
Quiescent Output Voltage	QVO	B_{IN} = 0 G	–	6.47	–	%V_{REF}

[1] Parameter not measured at final test. Determined by design and characterization.

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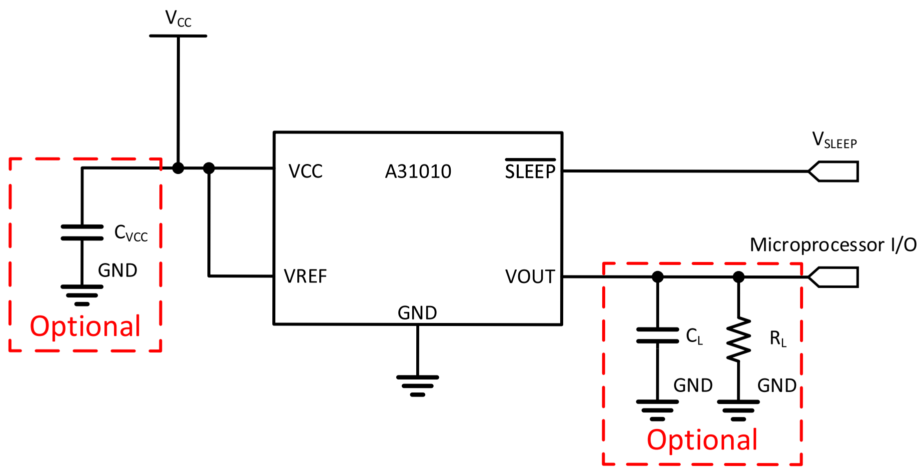

Figure 2: Example Application Circuit.
V_{SLEEP} may be controlled by a microprocessor I/O pin.

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APPLICATION INFORMATION

Sleep Mode

The A31010 is a low-power Hall-effect sensor IC that is perfect for power-sensitive customer applications. The current consumption of these devices is typically 3.2 mA, while the device is in active mode and less than 25 µA when the device is in sleep mode. Toggling the logic-level signal connected to the $\overline{\text{SLEEP}}$ pin drives the device into either active mode or sleep mode.

A logic-low sleep signal drives the device into sleep mode, and a logic-high sleep signal drives the device into active mode.

In cases when the VREF pin is powered before the VCC pin, the device will not operate within the specified limits until the supply voltage is equal to the reference voltage. When the device is switched from sleep mode to active mode, a time defined by t_{WU} must elapse before the output of the device is valid.

The device output transitions into the high-impedance state approximately t_{SLEEP} seconds after a logic-low signal is applied to the $\overline{\text{SLEEP}}$ pin (see Figure 3).

If possible, it is recommended to power-up the device in sleep mode. However, if the application requires that the device be powered-on in active mode, then a 10 kΩ resistor in series with the $\overline{\text{SLEEP}}$ pin is recommended. This resistor will limit the current that flows into the $\overline{\text{SLEEP}}$ pin if certain semiconductor junctions become forward-biased before the ramp-up of voltage on the VCC pin. Note that this current-limiting resistor is not required if the user connects the $\overline{\text{SLEEP}}$ pin directly to the VCC pin. The same precautions are advised if the device supply is powered-off while power is still applied to the $\overline{\text{SLEEP}}$ pin.

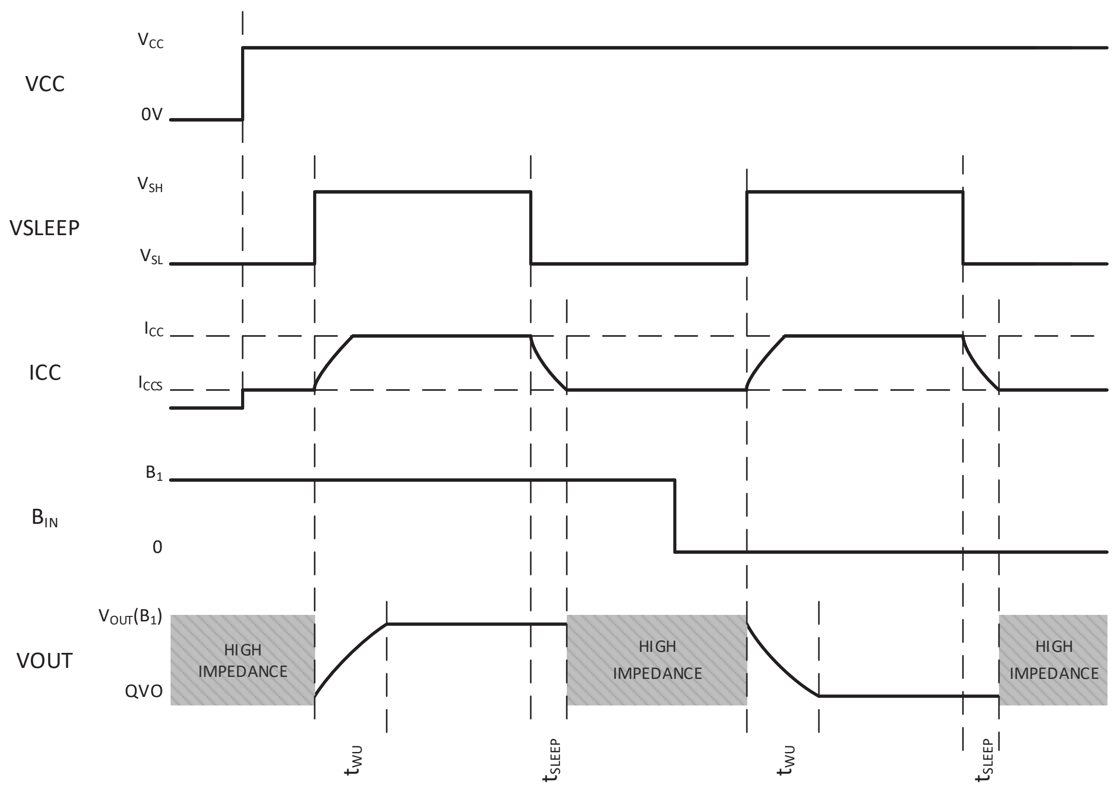

Figure 3: A31010 Timing Diagram

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CHARACTERISTIC DEFINITIONS

Ratiometry

A31010 devices feature a ratiometric output. The quiescent voltage output and sensitivity are proportional to the ratiometric supply reference voltage input at the VREF pin. The percent ratiometric change in the quiescent voltage output is defined as:

Equation 1:

$$\Delta QVO_{(\Delta \mathrm{VREF})} = \frac{QVO(VREF) \div QVO(3\mathrm{V})}{VREF \div 3\ \mathrm{V}} \times 100\%$$

And the error is defined as:

Equation 2:

$$E_{\mathrm{QVOR}} = \Delta QVO_{(\Delta \mathrm{VREF})} - 100\%$$

The percent ratiometric change in the sensitivity is defined as:

Equation 3:

$$\Delta Sens_{(\Delta \mathrm{VREF})} = \frac{Sens(VREF) \div Sens(3\mathrm{V})}{VREF \div 3\ \mathrm{V}} \times 100\%$$

And the error is defined as:

Equation 4:

$$E_{\mathrm{SENSR}} = \Delta Sens_{(\Delta \mathrm{VREF})} - 100\%$$

Linearity

The on-chip output stage is designed to provide a linear output with the maximum supply voltage of V_{CCN}. Although applications with very high magnetic fields will not damage these devices, it will force the output into a non-linear region. Linearity is measured and defined as:

Equation 5:

$$Lin = \frac{VOUT(B) - QVO}{2 \times (VOUT(\mathrm{B}/2)) - QVO} \times 100\%$$

And the error is defined as:

Equation 6:

$$E_{\mathrm{LIN}} = Lin - 100\%$$

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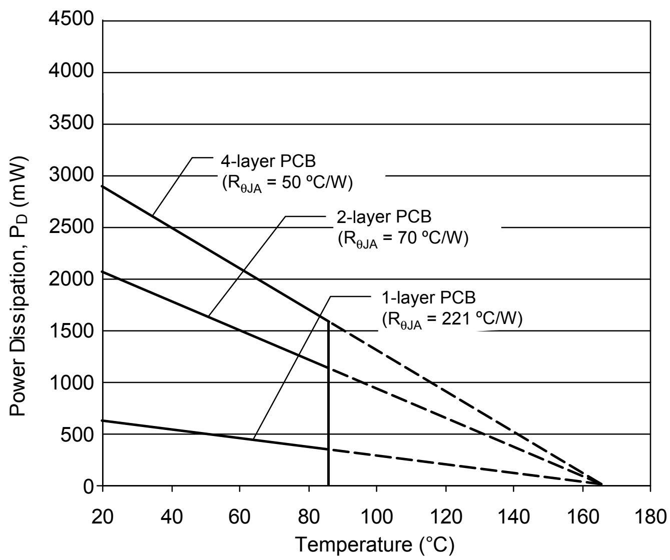
THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	221	°C/W
		2-layer PCB with 0.6 in.^{2} of copper area each side, connected by thermal vias	70	°C/W
		4-layer PCB based on JEDEC standard	50	°C/W

Power Dissipation versus Ambient Temperature



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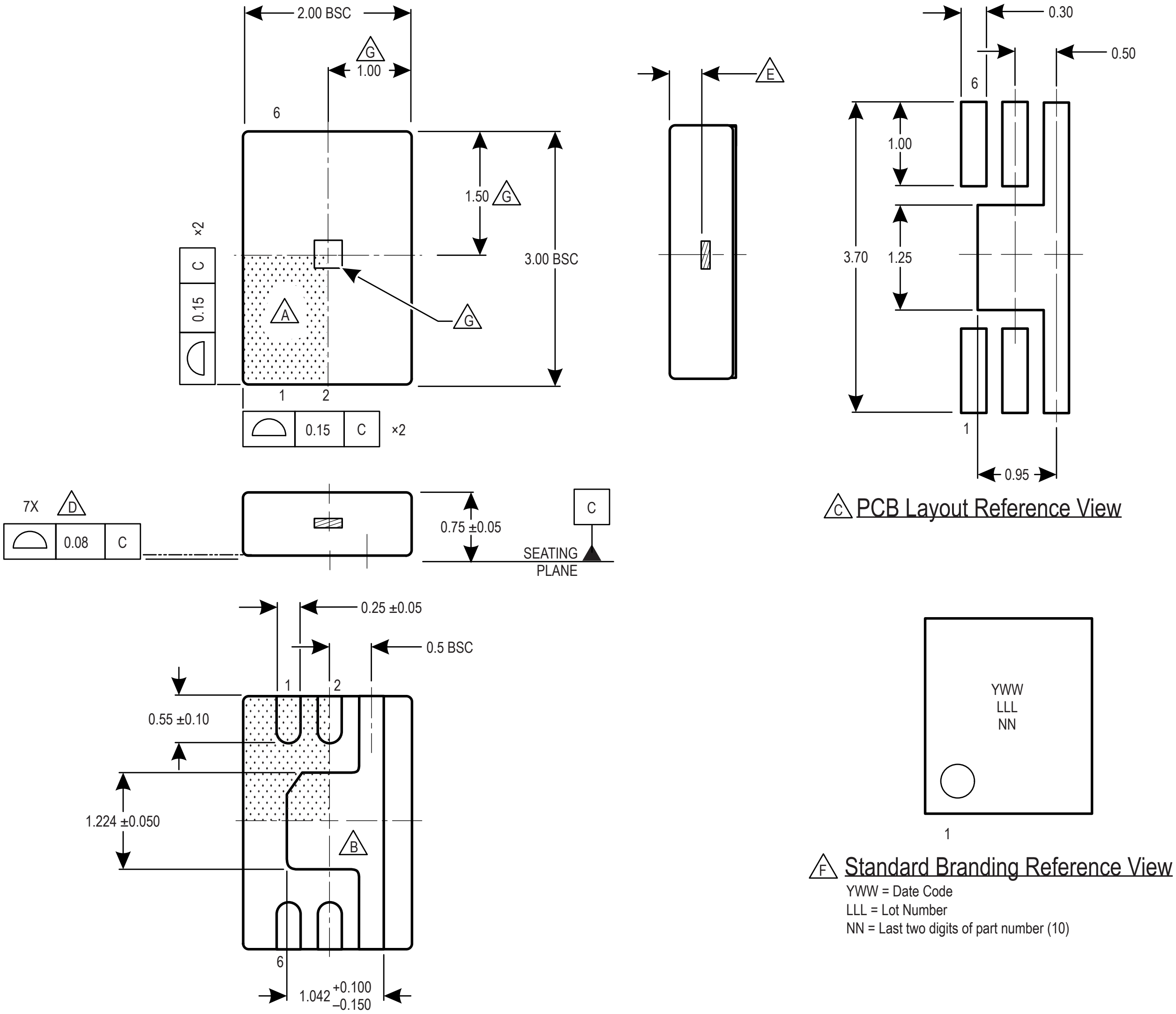
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000373)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A. Terminal #1 mark area

B. Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C. Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D. Coplanarity includes exposed thermal pad and terminals

E. Active Area Depth, 0.32 mm NOM

F. Branding scale and appearance at supplier discretion

G. Hall Element (not to scale); U.S. customary dimensions controlling

Figure 4: Package EH, 6-pin MLP/DFN

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Revision History

Number	Date	Description
–	September 2, 2021	Initial release
1	February 17, 2022	Updated product offerings

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