A31020

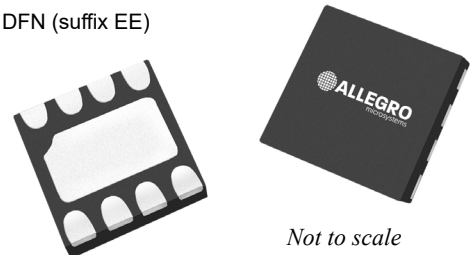
I²C Programmable Linear Hall IC

FEATURES AND BENEFITS

- Single supply with wide range: 1.6 to 3.6 V
- Low current consumption:
  - 2.3 mA active current (25°C, Z-axis)
  - 30 µA standby current (25°C)
  - 3 nA sleep current (25°C)
- Fast response time: <60 µs from standby to sample
- Configurable sleep timer for micropower operation
- Configurable sensing options:
  - Z-axis or X-axis sensing orientation
  - Configurable sensitivity (4 levels), polarity, quiescent output, and trigger threshold
  - Bipolar, omnipolar, and unipolar sensing options
- –40°C to 85°C operational ambient temperature
- I²C bus interface
  - Bit rate up to 1 Mbit/s with fast-mode plus (FM+)
- Pin for configurable sensor interrupt output
- Pin for optional user-timed sleep mode entry
- On-chip EEPROM for customer-configurable settings
- Low-profile and tiny size 8-pin DFN (2 mm × 2 mm)

PACKAGE

8-pin DFN (suffix EE)



Not to scale

DESCRIPTION

The A31020 linear Hall-effect sensor IC is a flexible magnetic sensor capable of measuring the raw field strength in either the Z-axis (perpendicular to the package) or X-axis (parallel to the package). The A31020 is highly customer-configurable with onboard EEPROM to store settings. The sensitivity, polarity, quiescent output, magnetic-field trigger threshold, and other settings are available for configuration.

The A31020 can be configured to operate in bipolar, unipolar, and omnipolar sensing modes, with different sensitivity and quiescent output options. The A31020 integrates a 12-bit analog-to-digital converter (ADC) to digitize the magnetic field measurement and to convert it to a digital output word.

Continued on next page...

APPLICATIONS

- Human-machine interface (HMI)
- Magnetic proximity sensors in factory applications
- Linear actuators
- Power tool triggers and button sensors
- Appliance buttons and closure detection
- E-meter anti-tampering detection
- Flow meter fluid measurement and valve closure detection
- Electronic smart locks
- Home security closure detection
- Game controller triggers and joysticks
- Virtual reality devices
- Keyboards

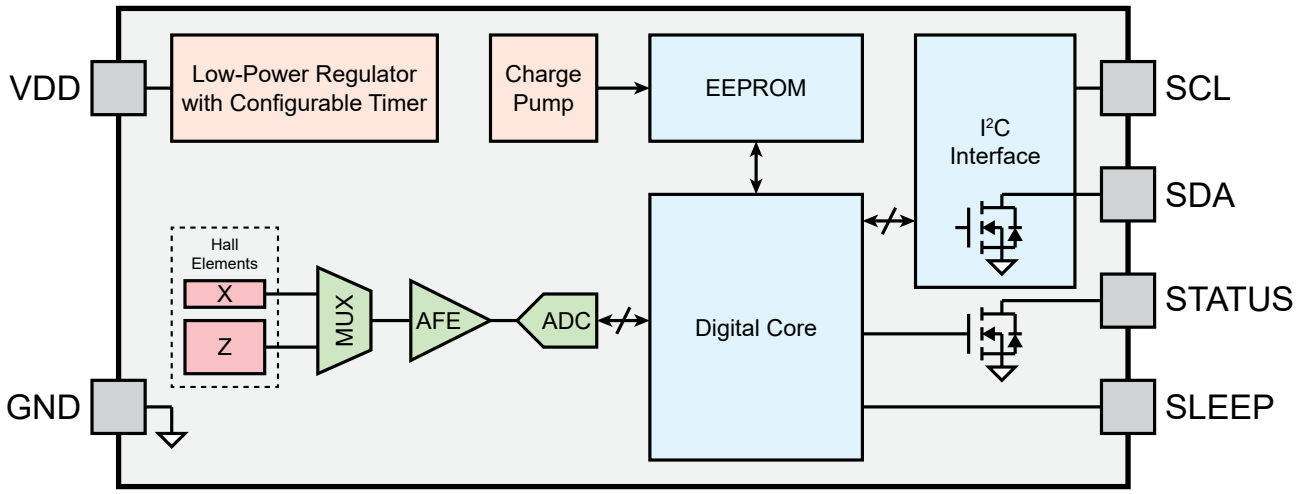


Figure 1: Functional Block Diagram

DESCRIPTION (continued)

The A31020 integrates an inter-integrated circuit (I²C) bus interface capable of up to 1 Mbit/s when using the fast-mode-plus feature (FM+).

Power management of the A31020 is highly configurable, allowing for system-level optimization of the supply current and performance. Sleep mode consumes just 3 nA typically (at 25°C), making the A31020 well suited for portable, battery-operated applications. Automatic micropower operation is supported to automatically duty-cycle between 30 µA of standby current and 2.3 mA of active current (at 25°C).

The A31020 is supplied in a 2 mm × 2 mm × 0.55 mm, 8-contact dual-flat no-leads (DFN) package (suffix EE). This small-footprint package lead (Pb) free with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	Sensing Axis	Package	Packing [1]
A31020EEEASR-Z	Z-Axis	EE (8-pin DFN)	13-inch Tape and Reel
A31020EEEASR-X	X-Axis		

[1] Contact Allegro for additional packing options.

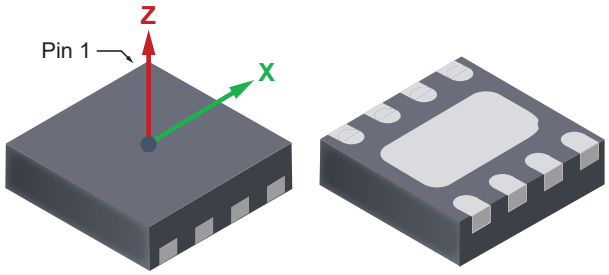


Figure 2: Sensing Axis Definition

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{DD}		3.7	V
Reverse Supply Voltage	V_{RDD}		–0.3	V
Forward I/O Voltage	–	Applies to SDA, SCL, STATUS, and SLEEP pins	V_{DD} + 0.3	V
Reverse I/O Voltage	–	Applies to SDA, SCL, STATUS, and SLEEP pins	–0.3	V
Operating Ambient Temperature Range	T_A	Range E	–40 to 85	°C
Junction Temperature	T_J		165	°C
Storage Temperature	T_{stg}		–65 to 150	°C
Applied Magnetic Field	B	Any axis	Unlimited	G
EEPROM Write Count [1]	–	Number of times EEPROM can be written	100	writes

[1] EEPROM writes are not supported above 85°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\Theta JA}$	4-layer PCB based on JEDEC standard	49	°C/W
		2-layer PCB with 0.23 in.^{2} exposed copper on each side	92	°C/W

[1] Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST TABLE

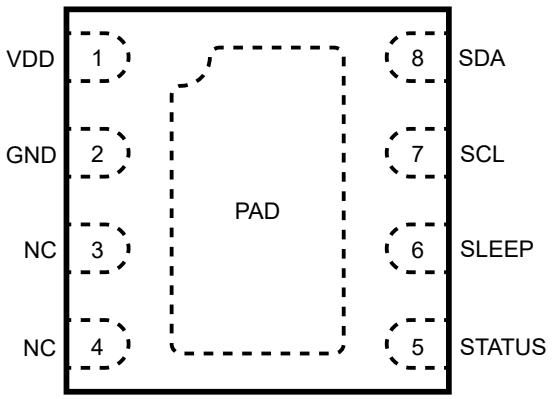

Figure 3: Pinout Diagram
(Top of Package)

Terminal List Table

Number	Name	Function
1	VDD	Supply voltage
2	GND	Ground reference
3	NC	No connect
4	NC	No connect
5	STATUS	Status signal output
6	SLEEP	Sleep control input
7	SCL	I²C clock
8	SDA	I²C data
–	PAD	Exposed pad for thermal dissipation, tie to GND

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TYPICAL APPLICATION CIRCUIT

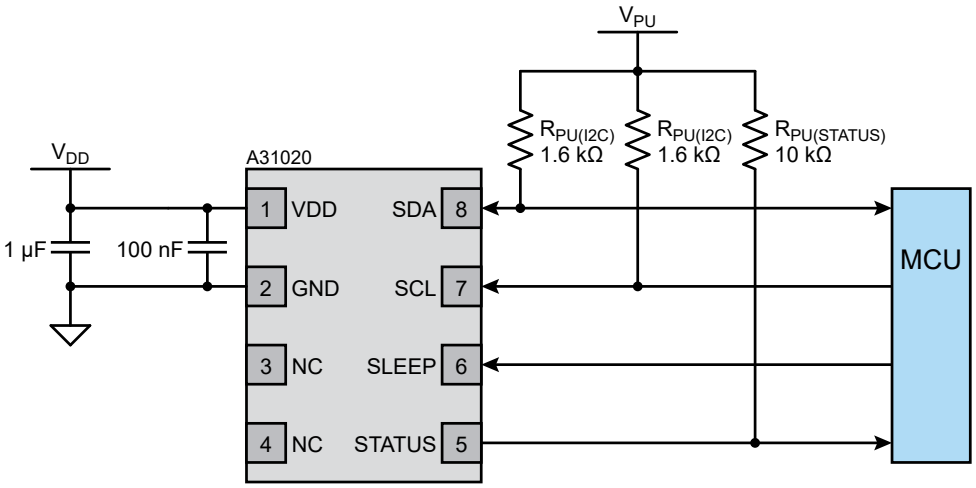

Figure 4: Typical Application Circuit

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ELECTRICAL CHARACTERISTICS: Valid through full operating voltage and temperature ranges unless otherwise specified [1]

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
Supply Voltage	V_{DD}			1.6	3.3	3.6	V
	$V_{DD(PROG)}$	For non-volatile memory programming		2.8	3.3	3.6	V
Supply Current [3]	$I_{DD(SLEEP)}$	Sleep State [4]	T_A = 25°C	–	3	7	nA
			T_A = 85°C	–	100	300	nA
	$I_{DD(STANDBY)}$	Standby State		–	30	40	µA
	$I_{DD(ACTIVE)}$	Active State	-X option (X-axis)	–	3.2	3.9	mA
		Active State	-Z option (Z-axis)	–	2.3	2.7	mA
Sleep Input Threshold [4][5]	V_{ACTIVE}	SLEEP pin voltage for active mode		–	–	40	$\%V_{DD}$
	V_{SLEEP}	SLEEP pin voltage for sleep/standby mode		60	–	–	$\%V_{DD}$
Pull-up Voltage	V_{PU}	On SDA, SCL, and STATUS pins		–	–	V_{DD} + 0.3	V
Pull-up Resistance [6]	$R_{PU(I2C)}$	On SDA and SCL pins		1.6	–	–	kΩ
	$R_{PU(STATUS)}$	On STATUS pin		10	–	–	kΩ
Input Capacitance	C_{IN}	Into SDA, SCL, SLEEP, and STATUS pins		–	–	10	pF
Input Current	I_{IN}	Into SDA, SCL, SLEEP, and STATUS pins		–1	–	1	µA
Drive Strength	$I_{SINK(SDA)}$	On SDA pin		–	–	20	mA
	$I_{SINK(STATUS)}$	On STATUS pin		–	–	5	mA
Response Time [4][7]	$t_{RESPONSE}$	T_A = 25°C; OSR_FILTER_ UPDATE = 1b0	IIR_EN = 1b1; BW_FLT_SEL = 3b000	–	2.1	–	ms
			IIR_EN = 1b0	–	60	–	µs

[1] Production tested at T_A = 25°C. Operating characteristics determined by design and characterization over full operating voltage and ambient temperature ranges unless otherwise specified.
[2] Typical values are for T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.
[3] V_{DD} = 3.3 V.
[4] Specification not measured at final test; determined by design and characterization.
[5] SLEEP pin is a high-impedance input.
[6] When implementing fast-mode plus (FM+) I²C operation, users must apply no greater than the minimum pull-up resistance specified. Users must evaluate if the system can support FM+ operation when using parallel devices loading the shared I²C bus.
[7] Time from transitioning to active state to Hall conversion (sample) ready. Response Time dependent on BW_FLT_SEL and OSR_FILTER_UPDATE settings. See Table 2 on page 16 for a detailed list of response times.

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MAGNETIC CHARACTERISTICS: Valid through full operating voltage and temperature ranges unless otherwise specified [1]

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
GENERAL MAGNETIC CHARACTERISTICS [3]							
Sensitivity Temperature Coefficient [4][5]	$SENS_{TC}$	D_MAG_TC = 2b00 (Flat)		–	0	–	%/°C
		D_MAG_TC = 2b01 (Ferrite)		–	0.2	–	%/°C
		D_MAG_TC = 2b10 (Neodymium)		–	0.12	–	%/°C
		D_MAG_TC = 2b11 (Samarium-Cobalt)		–	0.04	–	%/°C
Sensitivity Lifetime Drift [4]	–			–	0.5	–	%
Linearity Error [4][6]	ERR_{LIN}	Percentage of full-scale output (FSO)		–1.5	–	1.5	%FSO
Output Offset Error	ERR_{QO}	Percentage of full-scale output (FSO); T_A = 25°C; B = 0 G; V_{DD} = 3.3 V		–1.5	–	1.5	%FSO
Output Offset Temperature Drift [4][7]	ΔERR_{QO}	Relative to T_A = 25°C; B = 0 G; V_{DD} = 3.3 V	D_SENS_COARSE ≥ 2b01 (HF, MF, LF)	–12	–	12	G
			D_SENS_COARSE = 2b00 (VHF)	–20	–	20	G
Output Offset Lifetime Drift [4]	–			–	–0.01	–	%
Input Referred RMS Noise [4][7]	$N_{RMS(G)}$	-X option (X-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	0.11	–	G_{RMS}
			BW_FLT_SEL = 3b111	–	1.08	–	G_{RMS}
		-Z option (Z-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	0.135	–	G_{RMS}
			BW_FLT_SEL = 3b111	–	1.24	–	G_{RMS}
Effective Resolution [4][8]	ENOB	-X option (X-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	14.6	–	bits
			BW_FLT_SEL = 3b111	–	11	–	bits
		-Z option (Z-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	14	–	bits
			BW_FLT_SEL = 3b111	–	11	–	bits
Dynamic Range [4][9]	DR	-X option (X-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	85	–	dB
			BW_FLT_SEL = 3b111	–	65	–	dB
		-Z option (Z-Axis) D_SENS_COARSE = 2b00 (VHF)	BW_FLT_SEL = 3b000	–	83	–	dB
			BW_FLT_SEL = 3b111	–	64	–	dB

[1] Production tested at T_A = 25°C. Operating characteristics determined by design and characterization over full operating voltage and ambient temperature ranges unless otherwise specified.
[2] Typical values are for T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.
[3] IIR_EN = 1 and OSR_FLT_UPDATE = 0 unless otherwise specified.
[4] Specification not measured at final test; determined by design and characterization.
[5] Relative to sensitivity measured at T_A = 25°C.
[6] Valid when applied magnetic field is within the magnetic field input limits for the selected sensing mode. Linearity error is a percentage of the full-scale output range.
[7] 1 gauss (G) = 0.1 millitesla (mT).
[8] Calculated from the standard deviation of the noise (σ, in LSB) by: ENOB = ((20 × log(2^15 / σ) – 1.76) / 6.02.
[9] Calculated from the input-referred RMS noise ($N_{RMS(G)}$) and the maximum input signal (B_{MAX}) by: DR = 20 × log(B_{MAX} / $N_{RMS(G)}$).

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MAGNETIC CHARACTERISTICS (continued): Valid through full operating voltage and temperature ranges unless otherwise specified [1]

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
BIPOLAR MAGNETIC CHARACTERISTICS (OUT_MODE = 2b00) [3]							
Magnetic Field Input [4][5]	B	OFFSET_COARSE = 2b00 (25%)	D_SENS_COARSE = 2b00 (VHF)	–500	–	1500	G
			D_SENS_COARSE = 2b01 (HF)	–250	–	750	G
			D_SENS_COARSE = 2b10 (MF)	–125	–	375	G
			D_SENS_COARSE = 2b11 (LF)	–62.5	–	188	G
		OFFSET_COARSE = 2b01 or 2b10 (50%)	D_SENS_COARSE = 2b00 (VHF)	–2000	–	2000	G
			D_SENS_COARSE = 2b01 (HF)	–1000	–	1000	G
			D_SENS_COARSE = 2b10 (MF)	–500	–	500	G
			D_SENS_COARSE = 2b11 (LF)	–250	–	250	G
		OFFSET_COARSE = 2b11 (75%)	D_SENS_COARSE = 2b00 (VHF)	–1500	–	500	G
			D_SENS_COARSE = 2b01 (HF)	–750	–	250	G
			D_SENS_COARSE = 2b10 (MF)	–375	–	125	G
			D_SENS_COARSE = 2b11 (LF)	–188	–	62.5	G
Sensitivity [4][6]	SENS	OFFSET_COARSE = 2b01 or 2b10 (50%)	D_SENS_COARSE = 2b00 (VHF)	–	7.86	–	LSB/G
			D_SENS_COARSE = 2b01 (HF)	–	15.4	–	LSB/G
			D_SENS_COARSE = 2b10 (MF)	–	30.5	–	LSB/G
			D_SENS_COARSE = 2b11 (LF)	–	60.3	–	LSB/G
		OFFSET_COARSE = 2b00 or 2b11 (25% or 75%)	D_SENS_COARSE = 2b00 (VHF)	–	15.7	–	LSB/G
			D_SENS_COARSE = 2b01 (HF)	–	30.8	–	LSB/G
			D_SENS_COARSE = 2b10	–	61	–	LSB/G
			D_SENS_COARSE = 2b11	–	120	–	LSB/G
Quiescent Output [6]	QO	B = 0 G; OFFSET_COARSE = 2b00	POL = 0		8191		LSB
			POL = 1		24575		LSB
		B = 0 G; OFFSET_COARSE = 2b01 or 2b10	POL = 0		16383		LSB
			POL = 1		16383		LSB
		B = 0 G; OFFSET_COARSE = 2b11	POL = 0		24575		LSB
			POL = 1		8191		LSB

[1] Production tested at T_A = 25°C. Operating characteristics determined by design and characterization over full operating voltage and ambient temperature ranges unless otherwise specified.
[2] Typical values are for T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.
[3] IIR_EN = 1 unless otherwise specified.
[4] 1 gauss (G) = 0.1 millitesla (mT).
[5] Typical operating range. Actual range is slightly beyond the minimum and maximum values to ensure that the output range is inclusive of the typical operating magnetic range. Specification calculated from sensitivity, quiescent output, and output range (not measured at final test; determined by design and characterization).
[6] Specification not measured at final test; determined by design and characterization.

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MAGNETIC CHARACTERISTICS (continued): Valid through full operating voltage and temperature ranges unless otherwise specified [1]

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
UNIPOLAR SOUTH MAGNETIC CHARACTERISTICS (OUT_MODE = 2b01) [3]							
Magnetic Field Input [4][5]	B	D_SENS_COARSE = 2b00 (VHF)		0	–	2000	G
		D_SENS_COARSE = 2b01 (HF)		0	–	1000	G
		D_SENS_COARSE = 2b10 (MF)		0	–	500	G
		D_SENS_COARSE = 2b11 (LF)		0	–	250	G
Sensitivity [4][6]	SENS	D_SENS_COARSE = 2b00 (VHF)		–	15.4	–	LSB/G
		D_SENS_COARSE = 2b01 (HF)		–	30.5	–	LSB/G
		D_SENS_COARSE = 2b10 (MF)		–	60.3	–	LSB/G
		D_SENS_COARSE = 2b11 (LF)		–	121.2	–	LSB/G
Quiescent Output [6]	QO	B = 0 G	POL = 0	–	0	–	LSB
			POL = 1	–	32767	–	LSB
UNIPOLAR NORTH MAGNETIC CHARACTERISTICS (OUT_MODE = 2b10) [3]							
Magnetic Field Input [4][5]	B	D_SENS_COARSE = 2b00 (VHF)		–2000	–	0	G
		D_SENS_COARSE = 2b01 (HF)		–1000	–	0	G
		D_SENS_COARSE = 2b10 (MF)		–500	–	0	G
		D_SENS_COARSE = 2b11 (LF)		–250	–	0	G
Sensitivity [4][6]	SENS	D_SENS_COARSE = 2b00 (VHF)		–	15.4	–	LSB/G
		D_SENS_COARSE = 2b01 (HF)		–	30.5	–	LSB/G
		D_SENS_COARSE = 2b10 (MF)		–	60.3	–	LSB/G
		D_SENS_COARSE = 2b11 (LF)		–	121.2	–	LSB/G
Quiescent Output [6]	QO	B = 0 G	POL = 0	–	0	–	LSB
			POL = 1	–	32767	–	LSB
OMNIPOLAR MAGNETIC CHARACTERISTICS (OUT_MODE = 2b11) [3]							
Magnetic Field Input [4][5]	B	D_SENS_COARSE = 2b00 (VHF)		–2000	–	2000	G
		D_SENS_COARSE = 2b01 (HF)		–1000	–	1000	G
		D_SENS_COARSE = 2b10 (MF)		–500	–	500	G
		D_SENS_COARSE = 2b11 (LF)		–250	–	250	G
Sensitivity [4][6]	SENS	D_SENS_COARSE = 2b00 (VHF)		–	15.4	–	LSB/G
		D_SENS_COARSE = 2b01 (HF)		–	30.5	–	LSB/G
		D_SENS_COARSE = 2b10 (MF)		–	60.3	–	LSB/G
		D_SENS_COARSE = 2b11 (LF)		–	121.2	–	LSB/G
Quiescent Output [6]	QO	B = 0 G	POL = 0	–	0	–	LSB
			POL = 1	–	32767	–	LSB

[1] Production tested at T_A = 25°C. Operating characteristics determined by design and characterization over full operating voltage and ambient temperature ranges unless otherwise specified.
[2] Typical values are for T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.
[3] IIR_EN = 1 unless otherwise specified.
[4] 1 gauss (G) = 0.1 millitesla (mT).
[5] Typical operating range. Actual range is slightly beyond the minimum and maximum values to ensure that the output range is inclusive of the typical operating magnetic range. Specification calculated from sensitivity, quiescent output, and output range (not measured at final test; determined by design and characterization).
[6] Specifications measured at final test for D_SENS_COARSE = 2b01 and OFFSET_COARSE = 2b01. Other configurations not measured at final test; determined by design and characterization.

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I²C INTERFACE CHARACTERISTICS: Valid through full operating voltage and temperature ranges unless otherwise specified [1]

Characteristics	Symbol	Test Conditions	Min.	Typ. [2]	Max.	Unit
I²C TIMING CHARACTERISTICS						
Clock Frequency [3]	f_{CLK}		0.1	0.4	1	MHz
Bus Free Time Between Stop and Start	t_{BF}	f_{CLK} = 400 kHz	1.3	–	–	µs
		f_{CLK} = 1 MHz	0.5	–	–	µs
Data Hold Time	$t_{DAT(H)}$	f_{CLK} = 400 kHz	–	–	900	ns
		f_{CLK} = 1 MHz	–	–	450	ns
Start Condition Hold Time	$t_{STA(H)}$	f_{CLK} = 400 kHz	0.6	–	–	µs
		f_{CLK} = 1 MHz	0.26	–	–	µs
Setup Time for Repeated Start Condition	$t_{STA(S)}$	f_{CLK} = 400 kHz	0.6	–	–	µs
		f_{CLK} = 1 MHz	0.26	–	–	µs
SCL Low Time	t_{LOW}	f_{CLK} = 400 kHz	1.3	–	–	µs
		f_{CLK} = 1 MHz	0.5	–	–	µs
SCL High Time	t_{HIGH}	f_{CLK} = 400 kHz	0.6	–	–	µs
		f_{CLK} = 1 MHz	0.26	–	–	µs
Data Setup Time	$t_{DAT(S)}$	f_{CLK} = 400 kHz	100	–	–	ns
		f_{CLK} = 1 MHz	50	–	–	ns
Setup Time for Stop Condition	$t_{STO(S)}$	f_{CLK} = 400 kHz	0.6	–	–	µs
		f_{CLK} = 1 MHz	0.26	–	–	µs
Output Fall Time	t_f	f_{CLK} = 400 kHz; R_{PU} = 2.4 kΩ; C_{BUS} = 100 pF	–	–	250	ns
		f_{CLK} = 1 MHz; R_{PU} = 1.6 kΩ; C_{BUS} = 10 pF	–	–	120	ns
I²C ELECTRICAL CHARACTERISTICS						
Logic Input Low Level	V_{LO}	Low-voltage interface	–	–	0.54	V
		Ratiometric interface	–	–	0.3 × V_{DD}	V
Logic Input High Level	V_{HI}	Low-voltage interface	1.26	–	–	V
		Ratiometric interface	0.7 × V_{DD}	–	–	V
Input Threshold Hysteresis	$V_{I(HYS)}$	Low-voltage interface	90	–	–	mV
		Ratiometric interface	0.05 × V_{DD}	–	–	V
Logic Input Current	$I_{I2C(IN)}$	V_{IN} = 0 V to V_{DD}	–1	–	1	µA
Output Voltage Low Level	$V_{O(L)}$	I_{LOAD} = 20 mA	–	–	0.4	V
SCL Capacitive Load	C_{BUS}	f_{CLK} = 400 kHz	–	–	100	pF
		f_{CLK} = 1 MHz	–	–	20	pF

[1] Specification not measured at final test; determined by design and characterization.
[2] Typical values are for T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.
[3] The minimum pull-up resistance $R_{PU(I2C,MIN)}$ is recommended for high-speed operation (FM+). Users must evaluate the load conditions for bussed use at high frequency.

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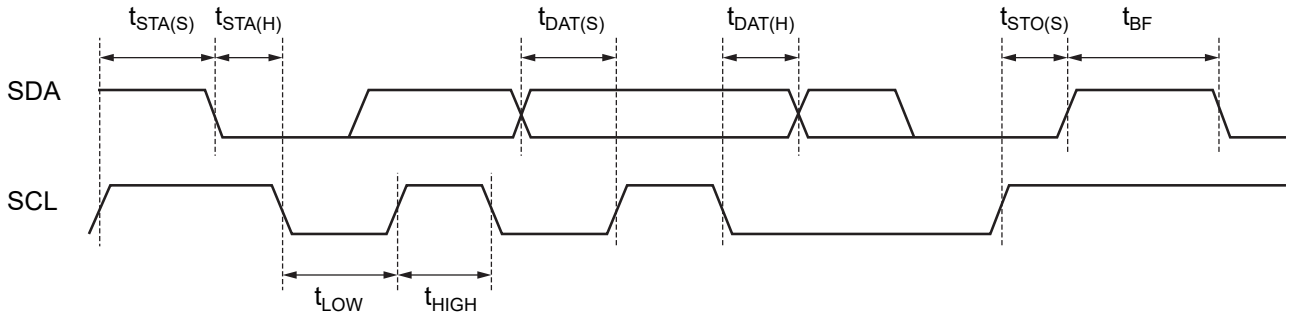

Figure 5: I²C Interface Timing Diagram

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CHARACTERIZATION PLOTS

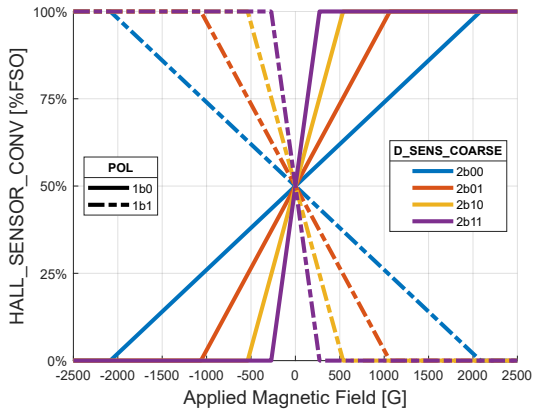

Figure 6: Bipolar Output with 50% Offset (OFFSET_COARSE = 2b01 or 2b10)

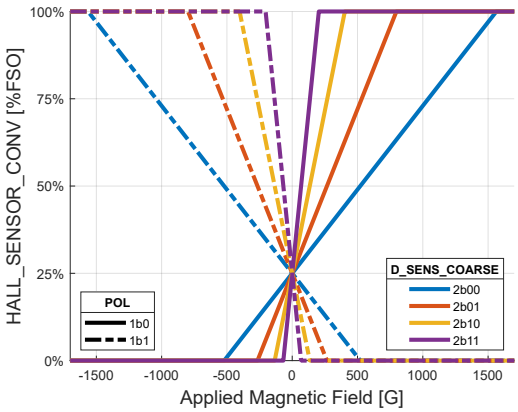

Figure 7: Bipolar Output with 25% Offset (OFFSET_COARSE = 2b00)

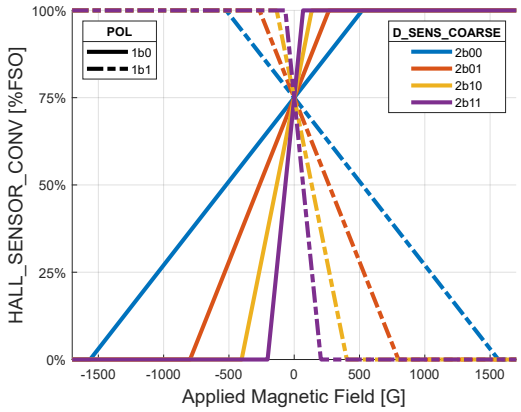

Figure 8: Bipolar Output with 75% Offset (OFFSET_COARSE = 2b11)

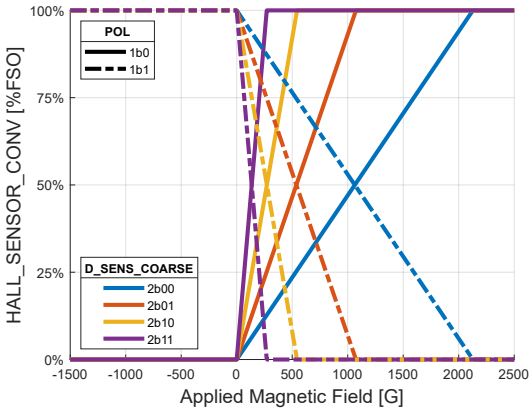

Figure 9: Unipolar South Output

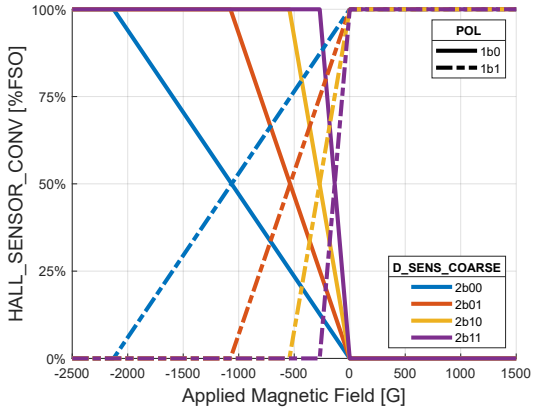

Figure 10: Unipolar North Output

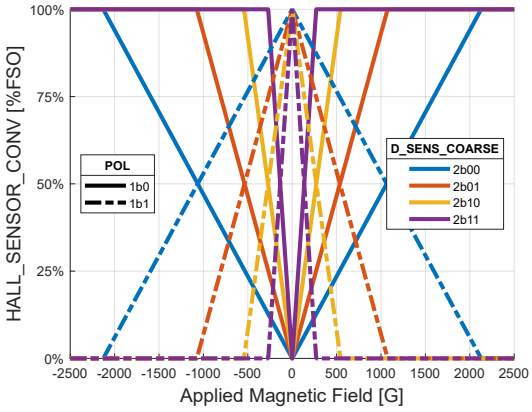

Figure 11: Omnipolar Output

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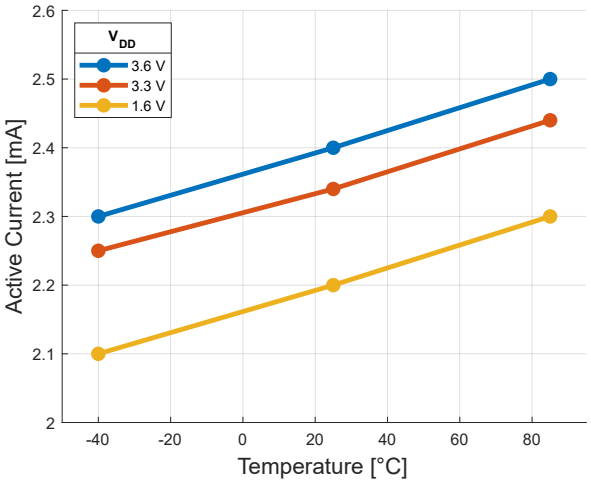

Figure 12: Active Current (-Z Option)

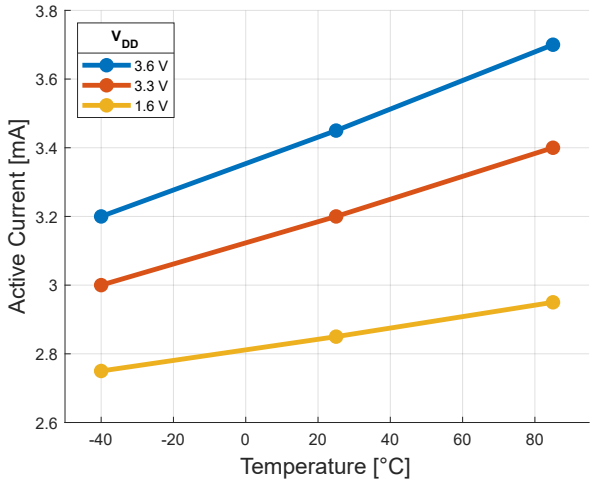

Figure 13: Active Current (-X Option)

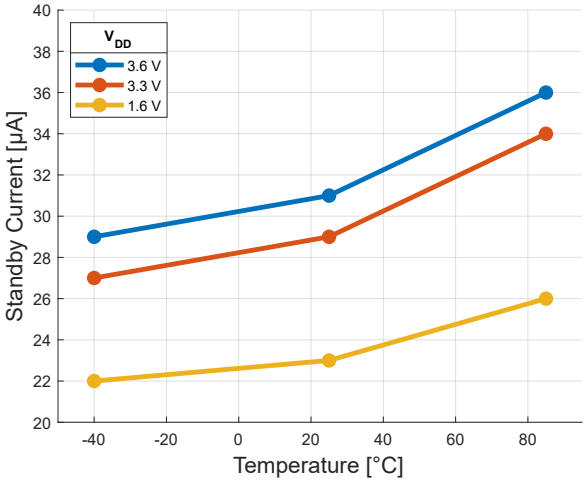

Figure 14: Standby Current

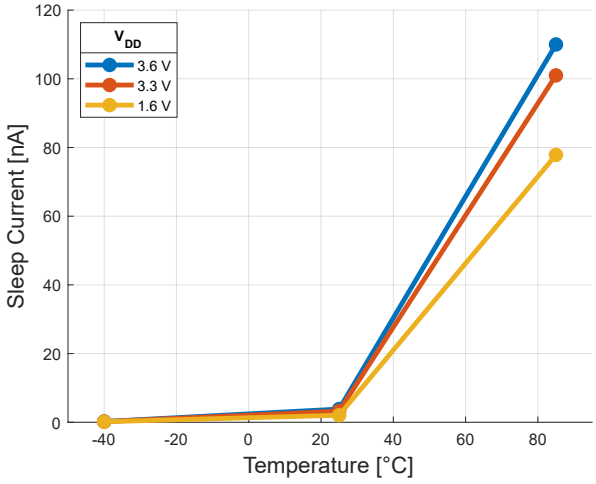

Figure 15: Sleep Current

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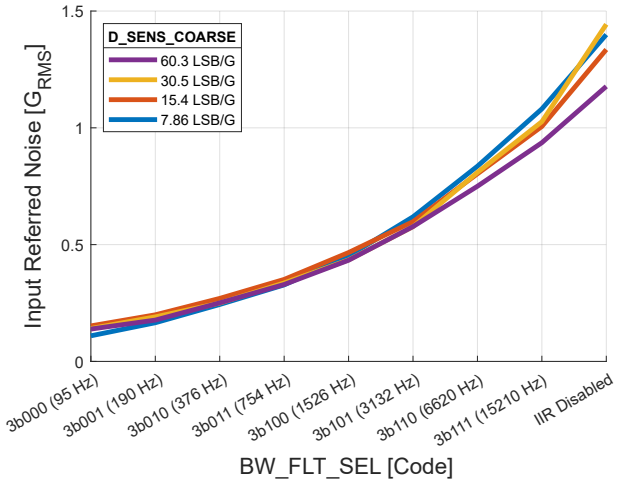

Figure 16: Output Noise Standard Deviation (-X Option)

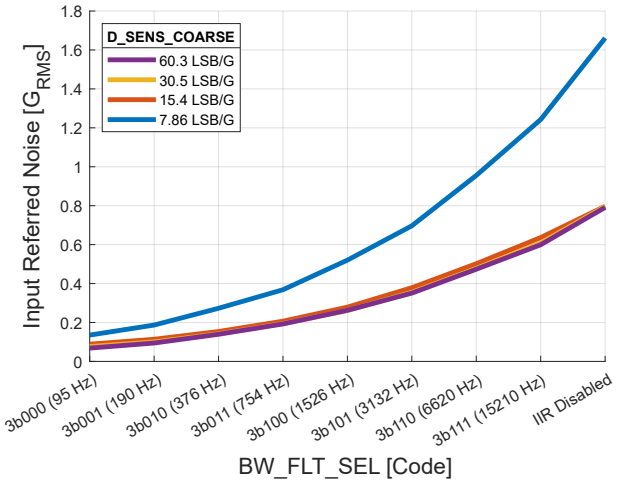

Figure 17: Output Noise Standard Deviation (-Z Option)

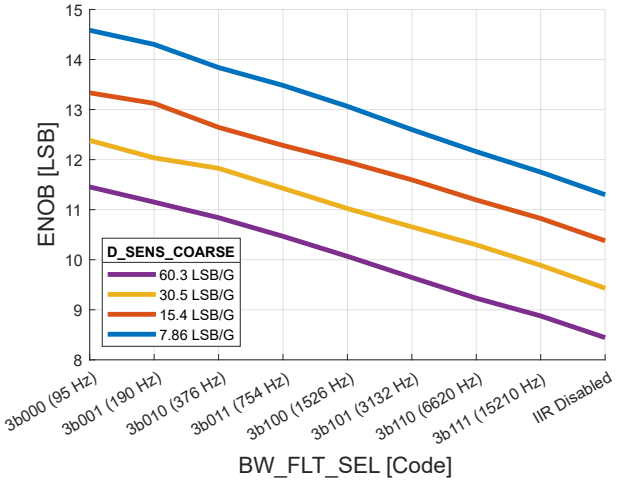

Figure 18: Effective Number of Bits (ENOB) (-X Option)

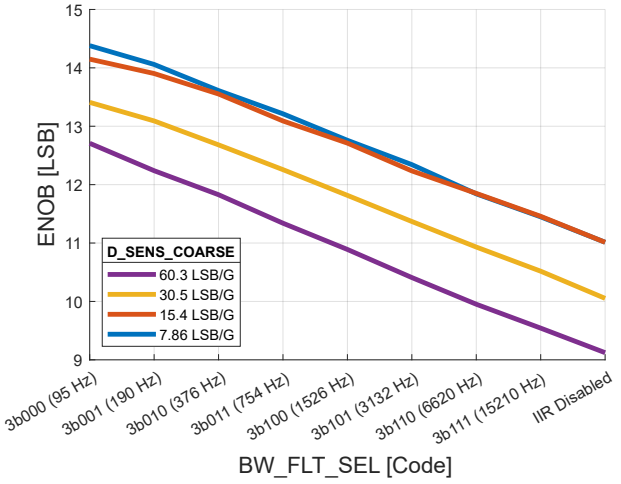

Figure 19: Effective Number of Bits (ENOB) (-Z Option)

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FUNCTIONAL DESCRIPTION AND CONFIGURATION OPTIONS

Magnetic Sensor Output

The A31020 provides a 15-bit digital output value proportional to the magnetic field applied nominally to the Hall elements. This output is read from the HALL_SENSOR_CONV field with an I²C read. The signal path is factory-trimmed for sensitivity and offset accuracy at ambient room temperature as well as with a target temperature compensation. The ambient room temperature sensitivity (D_SENS_COARSE) and offset temperature compensation (D_MAG_TC) parameters are accessible by the user for additional adjustment in application. This allows the A31020 to be configured to the application's magnetic field range with high accuracy and matching as the magnetic system changes over temperature.

Power States

Power management of the A31020 is user-selectable and highly configurable, allowing for system-level optimization of current consumption and performance. The A31020 supports three power states: active state, standby state, and sleep state.

ACTIVE STATE

In active state, the A31020 continuously updates the channel and angle outputs at an interval defined by the bandwidth selection. This is the required mode for the A31020 to sample the magnetic input. See the Operating Modes (next section) for details on how to configure the A31020 to enter each mode.

STANDBY STATE

Standby state is a low-power (µA) state used to conserve power when not actively sampling the magnetic field. The A31020 does not sample the magnetic input in standby state but does preserve all memory, including the last magnetic input sampled. In standby state, I²C communication is limited to the following functionality:

- Reading the MAGNETIC_OUTPUT register (0x12)
- Read/write OP_MODE_CONFIG register (0x14)
- Read/write START_SAMPLE field in the CMDS register (0x16)

SLEEP STATE

Sleep state is a ultra-low-power (nA) state used to conserve power when not actively sampling the magnetic field. The A31020 is effectively shut down in sleep state, i.e., the A31020 does not respond to any I²C commands and volatile memory is cleared.

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Operating Modes (Conversion Modes)

The A31020 operates in one of three modes configurable by the user: continuous mode, one-shot mode, and low-power duty cycle mode (LPDCM) which automatically toggles between active state and standby state. These operating modes are selectable by the end user by configuring the CONV_MODE_DIR (direct) or CONV_MODE (indirect) fields in memory. See Table 1 for more information.

CONTINUOUS MODE

In continuous mode, the A31020 stays in the active state, where the magnetic field is continuously sampled and the output is continuously updated.

While in continuous mode, the SLEEP pin can be used to toggle between active state and standby or sleep state (depending on the configuration of the SLEEP_CFG_DIR (direct) or SLEEP_CFG (indirect) fields in memory). Additionally, the inverse mode of what is configured in SLEEP_CFG_DIR can be entered by writing 2b1 to the CONV_MODE_DIR (direct) or CONV_MODE (indirect) fields in memory. Writing 2b0 to the same register puts the A31020 back to active state.

ONE-SHOT MODE

In one-shot mode, the A31020 automatically transitions into standby state after taking a single sample of the magnetic field and remains in standby state until commanded by the user to enter active state again to take another single sample. Depending on user configurations (see Table 1), the command to take a single measurement is either an I²C write of 1b1 to the START_SAMPLE field in the CMDS direct memory register (0x16 bit 12), and/or by asserting the SLEEP pin low.

LOW-POWER DUTY CYCLE MODE (LPDCM)

In low-power duty cycle mode (LPDCM), the A31020 toggles between active state and standby state, reducing the overall current consumption. The average I_{DD} for the A31020 during LPDCM varies based on the device configurations. The diagram in Figure 20 shows the profile of I_{DD} as the A31020 toggles between active state and standby state during LPDCM.

Table 1: Operating Mode Control

Programmable Configurations			Active State [1][2]		Standby State [2]		Sleep State [2]	
CONV_MODE	SLEEP_CFG	Ref.	From Standby	From Sleep	From Active	From Sleep	From Active	From Standby
2b00 or 2b01 (Continuous Mode)	1b0 (Sleep)	1A	See footnote 2	Hold SLEEP pin low	See footnote 2	–	Hold SLEEP pin high	Hold SLEEP pin high
	1b1 (Standby)	1B	Hold SLEEP pin low	See footnote 2	Hold SLEEP pin high	–	See footnote 2	See footnote 2
2b01 (One-Shot Mode)	1b0 (Sleep)	2A	Write 1b1 to START_SAMPLE	Hold SLEEP pin low	Automatic after sample	–	Hold SLEEP pin high	Hold SLEEP pin high
	1b1 (Standby)	2B	Toggle SLEEP pin low then high	Toggle SLEEP pin low then high	Automatic after sample	–	See footnote 2	See footnote 2
2b11 (LPDCM)	1b0 (Sleep)	3A	Automatic after LPDCM timer expires	Hold SLEEP pin low	Automatic after sample	–	Hold SLEEP pin high	Hold SLEEP pin high
	1b1 (Standby)	3B	Automatic after LPDCM timer expires or toggle SLEEP pin low then high	Toggle SLEEP pin low then high	Automatic after sample	–	See footnote 2	See footnote 2

[1] The A31020 always powers-on in active state, e.g., in one-shot mode or low-power duty cycle mode, a sample conversion is made before automatically transitioning to standby state for the first time.

[2] While not a primary use case, transitioning to this state can be accomplished by temporarily configuring the A31020 to a different programming configuration (using I²C commands to write the CONV_MODE and/or SLEEP_CFG fields) and configuring back to the initial configuration when the state is no longer desired. For example, to transition from active state to standby state when in programming configuration 1A, set the configuration to 1B and use the SLEEP pin, then program back to configuration 1A when standby state is no longer desired.

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LPDCM Sample Period

The LPDCM sample period of the A31020 is determined by adding the active time (t_{ACTIVE}) and standby time ($t_{STANDBY}$).

The active time is determined by the bandwidth configuration of the device, which is configured by the BW_FLT_SEL field found in the EEPROM_4 indirect register (0x04 bits 25:23). The active time based on the configurations is shown in Table 2.

The standby time is determined by the value set by the LPDCM_SLEEP_TIMER_DIR field found in the OP_MODE_CONF direct register (0x14 bits 4:2) or the LPDCM_SLEEP_TIMER field found in the EEPROM_4 indirect register (0x04 bits 4:2).The standby time based on the configurations is shown in Table 3.

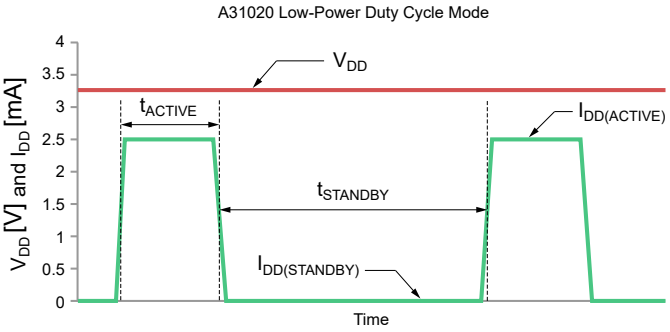

Figure 20: I_{DD} in Low-Power Duty Cycle Mode

Table 2: LPDCM Active Time (t_{ACTIVE}) Configurations

Bandwidth Filter Select Value (BW_FLT_SEL)		Typical t_{ACTIVE}	
		OSR_FILTER_UPDATE = 1b0	OSR_FILTER_UPDATE = 1b1
3b000	95 Hz	2.1 ms	3.8 ms
3b001	190 Hz	1 ms	1.9 ms
3b010	376 Hz	570 µs	1 ms
3b011	754 Hz	310 µs	530 µs
3b100	1526 Hz	180 µs	300 µs
3b101	3132 Hz	110 µs	180 µs
3b110	6620 Hz	85 µs	120 µs
3b111	15210 Hz	65 µs	90 µs
IIR_EN = 0 (Filter Disabled)		60 µs	75 µs

Table 3: LPDCM Standby Time ($t_{STANDBY}$) Configurations

LPDCM Timer Value (LPDCM_SLEEP_TIMER)	Typical $t_{STANDBY}$
3b000	0.125 ms
3b001	0.250 ms
3b010	0.500 ms
3b011	1.000 ms
3b100	10.00 ms
3b101	100.0 ms
3b110	500.0 ms
3b111	1000 ms

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Output Configurations

The A31020 provides several configurable options for sensing various types of magnetic fields allowing the user to customize the A31020 to meet the needs of their application.

SENSING AXIS

The A31020 is offered in two selectable options depending on the sensing axis (X-axis sensing or Z-axis sensing). Each come factory-trimmed for offset and sensitivity to correct for any non-ideality in the vertical (X-axis) or planar (Z-axis) Halls.

OUTPUT MODE

The A31020 can be user-configured to meet the application needs of the magnetic field applied.

Bipolar Mode

In bipolar mode, the A31020 responds to the applied north and south magnetic fields. With no magnetic field applied (0 G), the output of the A31020 is at 50% of the output range (approximately code 16383 of the 32768 output code range). The output of the A31020 increases/decreases prepositionally to the applied magnetic south/north field depending on the configuration of the polarity. The amount of increase/decrease (LSB/G) is dependent on the configuration of the sensitivity. See Figure 21.

Additionally, the A31020 can shift the 0 G offset from 50% to either 25% or 75% of the output range (approximately code 8191 or 24575 respectively). This can be accomplished by configuring the OFFSET_COARSE field in indirect memory (register 0x03 for non-volatile and 0x23 for volatile). This can be useful in applications that require sensing of north and south magnetic fields, but in unequal proportion. Note that when applying the 25% or 75% offset shift in bipolar mode, the sensitivity is doubled compared to the 50% offset configuration. See Figure 22.

Unipolar Mode (Unipolar North and Unipolar South)

In unipolar mode, the A31020 responds to only a north or south magnetic field (configurable by the user). With no magnetic field applied, the output of the A31020 is at 0% of the output range while increasing with applied magnetic field, or at 100% of the output range while decreasing with applied magnetic field (depending on the user configurations for the polarity). The amount of increase/decrease (LSB/G) is dependent on the configuration of the sensitivity. See Figure 23.

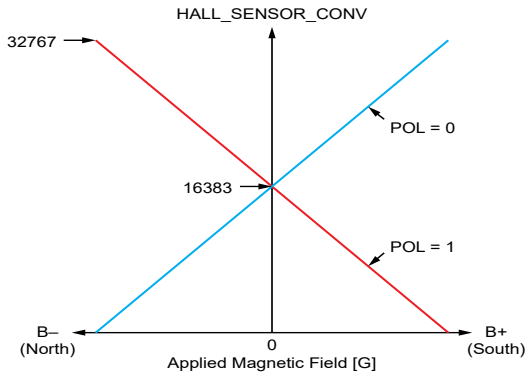

Figure 21: Bipolar Mode with 50% Offset

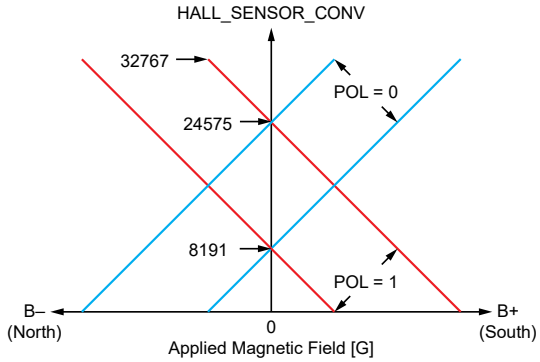

Figure 22: Bipolar Mode with 25% and 75% Offset

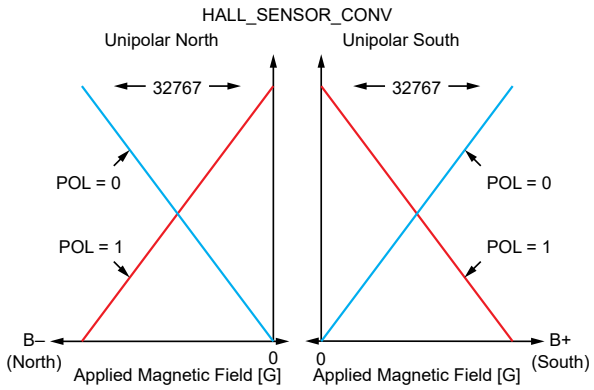

Figure 23: Unipolar North (Left) and Unipolar South (Right)

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Omnipolar Mode

In omnipolar mode, the A31020 responds to either a north or south magnetic field in the same way (i.e., the output responds to the absolute value of the magnetic field). With no magnetic field applied, the output of the A31020 is at 0% of the output range while increasing with applied magnetic field, or at 100% of the output range while decreasing with applied magnetic field (depending on the user configurations for the polarity). The amount of increase/decrease (LSB/G) is dependent on the configuration of the sensitivity. See Figure 24.

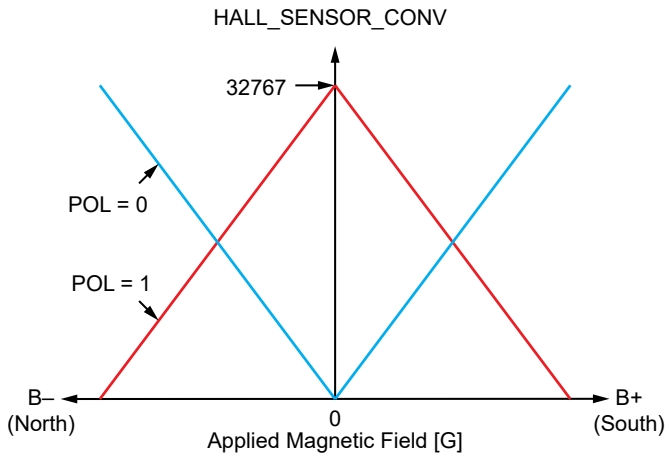

Figure 24: Omnipolar Mode

POLARITY

As noted in the Output Mode section, the polarity can be inverted in any of the output modes, such that the sensitivity (slope of the output with respect to the magnetic field input) is inverted. This can be used to set the desired output against the application's magnetic field input and/or orientation (north vs. south). The polarity can be configured by writing to the POL field in indirect memory (register 0x03 for non-volatile and 0x23 for volatile). See the figures above in the Output Mode section for how the polarity configuration impacts the HALL_SENSOR_CONV output.

SENSITIVITY

The A31020 offers four options for configuring the sensitivity (see Magnetic Characteristics table). This can be configured by the user to meet that application range of the magnetic field. Users can configure the sensitivity by writing the D_SENS_COARSE field in indirect memory (0x03 for non-volatile, 0x23 for volatile). See Table 4.

Table 4: D_SENS_COARSE Configurations

Output Mode	Sensitivity Value (D_SENS_COARSE)	Typical Sensitivity at 25°C (LSB/G)
Bipolar with 50% Offset	2b00 (VHF)	7.86
	2b01 (HF)	15.4
	2b10 (MF)	30.5
	2b11 (LF)	60.3
Bipolar with 25% or 75% Offset	2b00 (VHF)	15.7
	2b01 (HF)	30.8
	2b10 (MF)	61
	2b11 (LF)	120
Unipolar or Omnipolar	2b00 (VHF)	15.4
	2b01 (HF)	30.5
	2b10 (MF)	60.3
	2b11 (LF)	121.2

Note that when using VHF, set OFFSET_FINE_X2 field in indirect memory (0x04 for non-volatile, 0x24 for volatile) to 1b1.

SENSITIVITY TEMPERATURE COEFFICIENT (TC)

The A31020 offers a variety of options to compensate for common magnetic field strength variation over temperature. The sensitivity TC gains the sensitivity over temperature to compensate for the magnetic field variation, allowing for a consistent output of the A31020 over temperature. Users can configure the sensitivity TC by writing the D_MAG_TC field in indirect memory (0x03 for non-volatile, 0x23 for volatile).

Table 5: D_MAG_TC Configurations

Sensitivity TC Value (D_MAG_TC)	Typical Sensitivity TC
2b00 (Flat)	0%/°C
2b01 (Ferrite)	0.2%/°C
2b10 (Neodymium)	0.12%/°C
2b11 (Samarium-Cobalt)	0.04%/°C

Bandwidth

The A31020 can configure an internal bandwidth filter to meet the application needs of noise and input frequency. The lower the bandwidth frequency, the lower the noise of the A31020 output (at the cost of response time/maximum input frequency). Users can enable or disable the bandwidth filter by writing the IIR_EN field in indirect memory (0x03 for non-volatile, 0x23 for volatile), and configure the bandwidth filter frequency by writing the BW_FLT_SEL field in indirect memory (0x04 for non-volatile, 0x24 for volatile). See Table 6 and Characteristic Plots section.

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Table 6: IIR_EN and BW_FLT_SEL Configurations

Filter Enable (IIR_EN)	Bandwidth Select (BW_FLT_SEL)	Typical Bandwidth
1b1 (Enabled)	3b000	95 Hz
	3b001	190 Hz
	3b010	376 Hz
	3b011	754 Hz
	3b100	1526 Hz
	3b101	3132 Hz
	3b110	6620 Hz
	3b111	15210 Hz
1b0 (Disabled)	Any	26085 Hz

Over-Sampling Ratio (OSR) Filter

The A31020 contains an option to double the samples collected for each measurement and average them on each conversion. Enabling the OSR filter improves the noise performance at the cost of doubling the conversion time. Users can enable/disable the OSR filter by writing a 1/0 (respectively) to the OSR_FLT_UPDATE_DIR field in direct memory or OSR_FLT_UPDATE in indirect memory (0x04 for non-volatile, 0x24 for volatile).

STATUS Pin Output

The A31020 provides an open-drain output corresponding to the comparison of the output (HALL_SENSOR_CONV) to a user-programmable threshold. This can be used to poll the STATUS pin (rather than the HALL_SENSOR_CONV field) for a coarse check of the magnetic field movement prior to reading the high-resolution output over I²C.

The STATUS pin is latched when pulled low and can be cleared by reading the STATUS_FLAG field in direct memory (0x12) when the threshold condition is no longer met.

Users can enable/disable the threshold check by writing a 1/0 (respectively) to the INT_EN_DIR field in direct memory (0x14) or INT_EN field in indirect memory (0x04 for non-volatile, 0x24 for volatile). Users can then set the threshold by writing to the INT_THRESHOLD_DIR field in direct memory or INT_THRESHOLD field in indirect memory (0x04 for non-volatile, 0x24 for volatile). The value programmed into INT_THRESHOLD_DIR and INT_THRESHOLD corresponds to the 6 MSBs of the 15-bit output range.

When disabled, the STATUS pin remains high at all times. When enabled and POL = 0, the STATUS pin is high when the output is lower than the configured threshold, and is low when the output is higher than the configured threshold. When enabled and POL = 1, the STATUS pin is low when the output is lower than the configured threshold, and is high when the output is higher than the configured threshold. See Table 7 and Table 8.

Table 7: STATUS Pin Configurations

Threshold Enable (INT_EN)	Polarity (POL)	Output Comparison	STATUS Pin
1b1 (Enabled)	1b0	Output > Threshold	High
		Output ≤ Threshold	Low
	1b1	Output > Threshold	Low
		Output ≤ Threshold	High
1b0 (Disabled)	Any	Any	High

Table 8: INT_THRESHOLD Configurations

Threshold Setting (INT_THRESHOLD)	Threshold [LSBs]
6b000000	0
6b000001	512
6b000010	1024
...	...
6b111110	31744
6b111111	32256

I/O Reference Voltage

The A31020 supports two options for configuring the I/O high voltage level (SDA, SCL, SLEEP, and STATUS pins). This can be configured to use the supply voltage (V_{DD}) or to use the internal low-voltage rail of 1.8 V [1]. Users can configure this by writing a 0/1 to the D_IO_INTERFACE field in indirect memory (0x03 for non-volatile, 0x23 for volatile) to set the reference voltage to the supply voltage/internal low-voltage rail (respectively).

[1] Below supply voltages (V_{DD}) of 1.9 V, the internal low-voltage rail scales proportionally with the supply voltage from 1.8 V (with a supply voltage of 1.9 V) down to 1.55 V (with a supply voltage of 1.65 V).

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I²C INTERFACE INFORMATION

I²C Interface

I²C is a synchronous, 2-wire communication protocol which provides a full-duplex interface between two or more devices. The bus specifies two logic signals:

1. Serial Clock Line (SCL) output by the controller.
2. Serial Data Line (SDL) output by either the controller or the peripheral.

The A31020 may operate as a peripheral device. Therefore, it cannot initiate any transactions on the I²C bus.

I²C Data Transmission and Timing Considerations

I²C communication is composed of several steps outlined in the following sequence:

1. Start Condition: Defined by a falling edge of the SDA line, initiated by the controller, while SCL is high.
2. Address Cycle: 7-bit peripheral address, plus 1 bit to indicate write (0) or read (1), followed by an acknowledge bit.
3. Data Cycles: Reading or writing 8 bits of data, followed by an acknowledge bit. This cycle can be repeated for multiple bytes of data transfer. The first data byte on a write could be the register address. See the following sections for more information.
4. Stop Condition: Defined by a rising edge on the SDA line, while SCL is high.

Except to indicate start or stop conditions, SDA must remain stable while the clock is high. SDA may only change while SCL is low. It is acceptable for a start or stop condition to occur at any time during the data transfer. The A31020 always responds to a read or write request by resetting the transfer sequence.

The state of the read/$\overline{\text{write}}$ bit is set to 0 to indicate a write cycle and set to 1 to indicate a read cycle.

The controller monitors for an acknowledge bit to confirm the peripheral device (A31020) is responding to the address byte. When the A31020 decodes the 7-bit peripheral address as valid, it responds by pulling SDA low during the ninth clock cycle.

When a data write is requested by the controller, the A31020 pulls SDA low during the clock cycle following the data byte to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the controller must release the SDA line before the ninth clock cycle, allowing the handshake process to occur.

I²C Write Cycle Overview

The write cycle to access registers on the A31020 are outlined in the sequence below:

1. Controller initiates the start condition.
2. Controller sends the 7-bit peripheral address and then the write bit (0).
3. Controller waits for the ACK from the A31020.
4. Controller sends the 8-bit register address.
5. Controller waits for the ACK from the A31020.
6. Controller sends the 15:8 bits of data.
7. Controller waits for the ACK from the A31020.
8. Controller send the 7:0 bits of data.
9. Controller waits for the ACK from the A31020.
10. Controller initiates the stop condition.

The I²C write sequence is further illustrated in the timing diagrams below in Figure 25.

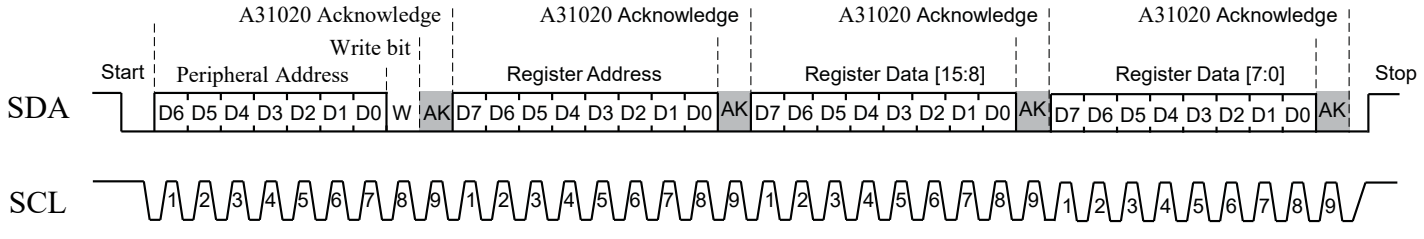

Figure 25: I²C Write Timing Diagram

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I²C Read Cycle Overview

The read cycle to access registers on the A31020 is outlined in the sequence below:

1. Controller initiates the start condition.
2. Controller sends the 7-bit peripheral address and then the write bit (0).
3. Controller waits for the ACK from the A31020.
4. Controller sends the 8-bit register address.
5. Controller waits for the ACK from the A31020.
6. Controller initiates a start condition; in this case it is referred to as the restart condition.
7. Controller sends the 7-bit peripheral address and then the read bit (1).
8. Controller waits for the ACK from the A31020.
9. Controller receives the 15:8 bits of data.
10. Controller sends the ACK to the A31020.
11. Controller receives the 7:0 bits of data.
12. Controller sends the NACK to the A31020.
13. Controller initiates the stop condition.

The I²C read sequence is further illustrated in the timing diagram in Figure 26.

The timing diagram in Figure 26 shows the entire contents (bits 15:0) of a single register location being transmitted. Optionally, the I²C controller may choose to replace the NACK on step 12 with an ACK instead, which allows the read sequence to continue. This case results in the transfer of contents (bits 31:24) from the next register of the memory. The controller can then continue to acknowledge (ACK), send the not-acknowledge (NACK), or stop after any byte to stop receiving data.

Note that only the initial register address is required for reads, allowing for faster data retrieval. However, this restricts data retrieval to sequential registers when using a single read command. When the controller provides a non-acknowledge bit and stop condition, the A31020 stops sending data. If nonsequential registers are to be read, separate read commands must be sent.

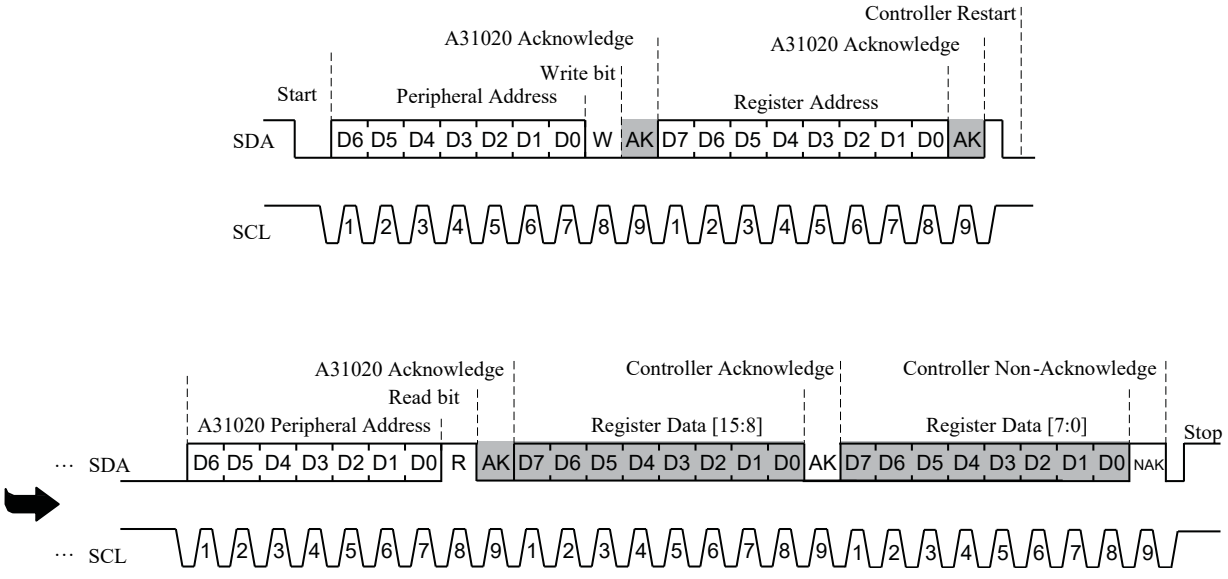

Figure 26: I²C Read Timing Diagram

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I²C Readback Modes

The A31020 supports two different readback modes of the I²C interface: single and continuous. Continuous mode simplifies the process of reading out blocks of data from memory.

SINGLE MODE

A single write or read command to any register—this is the default mode and is best suited for setting fields and reading static registers. This mode can be used to read data in a typical serial fashion. After each single read is complete, the controller shall issue a NACK to complete the transaction.

CONTINUOUS MODE

Instead of issuing a NACK after a read request, the controller can keep issuing an ACK. When this is done, the A31020 continues to transmit data from the next address. This can be useful for reading data from successive registers, without needing to send a read command for each register.

I²C Addressing

The A31020 responds to the peripheral address stored in the I2C_SLV_ADDR field (indirect memory space 0x04, bits 21:15). From the factory, this is set to 7b0000000.

When I2C_SLV_ADDR_IGNORE field (indirect memory space 0x04, bit 22) is enabled (set to 1), the A31020 responds to any address, regardless of what is programmed in the I2C_SLV_ADDR field.

MEMORY ACCESS

Direct and Indirect Memory Structure

The A31020 uses a direct and indirect memory structure.

Direct memory registers are volatile and contain some of the configuration options, the magnetic output of the A31020, and the registers required to interface with the Indirect memory registers. The direct memory registers are 16-bits and can be read or written without the customer access code.

Indirect memory registers contain EEPROM (non-volatile) and a shadow of the configuration registers found in EEPROM. Indirect registers are 32-bits. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to the shadow (volatile) memory at power-on.

Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an indirect write to the shadow address or by programming the corresponding EEPROM fields and power cycling the A31020. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at indirect addresses 0x20 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and returns 0 when read. Shadow registers do not contain the ECC bits. The mapping of bits from register address in EEPROM to their corresponding register address in shadow is shown in the Indirect Memory section.

Accessing Memory

The A31020 memory is accessible via the serial interface through I²C. Registers are given one of three access levels: general access, customer, and factory:

- General access registers are available to be read and written without providing the access code.
- Customer access registers are available to be read and written after providing the access code (see below).
- Factory registers are available to be read only after providing the access code (see below).

Access to customer and factory registers are controlled by a 32-bit access code, which is written to the ACCESS_KEY field in the ACCESS register (address 0x1A) using two consecutive I²C writes. The access code is 0x43555354, and is written to the ACCESS_KEY field as follows:

1. Write the 16 MSBs of the access code (0x4355, or 16b0100001101010101) to address 0x1A.
2. Write the 16 LSBs of the access code (0x5354, or 16b0101001101010100) to address 0x1A.

When the access code is received, factory registers are addressable, but are read-only.

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READING INDIRECT MEMORY (EEPROM AND SHADOW)

After providing the access code, reading an indirect memory register is a three-step process:

1. Write the desired indirect memory address to the INDIRECT_RD_ADDR field (0x0A).
2. Write a 1 to the EXR field (0x0C). The indirect register is read and loaded to INDIRECT_RD_DATA_MSB register (0x0E) and the INDIRECT_RD_DATA_LSB register (0x10).
3. Read the INDIRECT_RD_DATA_MSB register (0x0E) and INDIRECT_RD_DATA_LSB register (0x10). Multiple read transactions are required to obtain all 32 bits from the two 16-bit registers.

The RDN field in the INDIRECT_RD_STATUS register (0x0C) can be polled to determine if the load of the read data is complete before reading the data out. Do not attempt to read the INDIRECT_RD_DATA_MSB ro INDIRECT_RD_DATA_LSB registers if the data is still being loaded to those registers, as it could provide an unreliable read of the data.

Example read of the EEPROM_4 (0x04) indirect register:

1. Write 0x04 to the INDIRECT_RD_ADDR register.
2. Write 0x8000 to the INDIRECT_RD_STATUS register (setting EXR to 1).
3. Read the INDIRECT_RD_STATUS register until bit 0 (RDN) is set to 1 (or wait for a sufficient time for the load of the data to complete).
4. Read the INDIRECT_RD_DATA_MSB register (upper 16 bits of the read data).
5. Read the INDIRECT_RD_DATA_LSB register (lower 16 bits of the read data).

WRITING INDIRECT MEMORY (EEPROM AND SHADOW)

After providing the access code, writing an indirect memory register is a three-step process:

1. Write the desired indirect memory address to the INDIRECT_WR_ADDR field (0x02).
2. Write the desired data to INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB registers. Multiple write transactions are required to load all 32 bits of data.
3. Write a 1 to the EXW field (0x08) to initiate the write to the indirect memory register.

The indirect memory address provided to the INDIRECT_WR_ADDR field are then written with the 32 bits of data provided to the INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB registers. The WDN bit in the INDIRECT_WR_STATUS register (0x08) can be polled to determine when the write completes.

Note that writes are performed by register (not field). If a subset of fields from a register are needed to be written (while preserving the programming of other fields), users must read the register first, and re-write the values to the fields that the user does not intend to change.

Shared Factory and Customer Trim Registers

The memory contents in indirect memory address 0x03 (EEPROM_3) and 0x04 (EEPROM_4) as well as their shadow counterparts in address 0x23 (SHADOW_3) and 0x24 (SHADOW_4) contain registers used to factory trim the A31020 for the highest sensing accuracy. If configuring fields in these registers, users must ensure a read of those fields are recorded first, with those values re-written on the write to the register).

NOTE: It is up to the user to ensure accuracy of the device after end-of-line programming.

Memory Access in Low-Power Modes

When in standby mode, read/write access is limited to critical registers to help conserve power. Only a subset of the direct memory registers are available that are necessary to use the A31020 in normal operation. Writes are only possible to the OP_MODE_CONFIG register (0x14), which contain device configuration parameters, as well as the START_SAMPLE field in the CMDS register (0x16, bit 12). Reading of the MAGNETIC_OUT register (0x12) is also allowed in these low-power modes. See the MEMORY MAP section for more information on the contents of these registers.

NOTE: I²C communication is not available while the A31020 is in sleep mode.

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DIRECT MEMORY ACCESS

Direct Memory Register Map [1]

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x02	INDIRECT_WR_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
0x04	INDIRECT_WR_DATA_MSB	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
0x06	INDIRECT_WR_DATA_LSB	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
0x08	INDIRECT_WR_STATUS	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x0A	INDIRECT_RD_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							
0x0C	INDIRECT_RD_STATUS	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x0E	INDIRECT_RD_DATA_MSB	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
0x10	INDIRECT_RD_DATA_LSB	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
0x12	MAGNETIC_OUT	STATUS_FLAG	HALL_SENSOR_CONV														
0x14	OP_MODE_CONF	0	INT_EN_DIR	INT_THRESHOLD_DIR						CONV_MODE_DIR		SLEEP_CFG_DIR	LPDCM_SLEEP_TIMER_DIR			OSR_FILTER_UPDATE_DIR	0
0x16	CMDS	0	0	SOFT_RST	START_SAMPLE	0	0	0	0	0	0	0	0	0	0	0	0
0x1A	ACCESS	ACCESS_KEY															

[1] Fields with 0 must be written as 0 when writing to the register.

Direct Memory Register Reference

Address 0x02: INDIRECT_WR_ADDR – Indirect Write Address

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x02	INDIRECT_WR_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							

INDIRECT_WR_ADDRESS [7:0]

Indirect address to write.

Address 0x04: INDIRECT_WR_DATA_MSB – Indirect Write Data, MSB

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x04	INDIRECT_WR_DATA_MSB	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							

INDIRECT_WR_DATA_3 [15:8]

Indirect data to write, byte 3.

INDIRECT_WR_DATA_2 [7:0]

Indirect data to write, byte 2.

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Address 0x06: INDIRECT_WR_DATA_LSB – Indirect Write Data, LSB

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x06	INDIRECT_WR_DATA_LSB	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							

INDIRECT_WR_DATA_1 [15:8]

Indirect data to write, byte 1.

INDIRECT_WR_DATA_0 [7:0]

Indirect data to write, byte 0.

Address 0x08: INDIRECT_WR_STATUS – Indirect Write Status

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x08	INDIRECT_WR_STATUS	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN

EXW [15]

Write field with value 1 to initiate an indirect write command. This sets WIP to 1 and WDN to 0. Write-only field (always reads back as 0).

WIP [8]

Reads 1 when writing is in progress. Read-only field.

WDN [0]

Reads 1 when writing is complete. Read-only field.

Address 0x0A: INDIRECT_RD_ADDR – Indirect Read Address

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0A	INDIRECT_RD_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							

INDIRECT_RD_ADDRESS [7:0]

Indirect address to read.

Address 0x0C: INDIRECT_RD_STATUS – Indirect Read Status

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0C	INDIRECT_RD_STATUS	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN

EXR [15]

Write field with value 1 to initiate an indirect read command. This sets RIP to 1 and RDN to 0. Write-only field (always reads back as 0).

RIP [8]

Reads 1 when reading is in progress. Read-only field.

RDN [0]

Reads 1 when reading is complete. Read-only field.

Address 0x0E: INDIRECT_RD_DATA_MSB – Indirect Read Data, MSB

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0E	INDIRECT_RD_DATA_MSB	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							

INDIRECT_RD_DATA_3 [15:8]

Indirect data to read, byte 3.

INDIRECT_RD_DATA_2 [7:0]

Indirect data to read, byte 2.

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Address 0x10: INDIRECT_RD_DATA_LSB – Indirect Read Data, LSB

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x10	INDIRECT_RD_DATA_LSB	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							

INDIRECT_RD_DATA_1 [15:8]

Indirect data to read, byte 1.

INDIRECT_RD_DATA_0 [7:0]

Indirect data to read, byte 0.

Address 0x12: MAGNETIC_OUT – Magnetic Signal Output

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x12	MAGNETIC_OUT	STATUS_FLAG	HALL_SENSOR_CONV														

STATUS_FLAG [15]

Flag indicating the threshold has been exceeded (STATUS pin is pulled low). Read-only field. Clears on read.

HALL_SENSOR_CONV [14:0]

15-bit result of the Hall sensor conversion (magnetic output).

Address 0x14: OP_MODE_CONF – Operational Mode Configurations

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x14	OP_MODE_CONF	0	INT_EN_DIR	INT_THRESHOLD_DIR						CONV_MODE_DIR		SLEEP_CFG_DIR	LPDCM_SLEEP_TIMER_DIR			OSR_FILTER_UPDATE_DIR	0

INT_EN_DIR [14]

Enables/disables the status condition (STATUS_FLAG) when the Hall sensor conversion (HALL_SENSOR_CONV) exceeds the threshold set by INT_THEREHOLD_DIR.

0: Disable threshold checking
1: Enable threshold checking

INT_THRESHOLD_DIR [13:8]

Sets the 6-bit threshold used to compare to the 6 MSBs of the HALL_SENSOR_CONV field. If the threshold is exceeded, the STATUS_FLAG field is set to 1.

CONV_MODE_DIR [7:6]

Sets the conversion mode.

2b00: Continuous conversion mode
2b01: One-shot mode
2b10: Continuous conversion mode
2b11: LPDCM mode

SLEEP_CFG_DIR [5]

Configures the functionality of the SLEEP pin input.

0: Sleep mode
1: Standby mode

LPDCM_SLEEP_TIMER_DIR [4:2]

Sets the LPDCM timer period.

3b000: 0.125 ms
3b001: 0.250 ms
3b010: 0.500 ms
3b011: 1.000 ms
3b100: 10.00 ms
3b101: 100.0 ms
3b110: 500.0 ms
3b111: 1000 ms

OSR_FILTER_UPDATE_DIR [1]

Sets the sample update filter.

0: 40 clock cycles for OSR update (faster, more noise)
1: 80 clock cycles for OSR update (slower, less noise)

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Address 0x16: CMDS – Commands

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x16	CMDS	0	0	SOFT_RST	START_SAMPLE	0	0	0	0	0	0	0	0	0	0	0	0

SOFT_RST [13]

Reset the signal path (soft reset).

START_SAMPLE [12]

Write field with value 1 to initiate a sample measurement. Write-only field (always reads back as 0).

Address 0x1A: ACCESS – Memory Access

Address	Register Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x1A	ACCESS	ACCESS_KEY															

ACCESS_KEY [15:0]

Writing the customer access code to ACCESS_KEY enables access to reading and writing the other registers accessible to the customer.

The access code is 32-bits and must be written in two separate and consecutive 16-bit writes to address 0x1A, MSBs first, then LSBs.

Customer access code: 0x43555354.

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INDIRECT MEMORY ACCESS

Indirect Memory Register Map [1]

Address	Register Name	Bit																														
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EEPROM_0	0	0	0	0	0	0	FACTORY				Y_DIE_LOC								X_DIE_LOC								EEPROM_REV					
0x01	EEPROM_1	0	0	0	0	0	0	FACTORY				FACTORY_LOT																FACTOR Y_WAFER					
0x03	EEPROM_3	0	0	0	0	0	0	D_IO_ INTERFACE	IIR_EN	FACTORY			OUT_MODE	POL	D_MAG_TC	D_SENS_ COARSE		FACTORY									OFFSET_ COARSE	FACTORY					
0x04	EEPROM_4	0	0	0	0	0	0	BW_FLT_SEL			I2C_SLV_ ADDR_ IGNORE	I2C_SLV_ADDR							INT_EN	INT_THRESHOLD						CONV_MODE		SLEEP_ CFG	LPDCM_SLEEP_TIMER		OSR_ FILTER_ UPDATE	OFFSET_ FINE_X2
0x23	SHADOW_3	0	0	0	0	0	0	D_IO_ INTERFACE	IIR_EN	FACTORY			OUT_MODE	POL	D_MAG_TC	D_SENS_ COARSE		FACTORY									OFFSET_ COARSE	FACTORY					
0x24	SHADOW_4	0	0	0	0	0	0	BW_FLT_SEL			I2C_SLV_ ADDR_ IGNORE	I2C_SLV_ADDR							INT_EN	INT_THRESHOLD						CONV_MODE		SLEEP_ CFG	LPDCM_SLEEP_TIMER		OSR_ FILTER_ UPDATE	OFFSET_ FINE_X2

[1] Fields with 0 must be written as 0 when writing to the register. Factory fields must be read with the value re-written when writing to the register to preserve factory settings.

Indirect Memory Register Reference

Address 0x00: EEPROM_0

Address	Register Name	Bit																														
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EEPROM_0	0	0	0	0	0	0	FACTORY				Y_DIE_LOC								X_DIE_LOC								EEPROM_REV					

Y_DIE_LOC [21:14]

8-bit Y-axis die location.

X_DIE_LOC [13:5]

8-bit X-axis die location.

EEPROM_REV [5:0]

EEPROM revision.

Address 0x01: EEPROM_1

Address	Register Name	Bit																														
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01	EEPROM_1	0	0	0	0	0	0	FACTORY				FACTORY_LOT																FACTOR Y_WAFER					

FACTORY_LOT [21:6]

Factory probe lot.

FACTORY_WAFER [5:0]

Factory wafer number.

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Address 0x03: EEPROM_3

Address	Register Name	Bit																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x03	EEPROM_3	0	0	0	0	0	0	D_IO_ INTERFACE	IIR_EN	FACTORY			OUT_MODE		POL	D_MAG_TC		D_SENS_ COARSE		FACTORY							OFFSET_ COARSE		FACTORY					

D_IO_INTERFACE [25]

Sets the IO reference voltage:

1b0: V_{DD}
1b1: Internal 1.8 V [1] low-voltage rail (for low-voltage interface)

IIR_EN [24]

Enables/disables the IIR filter:

1b0: IIR filter disabled
1b1: IIR filter enabled

OUT_MODE [20:19]

Sets the magnetic sensing mode:

2b00: Bipolar
2b01: Unipolar south
2b10: Unipolar north
2b11: Omnipolar

POL [18]

Sets the magnetic polarity:

1b0: Output increases with increasing south magnetic field
1b1: Output increases with increasing north magnetic field

D_MAG_TC [17:16]

Sets the sensitivity temperature coefficient:

2b00: Flat (0%/°C)
2b01: Ferrite (0.2%/°C)
2b10: Neodymium (0.12%/°C)
2b11: Samarium-cobalt (0.04%/°C)

D_SENS_COARSE [15:14]

Sets the coarse adjustment of the sensitivity:

2b00: VHF (very high field)
2b01: HF (high field)
2b10: MF (medium field)
2b11: LF (low field)

When using VHF, set OFFSET_FINE_X2 to 1b1

OFFSET_COARSE [6:5]

Sets the coarse adjustment of the offset for bipolar mode:

2b00: 25% of $V_{OUT(MAX)}$
2b01: 50% of $V_{OUT(MAX)}$
2b10: 50% of $V_{OUT(MAX)}$
2b11: 75% of $V_{OUT(MAX)}$

[1] Below supply voltages (V_{DD}) of 1.9 V, the internal low-voltage rail scales proportionally with the supply voltage from 1.8 V (with a supply voltage of 1.9 V) down to 1.55 V (with a supply voltage of 1.65 V).

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Address 0x04: EEPROM_4

Address	Register Name	Bit																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x04	EEPROM_4	0	0	0	0	0	0	BW_FLT_SEL			I2C_SLV_ADDR_IGNORE	I2C_SLV_ADDR							INT_EN	INT_THRESHOLD						CONV_MODE		SLEEP_CFG	LPDCM_SLEEP_TIMER			OSR_FILTER_UPDATE	OFFSET_FINE_X2

BW_FLT_SEL [25]

Sets the IIR filter bandwidth:

3b000: 95 Hz
3b001: 190 Hz
3b010: 376 Hz
3b011: 754 Hz
3b100: 1526 Hz
3b101: 3132 Hz
3b110: 6620 Hz
3b111: 15210 Hz

I2C_SLV_ADDR_IGNORE [22]

Enables/disables I²C peripheral address ignore:

1b0: Ignore disabled (checks if address is valid)
1b1: Ignore enabled (accepts any/all addresses)

I2C_SLV_ADDR [21:15]

Stores the digital address for responding to I²C commands. No functionality if I2C_SLV_ADDR_IGNORE is set to 1b0.

INT_EN [14]

Enables/disables the status condition (STATUS_FLAG) when the Hall sensor conversion (HALL_SENSOR_CONV) exceeds the threshold set by INT_THEREHOLD.

0: Disable threshold checking
1: Enable threshold checking

INT_THRESHOLD [13:8]

Sets the 6-bit threshold used to compare to the 6 MSBs of the HALL_SENSOR_CONV field. If the threshold is exceeded, the STATUS_FLAG field is set to 1.

CONV_MODE [7:6]

Sets the conversion mode.

2b00: Continuous conversion mode
2b01: One-shot mode
2b10: Continuous conversion mode
2b11: LPDCM mode

SLEEP_CFG [5]

Configures the functionality of the SLEEP pin input.

0: Sleep mode
1: Standby mode

LPDCM_SLEEP_TIMER_DIR [4:2]

Sets the LPDCM timer period.

3b000: 0.125 ms
3b001: 0.250 ms
3b010: 0.500 ms
3b011: 1.000 ms
3b100: 10.00 ms
3b101: 100.0 ms
3b110: 500.0 ms
3b111: 1000 ms

OSR_FILTER_UPDATE [1]

Sets the sample update filter.

0: 40 clock cycles for OSR update (faster, more noise)
1: 80 clock cycles for OSR update (slower, less noise)

OFFSET_FINE_X2 [0]

Corrects offset when D_SENS_COARSE = 2b00

0: Use for D_SENS_COARSE ≥ 2b01 (HF, MF, LF)
1: Use for D_SENS_COARSE = 2b00

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Address 0x23: SHADOW_3

Address	Register Name	Bit																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x23	SHADOW_3	0	0	0	0	0	0	D_IO_ INTERFACE	IIR_EN	FACTORY			OUT_MODE		POL	D_MAG_TC		D_SENS_ COARSE		FACTORY							OFFSET_ COARSE		FACTORY					

D_IO_INTERFACE [25]

Sets the IO reference:

1b0: V_{DD} (ratiometric interface)
1b1: Internal 1.8 V [1] low-voltage rail (for low-voltage interface)

IIR_EN [24]

Enables/disables the IIR filter:

1b0: IIR filter disabled
1b1: IIR filter enabled

OUT_MODE [20:19]

Sets the magnetic sensing mode:

2b00: Bipolar
2b01: Unipolar South
2b10: Unipolar North
2b11: Omnipolar

POL [18]

Sets the magnetic polarity:

1b0: Output increases with increasing South magnetic field
1b1: Output increases with increasing North magnetic field

D_MAG_TC [17:16]

Sets the sensitivity temperature coefficient:

2b00: Flat (0%/°C)
2b01: Ferrite (0.2%/°C)
2b10: Neodymium (0.12%/°C)
2b11: Samarium-cobalt (0.04%/°C)

D_SENS_COARSE [15:14]

Sets the coarse adjustment of the sensitivity:

2b00: VHF (very high field)
2b01: HF (high field)
2b10: MF (medium field)
2b11: LF (low field)

When using VHF, set OFFSET_FINE_X2 to 1b1

OFFSET_COARSE [6:5]

Sets the coarse adjustment of the offset for bipolar mode:

2b00: 25% of $V_{OUT(MAX)}$
2b01: 50% of $V_{OUT(MAX)}$
2b10: 50% of $V_{OUT(MAX)}$
2b11: 75% of $V_{OUT(MAX)}$

[1] Below supply voltages (V_{DD}) of 1.9 V, the internal low-voltage rail scales proportionally with the supply voltage from 1.8 V (with a supply voltage of 1.9 V) down to 1.55 V (with a supply voltage of 1.65 V).

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Address 0x24: SHADOW_4

Address	Register Name	Bit																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x24	SHADOW_4	0	0	0	0	0	0	BW_FLT_SEL			I2C_SLV_ADDR_IGNORE	I2C_SLV_ADDR							INT_EN	INT_THRESHOLD						CONV_MODE		SLEEP_CFG	LPDCM_SLEEP_TIMER			OSR_FILTER_UPDATE	OFFSET_FINE_X2

BW_FLT_SEL [25]

Sets the IIR filter bandwidth:

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I2C_SLV_ADDR [21:15]

Stores the digital address for responding to I²C commands. No functionality if I2C_SLV_ADDR_IGNORE is set to 1b0.

INT_EN [14]

Enables/disables the status condition (STATUS_FLAG) when the Hall sensor conversion (HALL_SENSOR_CONV) exceeds the threshold set by INT_THEREHOLD.

0: Disable threshold checking
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INT_THRESHOLD [13:8]

Sets the 6-bit threshold used to compare to the 6 MSBs of the HALL_SENSOR_CONV field. If the threshold is exceeded, the STATUS_FLAG field is set to 1.

CONV_MODE [7:6]

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SLEEP_CFG [5]

Configures the functionality of the SLEEP pin input.

0: Sleep mode
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LPDCM_SLEEP_TIMER [4:2]

Sets the LPDCM timer period.

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3b001: 0.250 ms
3b010: 0.500 ms
3b011: 1.000 ms
3b100: 10.00 ms
3b101: 100.0 ms
3b110: 500.0 ms
3b111: 1000 ms

OSR_FILTER_UPDATE [1]

Sets the sample update filter.

0: 40 clock cycles for OSR update (faster, more noise)
1: 80 clock cycles for OSR update (slower, less noise)

OFFSET_FINE_X2 [0]

Corrects offset when D_SENS_COARSE = 2b00

0: Use for D_SENS_COARSE ≥ 2b01 (HF, MF, LF)
1: Use for D_SENS_COARSE = 2b00

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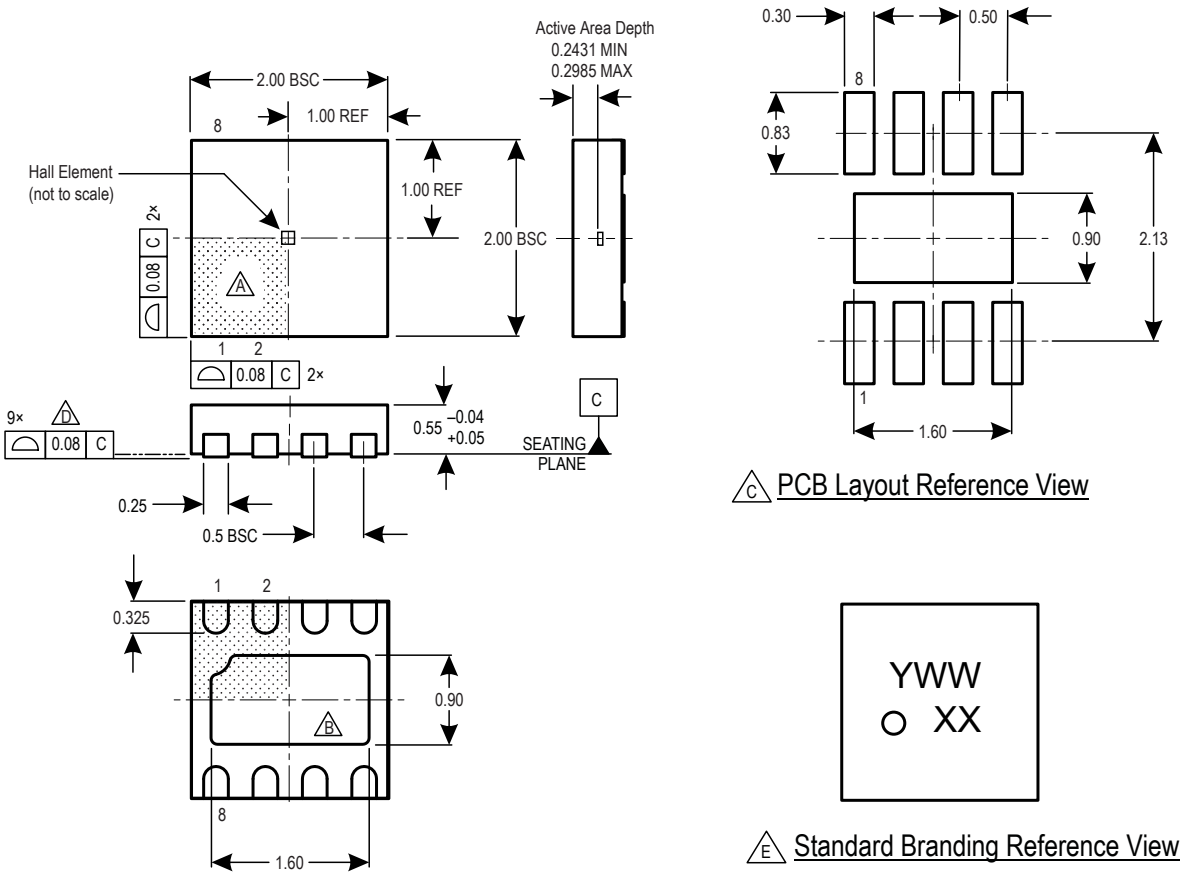
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000369)
NOT TO SCALE
All dimensions nominal unless otherwise stated – Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 27: Package EE, 8-Pin DFN

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Revision History

Number	Date	Description
–	December 9, 2025	Initial release

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