# A31331

## 3D Linear Hall-Effect Sensor
### with SPI, I²C Interfaces, and Advanced Low-Power Management

## FEATURES AND BENEFITS

- Flexible operating modes
  - Can measure input in any one, two, or three axes
  - 15-bit angle output from any selectable two-axis plane
- Low root-mean-square (RMS) angle noise for high system resolution
- SPI and I²C interfaces for easy system integration
  - Up to 10 MHz serial peripheral interface (SPI)
  - Up to 1 MHz inter-integrated circuit (I²C)
- Ideal for battery-powered, low-voltage applications
  - 2.65 to 3.6 V analog supply operation
  - 1.8 to 3.6 V digital supply operation
  - Low-leakage sleep ICC
  - Low-power duty cycle mode options for additional power savings
- Flexible multifunction pin for interrupt and sample-start functionality
  - Interrupt pin provides digital output when user-defined threshold is exceeded
- On-chip EEPROM for storing factory and customer-configured settings
- –40°C to 125ºC operation
- AEC-Q100, Grade 1 automotive qualified

## APPLICATIONS

- Valve position
- Shifter
- Human-machine interface (HMI)

## DESCRIPTION

The A31331 three-axis Hall-effect sensor integrated circuit (IC) is a flexible magnetic sensor capable of measuring the applied flux density in any one, two, or three axes, as well as calculating the angle in up to any of two user-defined planes. The A31331 comes in a standard field configuration of ±600 G. Additionally, the device is available preconfigured for SPI or I²C. The magnetic temperature coefficient is customer-programmable to support various magnet properties.

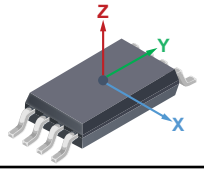
For ease of use, the A31331 supports two different digital interfaces: four-wire SPI or I²C. For high-speed applications, the SPI can operate at up to 10 MHz, and the I²C interface can operate at up to 1 MHz. The I²C address can be set by external resistors (16 unique addresses), or it can be programmed into EEPROM via I²C (127 unique addresses), allowing for multiple devices on the same bus.

Power management of the A31331 is highly configurable, allowing for system-level optimization of supply current and performance. Low-leakage sleep current makes the A31331 well-suited for portable, battery-operated applications.

The A31331 is supplied in an eight-pin thin-shrink small-outline package (TSSOP). The package is lead (Pb) free with 100% matte tin leadframe plating.

## PACKAGE: 8-Pin TSSOP (LE)

*Not to scale*



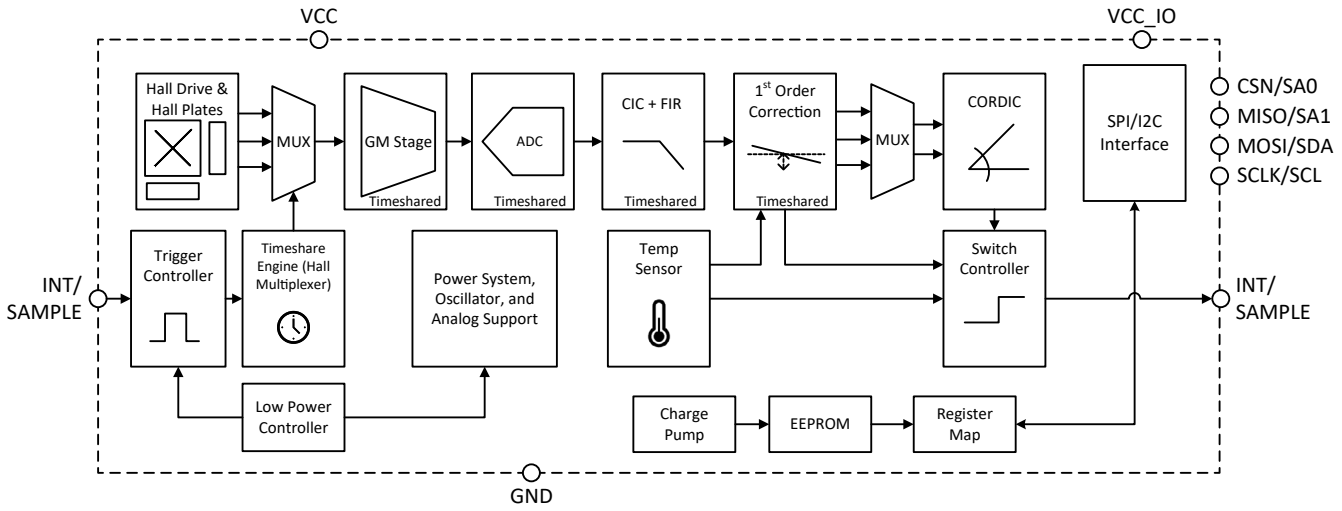



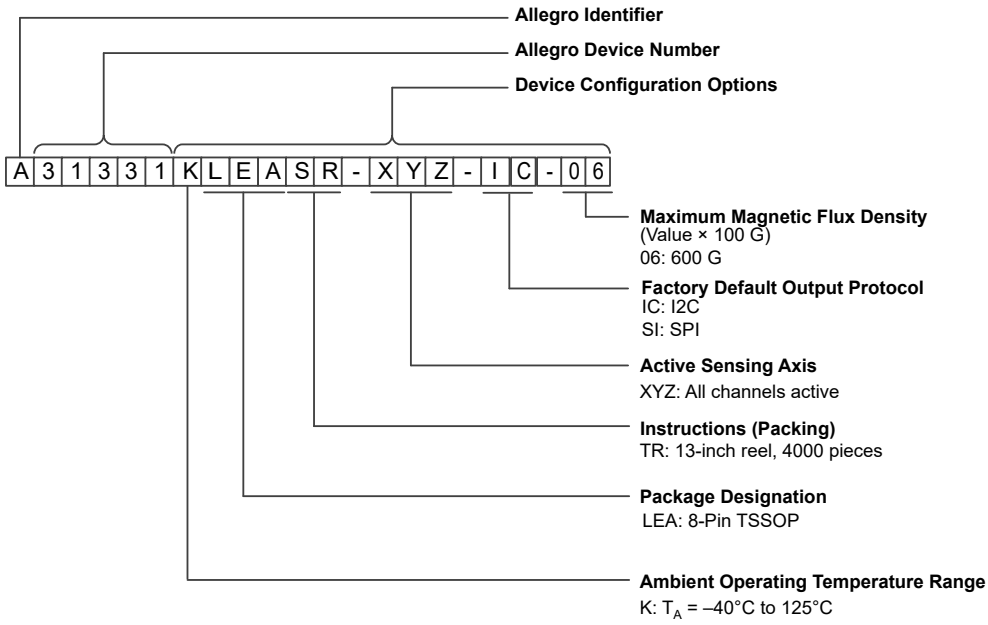

**Figure 1: Functional Block Diagram**

## SELECTION GUIDE

| Part Number | Default Interface | Supported Field Range (G) (Typ.) [1][2] | Packing [3] |
|---|---|---|---|
| A31331KLEATR-XYZ-IC-06 | I²C | ±600 | 4000 pieces per 13-inch reel |
| A31331KLEATR-XYZ-SI-06 | SPI | ±600 | |

[1] 1 gauss (G) = 0.1 millitesla (mT).
[2] For alternate field range options, contact Allegro.
[3] Contact Allegro™ for alternate packing options.

## NAMING SPECIFICATION






Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Forward Supply Voltage | $V_{CC}$ | | 3.6 | V |
| Reverse Supply Voltage | $V_{RCC}$ | | –0.5 | V |
| Forward IO Supply Voltage | $V_{CC(IO)}$ | | $V_{CC}$ | V |
| Reverse IO Supply Voltage | $V_{RCC(IO)}$ | | –0.5 | V |
| All Other Pins Forward Voltage | $V_{IN}$ | Digital IO Pins, SDA, SCL, SA0, SA1, SCLK, MISO, MOSI, CSN | $V_{CC(IO)}$ | V |
| All Other Pins Reverse Voltage | $V_R$ | | –0.5 | V |
| Operating Ambient Temperature | $T_A$ | Range K | –40 to 125 | °C |
| Maximum Junction Temperature | $T_{J(MAX)}$ | | 165 | °C |
| Storage Temperature [1] | $T_{stg}$ | | –65 to 170 | °C |
| EEPROM Write Count [2] | – | Number of times EEPROM can be written | 100 | writes |

[1] Stress beyond the absolute maximum rating might result in permanent device damage. Exposure to absolute maximum rating conditions for extended periods of time might affect device reliability.
[2] EEPROM writes are not supported at temperatures greater than 85°C.

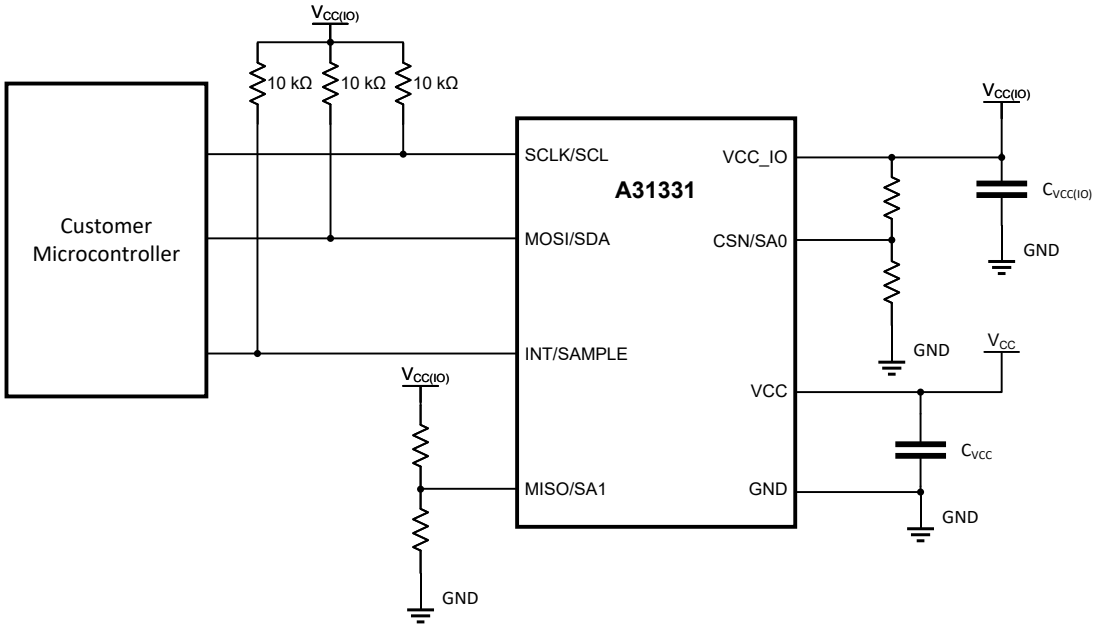
## THERMAL CHARACTERISTICS [1]

| Characteristic | Symbol | Test Conditions | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance [2] | $R_{\theta JA}$ | On four-layer printed circuit board (PCB) based on JEDEC standard | 145 | °C/W |

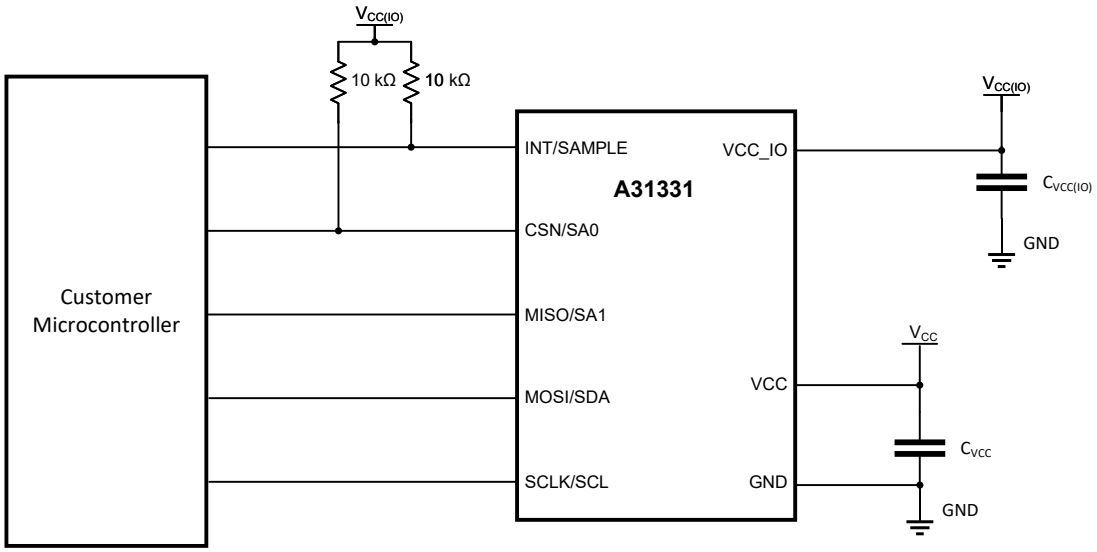
[1] Thermal characteristics might require derating at maximum conditions.
[2] Additional thermal information is available on the Allegro website.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com




(a) I²C Interface



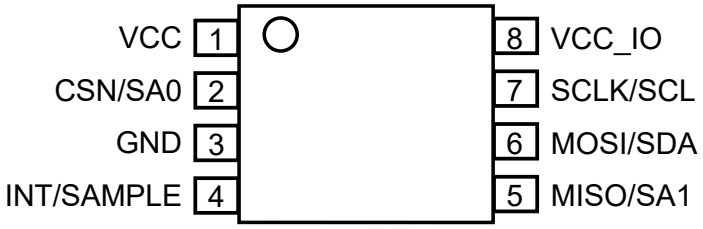

(b) SPI Interface

**Figure 2: Typical Application Circuits**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## PINOUT DIAGRAM AND TERMINAL LIST




**Package LE, 8-Pin TSSOP Pinout Diagram**

### Terminal List Table

| Number | Name | Function |
|---|---|---|
| 1 | VCC | Power supply input. Bypass VCC to GND with a 0.1 µF capacitor. |
| 2 | CSN/SA0 | CSN: SPI chip select, active low.<br>SA0: I²C address select 0. To select the device address, connect a resistive divider to SA0.<br>For more information about addressing, see the Application Information section. |
| 3 | GND | Ground signal terminal. |
| 4 | INT/ SAMPLE | INT: Interrupt output. For more information about the interrupt function, see the Application Information section.<br>SAMPLE: Sample trigger Input. For more information about the sample function, see the Application Information section.<br><br>If this functionality is not used and is disabled, it is recommended to tie this pin to ground. |
| 5 | MISO/SA1 | MISO (controller-in peripheral-out): SPI output<br>SA1: I²C address select 1. To select the device address, connect a resistive divider to SA1.<br>For more information about addressing, see the Application Information section. |
| 6 | MOSI/SDA | MOSI (controller-out peripheral-in): SPI input.<br>SDA: I²C serial data input/output. Open-drain. |
| 7 | SCLK/SCL | SCLK: SPI serial clock input.<br>SCL: I²C serial clock input. |
| 8 | VCC_IO | Voltage reference for digital input/output (IO) pins. |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**ELECTRICAL CHARACTERISTICS:** Valid at $T_A$ = 25°C, $V_{CC}$ = $V_{CC\_IO}$ = 3 V, $C_{BYPASS}$ = 0.1 µF, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage | $V_{CC}$ | Typical operation | 2.65 | 3 | 3.6 | V |
| | | EEPROM programming [1] | 2.8 | – | 3.5 | V |
| Supply Voltage Ramp[2] | $V_{CC\_RAMP}$ | Ramp rate from 0 to 3.3 V | 0.1 | – | 10000 | µs |
| Digital Supply Voltage | $V_{CC\_IO}$ | $V_{CC\_IO} \le V_{CC}$ | 1.7 | – | $V_{CC}$ | V |
| Supply Current [3] | $I_{CC(ACTIVE)}$ | Active state | – | 3.8 | 4.75 | mA |
| | $I_{CC(INACTIVE)}$ | OP_MODE = 5, 6; inactive state | – | 25 | – | µA |
| | $I_{CC(LPDCM)}$ | Average current in LPDCM; OP_MODE = 6, SLEEP_CNT = 7, CIC_BW_SEL_LPM = 6 | – | 25 | – | µA |
| | | Average current in LPDCM; OP_MODE = 6, SLEEP_CNT = 0, CIC_BW_SEL_LPM = 0 | – | 2 | – | mA |
| | $I_{CC(SLEEP)}$ | $V_{CC}$ = 3 V, OP_MODE = 3, 4 [4] | – | 2.5 | – | µA |
| | $I_{CC(EE)}$ | $V_{CC}$ = $V_{CC(MAX)}$, EEPROM programming occurring [2] | – | 6.2 | – | mA |
| | $I_{CC\_IO}$ | Current consumption on VCC_IO | – | 25 | – | µA |
| Power-On Reset | $V_{POR}$ | Minimum $V_{CC}$ before turn-on | – | 2.51 | – | V |
| Power-On Delay Time [5] | $t_{POD}$ | $T_A$ = 25°C, after $V_{CC}$ reaches $V_{CC(MIN)}$, BW select = 0 | 1 | – | – | ms |
| EEPROM Write Delay Time | $t_{EEP}$ | Wait after writing to EEPROM | – | 50 | – | ms |
| Linearity Sensitivity Error | $E_{LIN}$ | Through full range of $B_{IN}$ | – | ±1.7 | – | % |
| **INT PIN CHARACTERISTICS** | | | | | | |
| INT Output On Resistance | $R_{ON}$ | | – | 90 | – | Ω |
| INT Input Current | $I_{INT(IN)}$ | $V_{IN}$ = 0 V to $V_{CC}$ | –1 | 0 | 1 | µA |
| INT Pull Up Resistance | $R_{INT(PU)}$ | | 2.4 | 10 | – | kΩ |
| INT Pull Up Voltage | $V_{INT(PU)}$ | | – | 3 | 3.6 | V |
| **ADDRESS PIN CHARACTERISTICS [2]** | | | | | | |
| Address Value 0 Reference | $V_{ADDR0}$ | SA0, SA1 | – | 0 | 0.1 | × $V_{CC\_IO}$ |
| Address Value 1 Reference | $V_{ADDR1}$ | SA0, SA1 | 0.23 | 0.33 | 0.43 | × $V_{CC\_IO}$ |
| Address Value 2 Reference | $V_{ADDR2}$ | SA0, SA1 | 0.57 | 0.67 | 0.77 | × $V_{CC\_IO}$ |
| Address Value 3 Reference | $V_{ADDR3}$ | SA0, SA1 | 0.9 | 1 | – | × $V_{CC\_IO}$ |
| Address Pin Input Resistance | $R_{ADD(IN)}$ | SA0, SA1 | 0.8 | 1 | 1.2 | MΩ |

[1] Parameter is tested at wafer probe only.
[2] Parameter not measured at final test. Determined by design and characterization.
[3] $I_{CC}$ varies based on lower-power duty cycle settings. For more information about power modes, see the Application Information section.
[4] In OP_MODE = 4: $I_{CC(SLEEP)}$ occurs during the idle window. When a conversion is requested, the device draws the same current as $I_{CC(ACTIVE)}$. The average $I_{CC}$ is dependent on the user-set sampling rate.
[5] Minimum time to delay after power-on before initiating communications. The device does not respond to I²C or SPI inputs until after the power-on delay time, $t_{POD}$, which varies based on the bandwidth (BW) select code, where code 0 is the longest duration.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**I²C INTERFACE CHARACTERISTICS [1]:** Valid at $T_A$ = 25°C, $V_{CC}$ = $V_{CC\_IO}$ = 3 V, $C_{BYPASS}$ = 0.1 µF, $R_{PU}$ = 10 kΩ, and I²C clock speed (FCLK) = 400 kHz, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Bus Free Time Between Stop and Start | $t_{BF}$ | OP_MODE = 0, 1, 2 | 1.3 | – | – | µs |
| | | OP_MODE = 5, 6 | 25 | – | – | µs |
| Hold Time Start Condition | $t_{STA(H)}$ | | 0.6 | – | – | µs |
| Setup Time for Repeated Start Condition | $t_{STA(S)}$ | | 0.6 | – | – | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | – | – | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | – | – | µs |
| Data Setup Time | $t_{DAT(S)}$ | | 100 | – | – | ns |
| Data Hold Time | $t_{DAT(H)}$ | | 0 | – | 900 | ns |
| Setup Time for Stop Condition | $t_{STO(S)}$ | | 0.6 | – | – | µs |
| Logic Input Low Level (SDA, SCL Pins) | $V_{I(L)}$ | I2C_THRESH_SEL = 0; 3 V-compatible mode | – | – | 0.9 | V |
| | | I2C_THRESH_SEL = 1; 1.8 V-compatible mode | – | – | 0.54 | V |
| Logic Input High Level (SDA, SCL Pins) | $V_{I(H)}$ | I2C_THRESH_SEL = 0; 3 V-compatible mode | 2.1 | – | – | V |
| | | I2C_THRESH_SEL = 1; 1.8 V-compatible mode | 1.26 | – | – | V |
| Logic Input Current | $I_{I2C(IN)}$ | $V_{IN}$ = 0 V to $V_{CC}$, $R_{PU}$ = 2.4 kΩ | –1 | 0 | 1 | µA |
| Output Voltage (SDA Pin) | $V_{O(L)}$ | $I_{LOAD}$ = 1.5 mA | – | – | 0.36 | V |
| Clock Frequency (SCL Pin) | $f_{CLK}$ | | – | 400 | 1000 | kHz |
| Output Fall Time (SDA Pin) | $t_f$ | $R_{PU}$ = 2.4 kΩ, $C_{BUS}$ = 100 pF | – | – | 250 | ns |
| I²C Pull-Up Resistance | $R_{I2C(PU)}$ | | 2.4 | 10 | – | kΩ |
| I²C Pull-Up Voltage | $V_{I2C(PU)}$ | | 1.8 | 3 | 3.3 | V |
| Total Capacitive Load for SDL and SDA Buses | $C_{BUS}$ | | – | – | 100 | pF |

[1] I²C interface characteristics are not measured at final test. Determined by design and characterization.

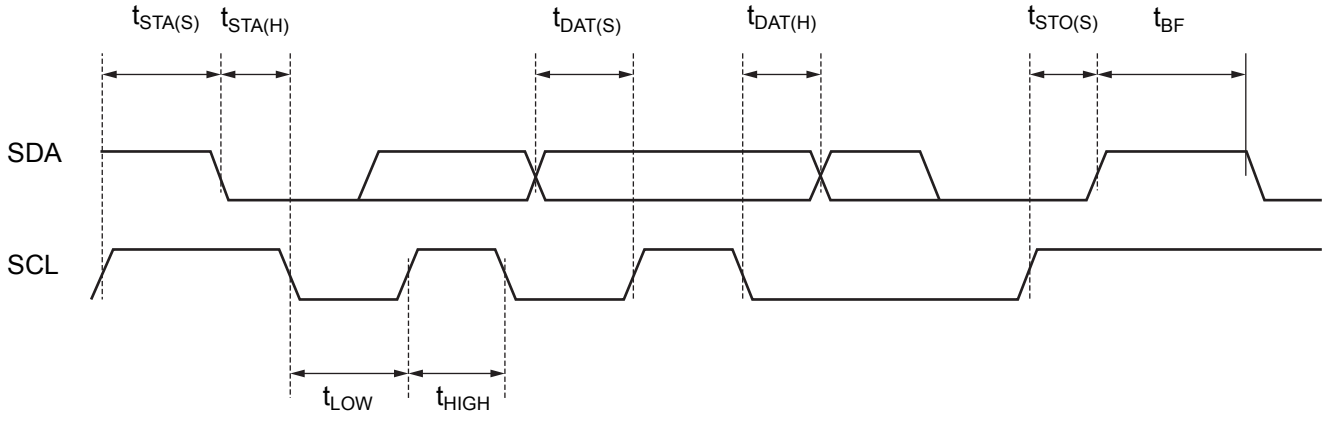



**Figure 3: I²C Interface Timing Diagram**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**SPI INTERFACE CHARACTERISTICS:** Valid at $T_A$ = 25°C, $C_{BYPASS}$ = 0.1 µF, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SPI INTERFACE SPECIFICATIONS** | | | | | | |
| SPI Packet Size | $N_{SPI}$ | Number of bits per SPI transaction, with and without cyclic redundancy check (CRC) | 16 | – | 20 | bits |
| Digital Input High Voltage | $V_{IH}$ | MOSI, SCLK, CSN pins | 0.65 | – | 1 | × $V_{CC\_IO}$ |
| Digital Input Low Voltage | $V_{IL}$ | MOSI, SCLK, CSN pins | – | – | 0.35 | × $V_{CC\_IO}$ |
| SPI Output High Voltage | $V_{OH}$ | MISO pins, $C_L$ = 10 pF | – | – | – | V |
| SPI Output Low Voltage | $V_{OL}$ | MISO pins, $C_L$ = 10 pF | – | – | – | V |
| SPI Clock Frequency | $f_{SPI}$ | | 0.1 | – | 10 | MHz |
| SPI Duty Cycle | $D_{fSCLK}$ | $SPICLK_{DC}$ | 40 | – | 60 | % |
| SPI Frame Rate | $t_{SPI}$ | | 5.8 | – | 588 | kHz |
| Chip Select to First SCK Edge | $t_{CS}$ | Time from CSN going low to SCLK falling edge | 50 | – | – | ns |
| Chip Select Idle Time | $t_{CS\_IDLE}$ | OP_MODE = 0, 1, 2 | 425 | – | – | ns |
| | | OP_MODE = 5, 6 | 37.5 | – | – | µs |
| Data Out Valid Time | $t_{DAV}$ | Data output valid after SCLK falling edge | – | 30 | – | ns |
| MOSI Setup Time | $t_{SU}$ | Input setup time before SCLK rising edge | 25 | – | – | ns |
| MOSI Hold Time | $t_{HD}$ | Input hold time after SCLK rising edge | 50 | – | – | ns |
| MISO Off Time | $t_{off}$ | Time from CSN going high to MISO tri-stating | – | 45 | – | ns |
| SCLK to CS Hold Time | $t_{CHD}$ | Hold SCLK high time before CS rising edge | 5 | – | – | ns |
| Load Capacitance | $C_L$ | Loading on digital output (MISO) pin, $V_{CC\_IO}$ = 3.3 V | – | – | 10 | pF |

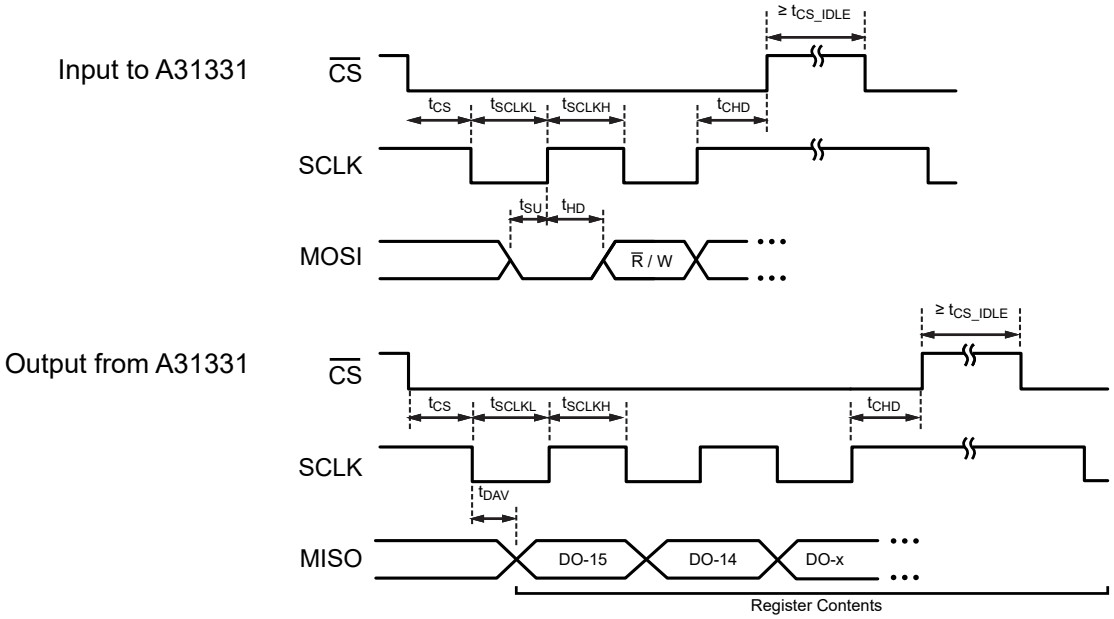



**Figure 4: SPI Interface Timings: Input (Top) and Register Output (Bottom)**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**A31331KLEA-XYZ-06 PERFORMANCE CHARACTERISTICS:** Valid at $V_{CC}$ = 3 V, and $C_{BYPASS}$ = 0.1 µF, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **NOMINAL PERFORMANCE** | | | | | | |
| Optimized Sensing Range | $B_{IN}$ | | – | ±600 | – | G |
| Sensitivity | SENS | $T_A$ = 25°C | – | 24.82 | – | LSB/G |
| Sensitivity Temperature Coefficient | $SENS_{TC}$ | –40°C < $T_A$ < 125°C | – | 0.04 | – | %/°C |
| Zero-Field Offset Code | OFF | $B_{IN}$ = 0 G, –40°C < $T_A$ < 125°C | – | 0 | – | LSB |
| **NOISE CHARACTERISTICS [2]** | | | | | | |
| RMS Noise X/Y Channels [3] | $N_{RMS(XY)}$ | BW select = 0 | – | 0.1 | – | G |
| | | BW select = 6 | – | 0.8 | – | G |
| RMS Noise Z Channel [3] | $N_{RMS(Z)}$ | BW select = 0 | – | 0.052 | – | G |
| | | BW select = 6 | – | 0.414 | – | G |
| RMS Angle Noise [3] | $N_{RMS(\theta XY)}$ | BW select = 0, $B_{IN}$ = 300 G | – | 0.02 | – | ° |
| **ACCURACY PERFORMANCE** | | | | | | |
| Offset Error X/Y Axes | $E_{OFF(XY)}$ | $B_{IN}$ = 0 G, $T_A$ = 25°C | –6 | – | 6 | G |
| | | $B_{IN}$ = 0 G, –40°C < $T_A$ < 125°C | –6 | – | 6 | G |
| Offset Error Z Axis | $E_{OFF(Z)}$ | $B_{IN}$ = 0 G, $T_A$ = 25°C | –6 | – | 6 | G |
| | | $B_{IN}$ = 0 G, –40°C < $T_A$ < 125°C | –6 | – | 6 | G |
| Sensitivity Error X/Y Axes | $E_{SENS(XY)}$ | $T_A$ = 25°C | –2.5 | – | 2.5 | % |
| | | 25°C < $T_A$ < 125°C | –4 | – | 4 | % |
| | | –40°C < $T_A$ < 25°C | –5.2 | – | 5.2 | % |
| Sensitivity Error Z Axis | $E_{SENS(Z)}$ | $T_A$ = 25°C | –3.5 | – | 3.5 | % |
| | | 25°C < $T_A$ < 125°C | –4 | – | 4 | % |
| | | –40°C < $T_A$ < 25°C | –5.2 | – | 5.2 | % |
| Sensitivity Mismatch Error X Axis to Y Axis | $E_{MATCH(XY)}$ | $T_A$ = 25°C | –1.1 | – | 1.1 | % |
| | | –40°C < $T_A$ < 125°C | –1.1 | – | 1.1 | % |
| Sensitivity Mismatch Error X/Y Axes to Z Axis | $E_{MATCH(XZ,YZ)}$ | $T_A$ = 25°C | –3 | – | 3 | % |
| | | –40°C < $T_A$ < 125°C | –4 | – | 4 | % |
| Orthogonality Error, X-Y Plane | $E_{ORTHO(XY)}$ | $T_A$ = 25°C | –1.75 | – | 1.75 | ° |
| | | –40°C < $T_A$ < 125°C | –2 | – | 2 | ° |
| Angle Error X-Y Plane | $E_{ANG(XY)}$ | $B_{IN}$ ≥ 300 G, $T_A$ = 25°C | –1.5 | – | 1.5 | ° |
| | | $B_{IN}$ ≥ 300 G | –2 | – | 2 | ° |
| Angle Error X-Z, Y-Z Plane [3] | $E_{ANG(XZ,YZ)}$ | $B_{IN}$ ≥ 300 G, $T_A$ = 25°C | –2 | – | 2 | ° |
| | | $B_{IN}$ ≥ 300 G | –2.5 | – | 2.5 | ° |

[1] 1 G (gauss) = 0.1 mT (millitesla)
[2] RMS noise equivalent to 1 standard deviation (sigma) distribution.
[3] Parameter not measured at final test. Determined by design and characterization.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**A31331KLEA-XYZ-06 PERFORMANCE CHARACTERISTICS (continued):** Valid at $V_{CC}$ = 3 V, and $C_{BYPASS}$ = 0.1 µF, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **DRIFT CHARACTERISTICS—TEMPERATURE** | | | | | | |
| Offset Drift X/Y Axes | $D_{OFF,TEMP(XY)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | –4 | – | 4 | G |
| Offset Drift Z Axis | $D_{OFF,TEMP(Z)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | –4 | – | 4 | G |
| Sensitivity Drift X/Y Axes | $D_{SENS,TEMP(XY)}$ | 25°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | 0.00 | – | 0.08 | %/°C |
| | | –40°C < $T_A$ < 25°C, relative to $T_A$ = 25°C | –0.04 | – | 0.12 | %/°C |
| Sensitivity Drift Z Axis | $D_{SENS,TEMP(Z)}$ | 25°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | 0.00 | – | 0.08 | %/°C |
| | | –40°C < $T_A$ < 25°C, relative to $T_A$ = 25°C | –0.04 | – | 0.12 | %/°C |
| Sensitivity Mismatch Error Drift X Axis to Y Axis | $D_{MATCH,TEMP(XY)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | –1.5 | – | 1.5 | % |
| Sensitivity Mismatch Error Drift X/Y Axes to Z Axis | $D_{MATCH,TEMP(XZ,YZ)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | –3.5 | – | 3.5 | % |
| Orthogonality Error Drift, X-Y Plane | $D_{ORTHO,TEMP(XY)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C | –1.5 | – | 1.5 | ° |
| Angle Error Drift, X-Y Plane | $D_{ANG,TEMP(XY)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C, $B_{IN}$ ≥ 300 G | –1.1 | – | 1.1 | ° |
| Angle Error Drift, X-Z, Y-Z Plane [3] | $D_{ANG,TEMP(XZ,YZ)}$ | –40°C < $T_A$ < 125°C, relative to $T_A$ = 25°C, $B_{IN}$ ≥ 300 G | –1.5 | – | 1.5 | ° |

[1] 1 G (gauss) = 0.1 mT (millitesla)
[2] Lifetime Drift Characteristics will be based on worst-case error or drift seen during device qualification.
[3] Parameter not measured at final test. Determined by design and characterization.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**A31331KLEA-XYZ-06 PERFORMANCE CHARACTERISTICS (continued):** Valid at $V_{CC}$ = 3 V, and $C_{BYPASS}$ = 0.1 µF, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **DRIFT CHARACTERISTICS—TEMPERATURE AND LIFETIME** [2] | | | | | | |
| Offset Drift X/Y Axes | $D_{OFF,LIFE(XY)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | –3 | – | 3 | G |
| Offset Drift Z Axis | $D_{OFF,LIFE(Z)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | –2 | – | 2 | G |
| Sensitivity Drift X/Y Axes | $D_{SENS,LIFE(XY)}$ | 25°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | 0.00 | – | 0.08 | %/°C |
| | | –40°C < $T_A$ < 25°C, Relative to $T_A$ = 25°C pre-stress conditions | –0.04 | – | 0.12 | %/°C |
| Sensitivity Drift Z Axis | $D_{SENS,LIFE(Z)}$ | 25°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | 0.00 | – | 0.11 | %/°C |
| | | –40°C < $T_A$ < 25°C, Relative to $T_A$ = 25°C pre-stress conditions | –0.07 | – | 0.04 | %/°C |
| Sensitivity Mismatch Error Drift X Axis to Y Axis | $D_{MATCH,LIFE(XY)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | –1.5 | – | 1.5 | % |
| Sensitivity Mismatch Error Drift X/Y Axes to Z Axis | $D_{MATCH,LIFE(XZ,YZ)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | –4.5 | – | 4.5 | % |
| Orthogonality Error Drift, X-Y Plane | $D_{ORTHO,LIFE(XY)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions | –2.6 | – | 2.6 | ° |
| Angle Error Drift, X-Y Plane | $D_{ANG,LIFE(XY)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions, $B_{IN}$ ≥ 300 G | –1.6 | – | 1.6 | ° |
| Angle Error Drift, X-Z, Y-Z Plane | $D_{ANG,LIFE(XZ,YZ)}$ | –40°C < $T_A$ < 125°C, Relative to $T_A$ = 25°C pre-stress conditions, $B_{IN}$ ≥ 300 G | –2.25 | – | 2.25 | ° |

[1] 1 G (gauss) = 0.1 mT (millitesla)
[2] Lifetime drift characteristics are based on the worst-case error or drift observed during device AEC-Q100 Grade 1 quality stress testing.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## APPLICATION INFORMATION

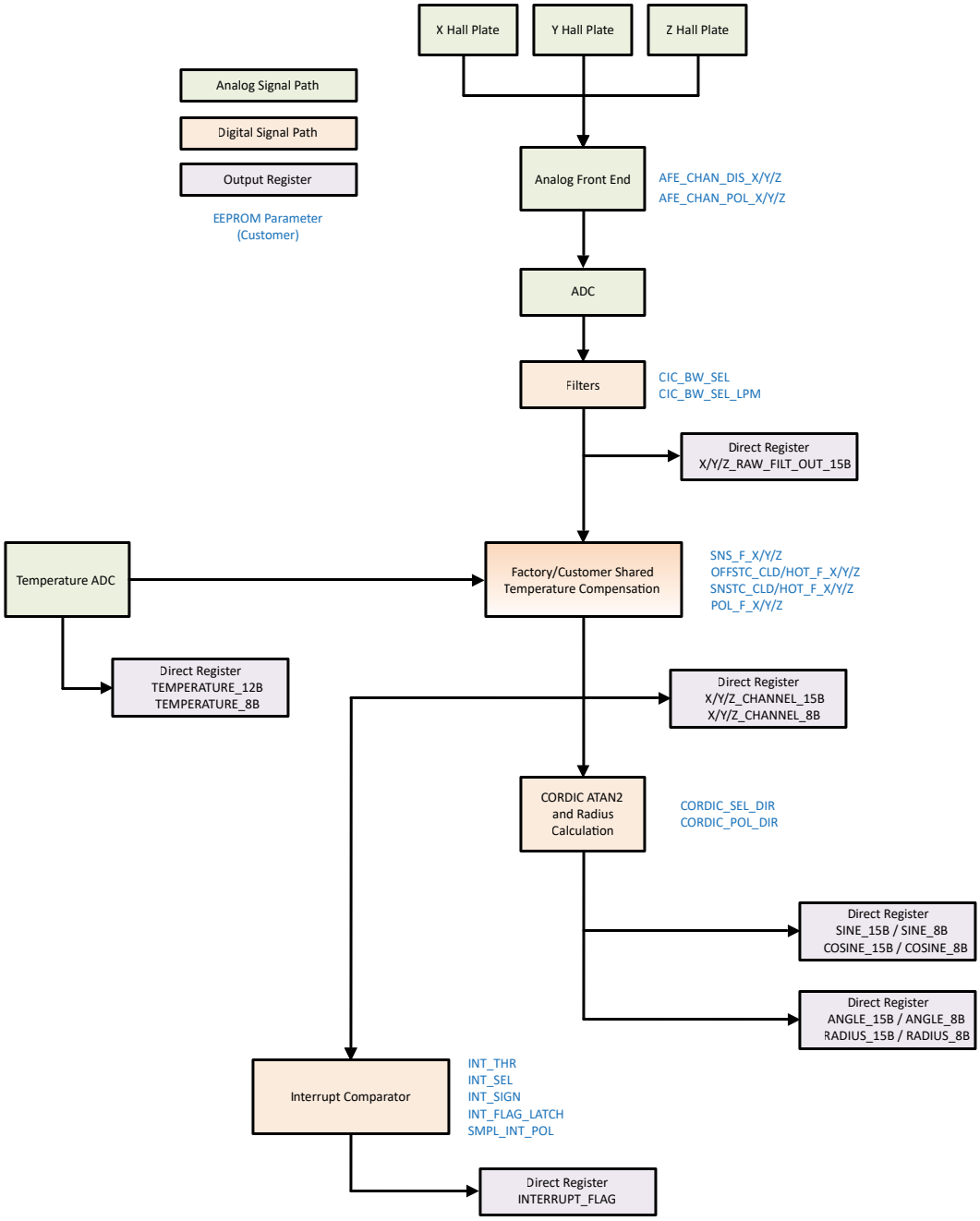



**Figure 5: A31331 Signal Path**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Magnetic Sensor(s) Output

The A31331 provides 8-bit and 15-bit digital output value options that are proportional to the magnetic field that is typically applied to any of the Hall elements as the X-, Y-, and Z-channels. Each channel is factory-trimmed for sensitivity and offset accuracy at room temperature, as well as with a target temperature compensation. For additional adjustment in application, the room sensitivity and sensitivity parameter and the offset temperature compensation parameter are accessible by the customer. This allows the A31331 to be used in both rotary and linear position applications in any mounting orientation relative to the sensing magnet and to provide high accuracy and matching as the device and magnetic system changes over temperature. Starting with the raw filter output, which can be read in registers X/Y/Z_RAW_FILT_OUT_15B, the single-dimension magnetic data is corrected through the following steps:

$A = X/Y/Z\_RAW\_FILT\_OUT\_15B + Factory\ Offset\ Correction$

$B = A \times SENS\_F\_X/\_Y/\_Z \times -1^{(POL\_F\_X/Y/Z)}$

$C = B + (OFFSTC\_HOT/CLD\_F\_X/Y/Z \times Temperature)$

$X/Y/Z\_CHANNEL\_15B = C \times (SENSTC\_HOT/CLD\_F\_X/Y/Z \times Temperature)$

The A31331 features an internal ATAN calculation on any two of the three user-selectable axes, X, Y, or Z. One of the channels is designated as the sine channel, and the other is designated as the cosine channel. This is performed with the indirect extended-space EEPROM parameter CORDIC_SEL or the volatile direct primary-space parameter CORDIC_SEL_DIR.

**Table 1: CORDIC_SEL Decode**

| CORDIC_SEL | COSINE Channel | SINE Channel |
|---|---|---|
| 0 | X | Y |
| 1 | X | Z |
| 2 | Y | Z |
| 3 | Y | X |
| 4 | Z | X |
| 5 | Z | Y |
| 6 | X | Y |
| 7 | X | Y |

The sine channel is stored in the direct primary-space registers SIN_8B and SINE_15B. The cosine channel is stored in the direct primary-space registers COS_8B and COSINE_15B.

The angle between the magnetic vectors selected by the sine and cosine channels is taken as the ATAN, following the equation:

$$\theta = \tan^{-1}\frac{\sin\theta}{\cos\theta}$$

This angle can have an inverted polarity, decreasing code output with increasing input angle using the CORDIC_POL parameter.

$$Angle_{Out} = \begin{cases} Angle_{in} & for\ CORDIC\_POL = 0 \\ 360° - Angle_{in} & for\ CORDIC\_POL = 1 \end{cases}$$

Polarity can also be adjusted after power-on in the volatile direct primary-space register CORDIC_POL_DIR. The angle output is stored in the direct-space registers ANGLE_8B and ANGLE_15B.

While calculating the angle, digital processing also tracks the magnitude of the angle vector from the sine and cosine channels as the radius squared, following the equation:

$$radius^2 = cosine^2 + sine^2$$

This radius-squared value is stored in the direct-space registers RADIUS_SQ_8B and RADIUS_15B.

## Temperature Sensor Output

The A31331 provides a 12-bit digital output that is proportional to the junction temperature of the IC. Temperature can be calculated by:

$$Temp\ [°C] = \frac{TEMPERATURE\_12B}{8.052} + 25$$

## Special Function Pin INT/SAMPLE

The A31331 has a special function pin, INT/SAMPLE, that can be set as either an output as an interrupt pin, or an input as a sample request pin, depending on the configured power mode.

### SAMPLE MODE

While in sample mode, the special function pin acts as an input and can trigger a request to start a new conversation of the magnetic signal. This allows the host/user to synchronize the acquisition of the magnetic data. The device remains in a standby mode (no data acquisition) until either the INT/SAMPLE pin is brought high or the direct register START_SAMPLE bit is set by the host. When this pin transitions to active (defined by SAMPLE_INT_POLARITY_DIR) or when the START_SAMPLE bit is set, a sample is triggered. The front end acquires data, the output registers are updated with the new data, the output registers are set, the STATUS_READY flag asserts, and the device returns to standby. This mode is particularly useful for signal-processing applications that are sensitive to time/speed considerations (such as feedback and control applications) where deterministic sam-



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

pling is critical for loop stability.

If the device is in the process of acquiring new data from an initial sample request, subsequent sample signals are ignored. Data registers are updated only once per INT/SAMPLE pin or START_SAMPLE write trigger. If DATA_LATCH = 1, the STATUS_READY bit must be cleared by the host writing a one to the bit once the reading of the stored data is complete, in order to allow a new acquisition to occur.

## INTERRUPT MODE

When the pin is in interrupt mode, the special function pin is an output and is used to indicate when a certain internal threshold is surpassed. The threshold of interest is set by the direct-space INTERRUPT_SEL_DIR register or the indirect-space INT_SEL parameter and is compared to the programmed threshold in INTERRUPT_THR_MSB/LSB_DIR in the direct space, loaded from INT_THR in the indirect space. When the selected threshold condition is met, the interrupt flag becomes set in the direct-space register INTERRUPT_FLAG and through the INT/SAMPLE pin. The INTERRUPT_FLAG direct-space bit always remains asserted once it is set and, after the interrupt condition is removed, it must be cleared by writing it to a 1. If the parameter INTERRUPT_FLAG_LATCH_DIR is set, the INT pin status also becomes latched until the INTERRUPT_FLAG bit is written to a 1. In low-power mode, the flag requires 20 µs to clear after the write.

**Table 2: Interrupt Selection Options, THR set by INTERRUPT_THR_MSB/LSB_DIR in Direct Space**

| INTERRUPT_SEL_ DIR/INT_SEL | Condition (INTERRUPT_SIGN_DIR = 0) | Threshold Register | Description |
|---|---|---|---|
| 0 | THR > X | SIGNED | Threshold register is compared to the trimmed X output |
| 1 | THR > Y | SIGNED | Threshold register is compared to the trimmed Y output |
| 2 | THR > Z | SIGNED | Threshold register is compared to the trimmed Z output |
| 3 | THR > ABS(X) | UNSIGNED | Threshold register is compared to the absolute value of the trimmed X output |
| 4 | THR > ABS(Y) | UNSIGNED | Threshold register is compared to the absolute value of the trimmed Y output |
| 5 | THR > ABS(Z) | UNSIGNED | Threshold register is compared to the absolute value of the trimmed Z output |
| 6 | THR > TEMP | SIGNED | Threshold register is compared to the temperature output |
| 7 | THR > ANGLE | UNSIGNED | Threshold register is compared to the angle output |
| 8 | THR > RADIUS | UNSIGNED | Threshold register is compared to the radius output |
| 9 | THR = New Sample | – | No comparison; pin provides one 10 µs pulse that occurs when data is valid |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Operation Modes

Power management on the A31331 is user-selectable and highly configurable, allowing for system-level optimization of current consumption and performance. The A31331 supports three different power modes: active mode, sleep mode, and low-power duty cycle mode (LPDCM), each with various subconfigurations using the special function pin INT/SAMPLE. The operating mode of the A31331 is determined by the value in the OP_MODE field, in direct-space address [0x32:0x33], bits [3:1], described in Table 3.

### ACTIVE MODE

In active mode, the A31331 continuously updates the channel and angle outputs at an interval defined by the bandwidth selection. This mode requires the most power but provides output register updates at the highest frequency. In addition to the standard output of active mode, the OP_MODE register can be configured to set the device in active mode with the interrupt output enabled.

### SLEEP MODE

In sleep mode, the A31331 enters a near powered-off state where it consumes the minimum amount of current. In this mode, the device continues to respond to I²C or SPI commands, but it does not update magnetic or temperature data. In OP_MODE = 4, sleep mode with sample wake, the device operates similarly to full-sleep mode, but it also monitors the INT/SAMPLE pin or START_SAMPLE bit for a trigger to start a conversion. This allows the host to set a conversion frequency to best balance power and response time in the system. Sleep mode is valuable in applications where the supply voltage cannot be disabled but minimal power consumption is required. The time it takes to exit sleep mode is equivalent to the power-on delay time ($t_{POD}$).

### LOW-POWER DUTY CYCLE MODE (LPDCM)

In low-power duty cycle mode (LPDCM), the A31331 toggles between the active and inactive states, reducing overall current consumption. During LPDCM, the average $I_{CC}$ for the A31331 varies based on the device configuration. The profile of $I_{CC}$ as the A31331 toggles between active and inactive states during LPDCM is shown in Figure 6.

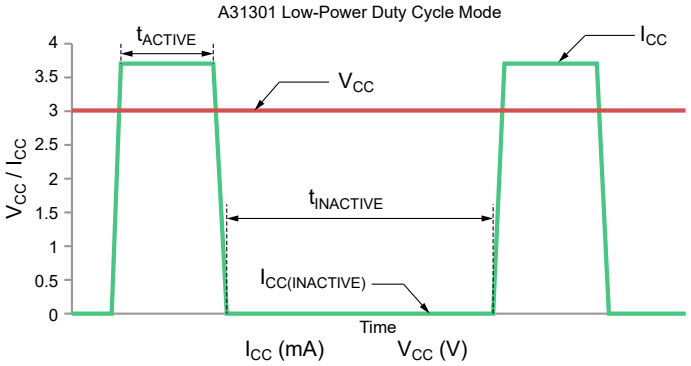



**Figure 6: $I_{CC}$ in Low-Power Duty Cycle Mode**

The inactive time is determined by the value set in the SLEEP_CNT field, address [0x32:0x33], bits [6:4]. The A31331 offers eight discrete time frames, explained in Table 4.

**Table 3: OP_MODE Control**

| Address | Bits | Value | Operating Mode | INT/SAMPLE Pin Function |
|---|---|---|---|---|
| Direct: 0x32:0x33 | 3:1 | 0 | Active Mode | None |
| | | 1 | Active Mode—Interrupt | Interrupt Output |
| | | 2 | Active Mode—Sample | Sample Input |
| | | 3 | Sleep Mode | None |
| | | 4 | Sleep Mode with Sample Wake | Sample/Wake Input |
| | | 5 | Low-Power Duty Cycle Mode (LPDCM) with Interrupt | Interrupt Output |
| | | 6 | Low-Power Duty Cycle Mode (LPDCM) | None |
| | | 7 | Active Mode | None |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 4: SLEEP_CNT Decode; LPDCM Inactive Time ($t_{INACTIVE}$)**

| Address | Bits | Value | $t_{INACTIVE}$ (typ) (ms) |
|---|---|---|---|
| Direct: 0x32:0x33 | 6:4 | 0 | 0.68 |
| | | 1 | 1.36 |
| | | 2 | 6.82 |
| | | 3 | 13.64 |
| | | 4 | 68.18 |
| | | 5 | 136.36 |
| | | 6 | 681.82 |
| | | 7 | 1363.64 |

The active time is determined by a combination of the value in the BW select field and the number of magnetic sensing channels enabled.

## Bandwidth Selection

The A31331 has two parameters to control the device bandwidth and update rate in active mode and low-power mode: CIC_BW_SEL in indirect address 0x14, bits [2:0], controls filtering modes on the A31331 for the X, Y, and Z magnetic channels in active mode; and CIC_BW_SEL_LPM in indrect address 0x14, bits [5:3] controls the filtering modes of the channels in low-power duty cycle mode. This setting impacts the resolution of the sampled magnetic data, device update rate, and overall bandwidth.

A lower value for CIC_BW_SEL/LPM offers increased measurement resolution with a longer measurement duration. A higher value for CIC_BW_SEL/LPM offers faster measurement time at the expense of reduced resolution. This setting is valuable for controlling active time during low-power duty cycle mode or increasing response time. Typical noise versus CIC_BW_SEL/LPM is listed in Table 5.

Update rate (typical) versus CIC_BW_SEL/LPM and active channels is shown in Table 5. The A31331 updates internally at a high bandwidth. However, throughput may be limited by the communication protocol clocking frequency at the application level.

Magnetic sensing channels on the A31331 may be enabled independently with the AFE_CHAN_DIS_X, AFE_CHAN_DIS_Y, and AFE_CHAN_DIS_Z bits in the indirect space, or the equivalent AFE_CHAN_DIS_X_DIR, AFE_CHAN_DIS_Y_DIR, and AFE_CHAN_DIS_Z_DIR in the direct space.

NOTE: When updating the CIC_BW_SEL or CIC_BW_SEL_LPM, the device must be reset for the change to correctly take effect.

**Table 5: Bandwidth Select, Filtering Modes, and Input Referred Noise (600 G Device Only)**

| BW Select Value | Approximate Bandwidth (Hz) | Approximate Update Rate, 1 Channel (µs) | Approximate Update Rate, 2 Channels (µs) | Approximate Update Rate, 3 Channels (µs) | Z-Channel Noise (G) | X-/Y-Channel Noise (G) |
|---|---|---|---|---|---|---|
| 0 | 195.5 | 1024 | 6156 | 9234 | 0.052 | 0.100 |
| 1 | 391 | 512 | 3084 | 4626 | 0.073 | 0.141 |
| 2 | 782 | 256 | 1548 | 2322 | 0.103 | 0.200 |
| 3 | 1564 | 128 | 780 | 1170 | 0.146 | 0.283 |
| 4 | 3128 | 64 | 396 | 594 | 0.207 | 0.400 |
| 5 | 6256 | 32 | 204 | 306 | 0.293 | 0.566 |
| 6 | 12512 | 16 | 108 | 162 | 0.414 | 0.800 |
| 7 | Not Supported | | | | | |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

# INTERFACE INFORMATION

## I²C Interface

I²C is a synchronous, two-wire serial communication protocol that provides a full-duplex interface between two or more devices. The bus specifies two logic signals:

1. Serial clock line (SCL) output by the controller.
2. Serial data line (SDA) output by either the controller or the peripheral.

The A31331 may only operate as a peripheral device. Therefore, it cannot initiate any transactions on the I²C bus.

## Data Transmission and Timing Considerations

I²C communication comprises the following steps:

1. Start Condition: Defined by a negative edge of the SDA line, initiated by the controller, while SCL is high.
2. Address Cycle: 7-bit peripheral address, plus 1 bit to indicate write (0) or read (1), followed by an acknowledge bit.
3. Data Cycles: Reading or writing 8 bits of data, followed by an acknowledge bit. This cycle can be repeated for multiple bytes of data transfer. The first data byte on a write could be the register address. For further information, see the sections that follow.
4. Stop Condition: Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate the start or stop condition, SDA must remain stable while the clock signal is high. SDA may only change states while SCL is low. It is acceptable for a start or stop condition to occur at any time during the data transfer. The A31331 always responds to a read or write request by resetting the data transfer sequence.

The state of the Read/$\overline{\text{Write}}$ bit is set to 0 to indicate a write cycle and is set to 1 to indicate a read cycle.

The controller monitors for an acknowledge bit to confirm the peripheral device (A31331) is responding to the address byte. When the A31331 decodes the 7-bit peripheral address as valid, it responds by pulling SDA low during the ninth clock cycle.

When a data write is requested by the controller, the A31331 pulls SDA low during the clock cycle following the data byte to indicate that data receipt is successful.

After sending either an address byte or a data byte, the controller must release the SDA line before the ninth clock cycle, allowing the handshake process to occur.

## I²C Write Cycle Overview

The write cycle to access registers on the A31331 comprises the following steps:

1. Controller initiates the start condition.
2. Controller sends the 7-bit peripheral address and the write bit (0).
3. Controller waits for acknowledgement (ACK) from A31331.
4. Controller sends the 8-bit register address.
5. Controller waits for ACK from A31331.
6. Controller sends the data from bits [15:8].
7. Controller waits for ACK from A31331.
8. Controller sends the data from bits [7:0].
9. Controller waits for ACK from A31331.
10. Controller initiates the stop condition.

The I²C write sequence is further illustrated in the timing diagram in Figure 7.

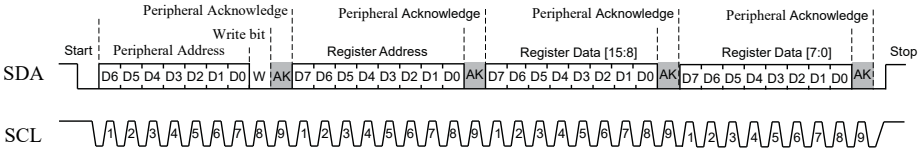



**Figure 7: I²C Write Timing Diagram**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Read Cycle Overview

The read cycle to access registers on A31331 comprises the following steps:

1. Controller initiates the start condition.
2. Controller sends the 7-bit peripheral address and the write bit (0).
3. Controller waits for ACK from A31331.
4. Controller sends 8-bit register address.
5. Controller waits for ACK from A31331.
6. Initiate a start condition; this time it is referred to as a restart condition.
7. Controller sends the 7-bit peripheral address and the read bit (1).
8. Controller waits for ACK from A31331.
9. Controller receives the data of bits [15:8].
10. Controller sends ACK to A31331.
11. Controller receives the data of bits [7:0].
12. Controller sends negative acknowledgement (NACK) to A31331.
13. Controller initiates the stop condition

The I²C read sequence is further illustrated in the timing diagrams in Figure 8.

The timing diagram in Figure 8 shows the entire contents (bits [15:0]) of a single register location being transmitted. Optionally, the I²C Controller may choose to replace the NACK with an ACK instead, which allows the read sequence to continue. This case will result in the transfer of contents (bits [15:8]) from the following register, address + 1. The controller can then continue acknowledging, issue the NACK, or stop after any byte to stop receiving data.

NOTE: Only the initial register address is required for reads, allowing for faster data retrieval. However, this restricts data retrieval to sequential registers when using a single read command. When the controller provides a NACK bit and a stop bit, the A31331 stops sending data. If nonsequential registers are to be read, separate read commands must be sent.

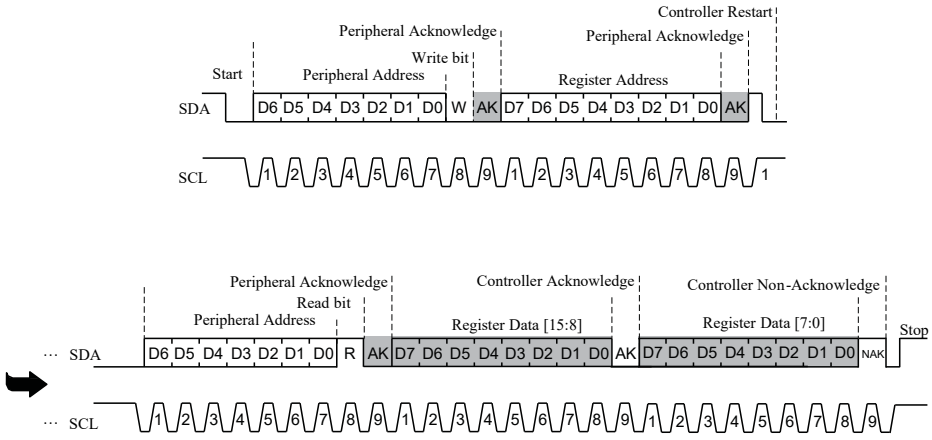



**Figure 8: I²C Read Timing Diagram**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## I²C CRC Byte

To enable the A31331 cyclic redundancy check (CRC) feature, set the I2C_CRC_EN bit, indirect address 0x15, bit [18]. When enabled, the A31331 read transaction returns one extra byte, which corresponds to the CRC calculation of that read. The bytes of the I²C read sequence used for CRC calculation are:

1. 8-bit register address
2. 7-bit peripheral address + read bit (1'b1)
3. 2 data bytes (16 bits, MSB first)

The 8-bit-long code is generated using the CRC8-ATM (0x83) polynomial:

$$p(x) = x^8 + x^2 + x + 1$$

## I²C Readback Modes

The A31331 supports three different readback modes over the I²C interface, including single, continuous, and loopback modes. These modes simplify the process of repeatedly polling the A31331 for magnetic X, Y, Z, and temperature data.

### SINGLE MODE

In single mode, there is a single write or read command to any register. This is the default mode and is best suited for setting fields and reading static registers. If desired, this mode can be used to read data in a typical serial fashion, but fast or full-loop read modes are recommended for high-speed data retrieval. After each single read is complete, the controller must issue a NACK to complete the transaction.

### CONTINUOUS MODE

Instead of issuing a NACK after a read request, the controller can continue to issue an ACK. When this occurs, the A31331 continues to transmit data from the next address, address + 2. This feature allows successive register reads without the need to send a read command for each register.

### LOOPBACK MODE

Loopback mode on the A31331 is described in Table 6. The desired data to be returned serially in the loopback output register, I2C_LOOP_BACK_16B, can be enabled by setting the appropriate bit(s) for I2C_LOOPBACK_CH_SEL, direct address [0x34:0x35], bits [7:0]. In this mode, the desired data are loaded into the same read address sequentially. This allows continuous polling of a single register to obtain all of the necessary data. If a NACK is sent before the loopback sequence is complete, the loop restarts upon the next request.

**Table 6: A31331 Looping Read Modes**

| I2C_LOOPBACK_CH_SEL | Enabled Data in Loop |
|---|---|
| 0 | X_CHANNEL_15B |
| 1 | Y_CHANNEL_15B |
| 2 | Z_CHANNEL_15B |
| 3 | TEMPERATURE_12B |
| 4 | SINE_15B |
| 5 | COSINE_15B |
| 6 | RADIUS_15B |
| 7 | ANGLE_15B |

## I²C Addressing

The different addresses available to the A31331 are outlined in Table 7. In the special case where AD0 and AD1 are both tied to VCC, the device responds to the peripheral address stored in register I2C_SLV_ADDR in indirect-space address 0x15 (bits [16:10]). From the factory, this is set to 111, with the bit following the address indicating a read or write per the I²C specification.

NOTE: Different values for the three most significant bits (MSBs) of the address bits (A6, A5, and A4) are available for factory programming if a conflict with other units occurs in the application design.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 7: I²C Peripheral Address Decoding**

| Voltage on AD1, $V_{A1}$ (× $V_{CC\_IO}$) | Voltage on AD0, $V_{A0}$ (× $V_{CC\_IO}$) | 4-Bit Code from ADR1 and ADR0 Voltages | | | | Peripheral Address Bits | | | | | | | Peripheral Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | E3 | E2 | E1 | E0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 96 |
| | 0.33 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 97 |
| | 0.67 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 98 |
| | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 99 |
| 0.33 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 100 |
| | 0.33 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 101 |
| | 0.67 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 102 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 103 |
| 0.67 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 104 |
| | 0.33 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 105 |
| | 0.67 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 106 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 107 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 108 |
| | 0.33 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 109 |
| | 0.67 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 110 |
| | 1 | 1 | 1 | 1 | 1 | I2C_SLV_ADDR | | | | | | | Programmed to 111 at the factory |

## SPI Protocol

The A31331 provides a full-duplex 4-pin SPI interface for each die. The sensor responds to commands received on the corresponding controller-out peripheral-in (MOSI), serial clock (SCLK), and chip-select ($\overline{CS}$) pins, and outputs data on the controller-in peripheral-out (MISO) pin. The A31331 supports SPI mode 3 (CPOL = 1, and CPHA = 1).

## SPI Interface Timing

The SPI interface operates in pure peripheral mode, with the controller governing the SCLK, MOSI, and $\overline{CS}$ lines. Clock frequencies up to 10 MHz are supported. Timings of the write and read cycles are shown in Figure 4.

## SPI Message Frame Size

An SPI transaction is a minimum of 16 bits in length. An extended 20-bit SPI packet allows 4 bits of CRC to accompany every data packet. The 4-bit CRC is automatically generated and placed on the MISO line during clock pulses 17 through 20. The A31331 contains 16-bit primary-access registers that are byte-addressable to match the SPI frame size. To access the 32-bit EEPROM, an extended access scheme is implemented. This scheme consists of two 16-bit registers that contain the memory contents for a write, two 16-bit registers that contain the memory contents for a read, and registers that contain the memory locations for the write, read, and execution control to begin and monitor the write/read.

## SPI Error Checking

The SPI CRC algorithm is based on the following polynomial, initialized with 0xF:

$$g(x) = x^4 + x + 1$$

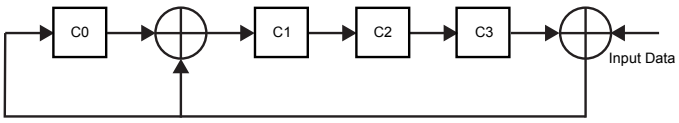



**Figure 9: SPI CRC**

For the A31331 to accept the CRC on the MOSI line, the EEPROM parameter, SPI_CRC_EN, must be set to 1. If the incoming SPI message is greater than 16 bits and SPI_CRC_EN = 0, the message is ignored.

When enabled, the 4-bit CRC is expected. If the CRC is incorrect, the SPI packet is discarded. The MISO packet on the next message is the previous read data.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

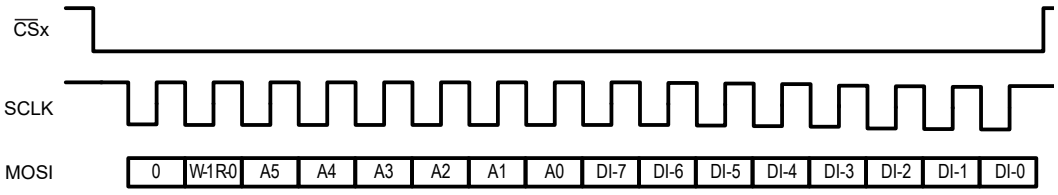



**Figure 10: Sixteen-Bit SPI Message**

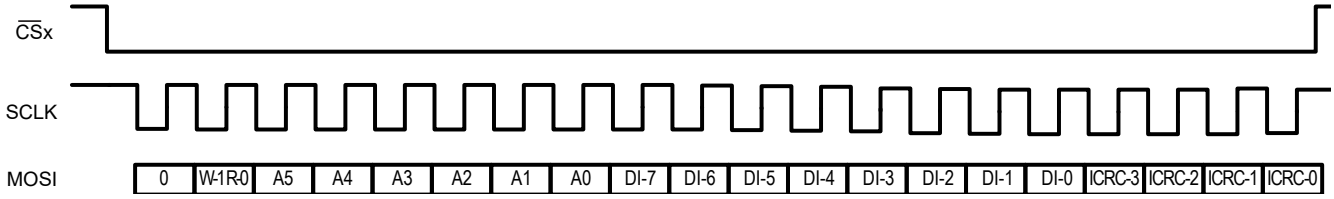



**Figure 11: Twenty-Bit SPI Message**

## Write Cycle Overview

Write cycles consist of 1 synchronization (sync) bit (low), 1 read/write bit (R/W) asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two write commands are required (even and odd byte addresses). MOSI bits are clocked-in on the rising edge of the controller-generated SCLK signal. The complete SPI packet is latched on the rising edge of the controller-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet, including 16 data bits and 4 optional CRC bits. The data bits correspond to the register contents selected during the previous read command. If a previous read command was not issued (for instance, a write command), the MISO line transmits all zeroes as a return.

## Read Cycle Overview

Read cycles have two stages: a read command, selecting a serial register address, followed by another SPI command; it is during this second SPI command that data from the selected register is transmitted from the part to the host. Both commands consist of a 1-bit sync (low), a 1-bit R/W asserted low for a read, 6 address bits identifying the target register, and 8 data bits (these are immaterial because data is not being written), followed by 4 optional CRC bits.

In the first stage, as with the write command, the read command MOSI bits are clocked-in on the rising edge of the controller-generated SCLK signal, and data are latched on the rising edge of the $\overline{CS}$ signal. During the first read stage, the simultaneous MISO signal output is composed of either the contents of the SPI read data from a previous read command cycle, or the contents of the angle register if the previous command was a write.

In the second stage, the read command continues on the next falling edge of the controller-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, read 16 bits at a time. The MISO bits transmit on the falling edges of the SCLK signal, such that the controller can sample them on the SCLK rising edges.

Because an SPI read command can transmit 16 data bits at one time, and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register can be transmitted with one SPI frame.

Examples of both an SPI write and an SPI read request using a 16-bit SPI message frame are shown in Figure 12.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

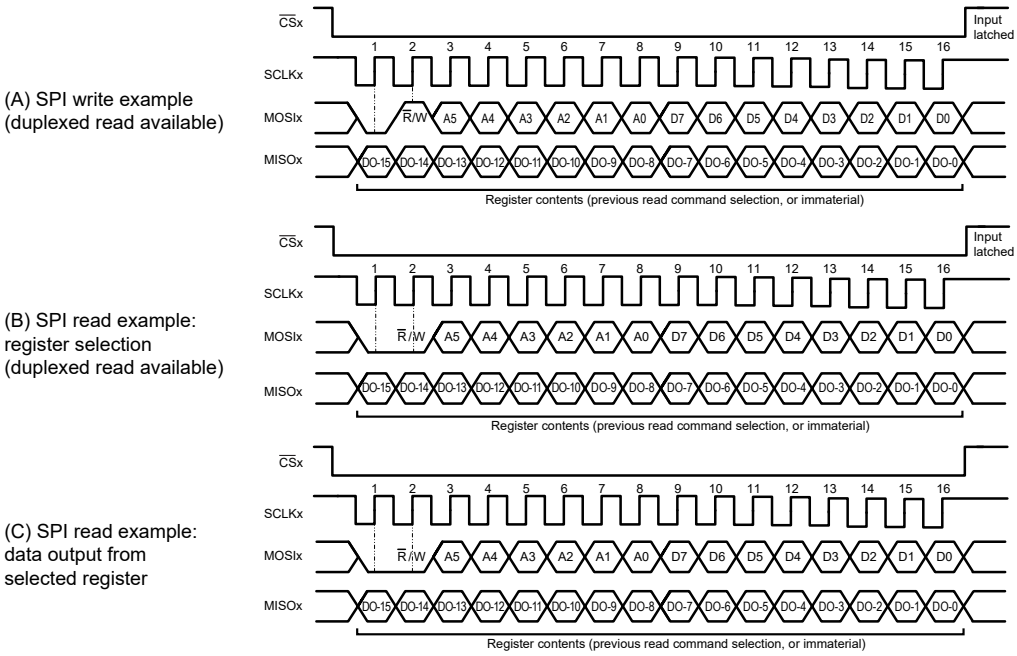



**Figure 12: SPI Read and Write Pulse Sequences**

## EEPROM Margin Checking

The A31331 contains a test mode, known as EEPROM margining, to check the logic levels of the EEPROM bit cells. Due to nonidealities in transistors, current slowly leaks into or out of EEPROM cells and can, over time, cause small changes in the stored voltage level. During programming, variances in voltage levels of the charge pump can result in a variety of stored EEPROM cell voltages. If this value is marginally close to the threshold, the small drift over lifetime can cause this value to surpass the threshold. This results in a corrupted EEPROM value. Because this drift occurs slowly over time, if an issue arises, it might not appear for years. For this reason, it is important to perform margin testing (margining) to verify the internal voltage levels of EEPROM cells after programming and to ensure that issues do not occur in the future.

This test should be run after writing to the EEPROM to ensure the bit cell thresholds are within the specification for reliable EEPROM operation.

To perform the test, set the volatile MARGIN_START bit. Once set, the device enters the test mode where all bit cells within the EEPROM array are checked. The EEPROM margining is selectable to check all logic 1 thresholds (can be disabled by MARGIN_NO_MAX), logic 0 thresholds (can be disabled by MARGIN_NO_MIN), or both thresholds.

**Table 8: Margin Status Return Decoding**

| MARGIN_STATUS | Meaning |
|---|---|
| 0 | Reset condition (result from margin testing not available) |
| 1 | Pass: Failure not detected during margin testing |
| 2 | Fail: Failure detected during margin testing |
| 3 | Running: Margin test is still running |

The EEPROM margin test spans 1 ms (typical). After the EEPROM margin test completes, the status can be read out via the MARGIN_STATUS bit in the volatile space. The best practice is to perform EEPROM margin checking after end-of-line programming.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## MEMORY ACCESS

The A31331 uses a primary and extended memory structure. The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power-cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x20 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. The serial interface primary access registers can be read or written to without the customer access code. The mapping of bits from register addresses in EEPROM to their corresponding register addresses in shadow is shown in the EEPROM tables in the Indirect Extended Space section. The access register is used to unlock the device. The access code must be written to ACCESS_KEY [15:0] one byte at a time. Once unlocked, EEPROM and shadow registers can be written.

Extended access is provided to additional memory space via the primary registers. This access includes the EEPROM, shadow registers, and registers for additional status and diagnostics. All extended registers are 32 bits wide.

### Customer Access Modes

The device memory contains nonvolatile EEPROM and volatile registers that are accessible via the serial interface through SPI or I²C communication mode. The memory address space is divided into three areas: factory, customer, and general access.

Customer access is controlled by an access code shown in Table 9. The access codes contain 32 bits.

To send the access codes shown in Table 9, the user writes to the access register with four consecutive 8-bit writes.

When the customer access code is received, factory registers are addressable but are read-only.

**Table 9: 32-bit Customer Access Code**

| | Byte 1 | Byte 2 | Byte 3 | Byte 4 |
|---|---|---|---|---|
| Customer (Read access to fact) | 43 | 55 | 53 | 54 |

### Read Transaction from EEPROM (or Shadow Memory)

To invoke an extended read access:

1. Load the INDIRECT_RD_ADDR parameter with the target extended address. INDIRECT_RD_ADDR is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Invoke the extended access by writing the primary INDIRECT_RD_STATUS register EXR bit with 1. The INDIRECT_RD_ADDR address is then read, and the data is loaded into the INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB registers.
3. Read the INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB registers to obtain the extended data. Multiple packets are required to obtain all 32 bits.

The RDN bit in the INDIRECT_RD_STATUS register can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the INDIRECT_RD_DATA_MSB or INDIRECT_RD_DATA_LSB register when read access is in progress. If the read access is potentially in progress, the data might change during serial access. Therefore, an attempt to read these registers when read access is in progress can result in inconsistent data. A data change during a serial read via the SPI interface can also produce an SPI CRC error.

For example, to read location 0x15 in the EEPROM:

- Write 0x15 to the lower 8 bits of INDIRECT_RD_ADDR (0x15 to address 0x0B).
- Write 0x80 to the upper 8 bits of INDIRECT_RD_STATUS to set the EXR bit (0x80 to address 0x0C).
- Read INDIRECT_RD_STATUS until bit 0 (RDN) is set (or until sufficient time elapses).
- Read INDIRECT_RD_DATA_MSB (upper 16 bits of read data).
- Read INDIRECT_RD_DATA_LSB (lower 16 bits of read data).



ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Write Transaction to EEPROM (or Shadow Memory)

An extended write access can be invoked as follows:

1. Load the INDIRECT_WR_ADDR parameter with the target extended address.
2. Load the INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB registers with the data to be written to the target. Multiple writes are required to load all 32 bits of data.
3. Invoke the extended access by writing the primary INDIRECT_WR_STATUS register EXW bit with 1.

The INDIRECT_WR_ADDR address is then written with the 32-bit INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB data. The WDN bit in the INDIRECT_WR_STATUS register can be polled to determine when the write completes.

## Shadow Memory Read and Write Transactions

Read and write transactions for shadow memory are nearly identical to those for EEPROM: Instead of addressing to the EEPROM addresses, the shadow extended addresses must be addressed; these are located at an offset of 0x20 higher than the EEPROM.

## Shared Factory and Customer Trim Registers

Register addresses [0x07:0x12] contain memory used to factory-trim the device for the highest sensing accuracy in any application where the input vectors match in amplitude. If the application requires additional end-of-line adjustments to the device trim, these registers can be adjusted by the customer.

NOTE: The customer must ensure the accuracy of the device after end-of-line programming.

## Memory Access in Low-Power Modes

When in sleep mode or low-power duty cycle mode, OP_MODE = 3 through 6, read/write access is limited to critical registers. This helps conserve power. Only the subset of direct-space registers needed to use the part in typical operation is available. Writes are only possible to direct-space addresses [0x32:0x33] that contain device configuration parameters. For reads, direct-space addresses [0x12:0x2B] and [0x32:0x33] are available in the I²C interface, and [0x1C:0x2A] and [0x32:0x33] are available in the SPI interface. For more information about the contents of these registers, see the Memory Map section.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## MEMORY MAP

The A31331 uses a primary and extended memory structure designated as direct (primary) and indirect (extended) space.

### Direct Primary Space

**Table 10: Direct Memory Map**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 | 0x1 | NOP_REGISTER | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x2 to 0x8 | 0x3 to 0x9 | INDIRECT_WRITE_ REGISTERS | Indirect Write Registers | | | | | | | | | | | | | | | |
| 0xA to 0x10 | 0xB to 0x11 | INDIRECT_READ_ REGISTERS | Indirect Read Registers | | | | | | | | | | | | | | | |
| 0x12 to 0x1A | 0x13 to 0x1B | I2C_ONLY_REGISTERS | I2C Only Registers | | | | | | | | | | | | | | | |
| 0x1C to 0x30 | 0x1D to 0x31 | OUTPUT_REGISTERS | Output Registers | | | | | | | | | | | | | | | |
| 0x32 | 0x33 | CONTROL_REGISTER_1 | Control Register 1 | | | | | | | | | | | | | | | |
| 0x34 | 0x35 | I2C_LOOPBACK REGISTER | I2C Loopback Register | | | | | | | | | | | | | | | |
| 0x36 | 0x37 | CONTROL_REGISTER_2 | Control Register 2 | | | | | | | | | | | | | | | |
| 0x38 | 0x39 | CONTROL_REGISTER_3 | Control Register 3 | | | | | | | | | | | | | | | |
| 0x3A | 0x3B | CONTROL_REGISTER_4 | Control Register 4 | | | | | | | | | | | | | | | |
| 0x3C | 0x3D | RESERVED_REGISTER | Reserved Register | | | | | | | | | | | | | | | |
| 0x3E | 0x3F | ACCESS KEY_REGISTER | Access Key Register | | | | | | | | | | | | | | | |

The direct register map is the main access point to the data of the device. During typical operation, the host requests data from the device by reading the direct register. The requested data is output/status data or volatile configuration parameters. Nonvolatile configuration of the device and certain volatile test features are accessible via the indirect write/read registers.

**Table 11: NOP Register**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 | 0x1 | VOLATILE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 12: Indirect Write Registers**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x2 | 0x3 | INDIRECT_WR_ADDRESS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | INDIRECT_WR_ADDR | | | | | | | |
| 0x4 | 0x5 | INDIRECT_WR_DATA_MSB | INDIRECT_WR_DATA_3 | | | | | | | | INDIRECT_WR_DATA_2 | | | | | | | |
| 0x6 | 0x7 | INDIRECT_WR_DATA_LSB | INDIRECT_WR_DATA_1 | | | | | | | | INDIRECT_WR_DATA_0 | | | | | | | |
| 0x8 | 0x9 | INDIRECT_WR_STATUS | EXW | 0 | 0 | 0 | 0 | 0 | 0 | WIP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WDN |

**INDIRECT_WR_ADDR (0x02:0x03 [7:0])**

Address to be used for an extended write.

**INDIRECT_WR_DATA_3 (0x04:0x05 [15:8])**

Most significant 8 bits of data to be written to the extended space (bits [31:24]).

**INDIRECT_WR_DATA_2 (0x04:0x05 [7:0])**

Next 8 bits of data to be written to the extended space (bits [23:16]).

**INDIRECT_WR_DATA_1 (0x06:0x07 [15:8])**

Next 8 bits of data to be written to the extended space (bits [15:8]).

**INDIRECT_WR_DATA_0 (0x06:0x07 [7:0])**

Least-significant 8 bits of data to be written to the extended space (bits [7:0]).

**EXW (0x08:0x09 [15])**

Initiate extended write by writing with 1. Sets WIP. Clears WDN. Always reads back 0.

**WIP (0x08:0x09 [8])**

Extended write is in progress when 1.

**WDN (0x08:0x09 [0])**

Extended write is complete when 1.

**Table 13: Indirect Read Registers**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xA | 0xB | INDIRECT_RD_ADDRESS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | INDIRECT_RD_ADDR | | | | | | | |
| 0xC | 0xD | INDIRECT_RD_STATUS | EXR | 0 | 0 | 0 | 0 | 0 | 0 | RIP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RDN |
| 0xE | 0xF | INDIRECT_RD_DATA_MSB | INDIRECT_RD_DATA_3 | | | | | | | | INDIRECT_RD_DATA_2 | | | | | | | |
| 0x10 | 0x11 | INDIRECT_RD_DATA_LSB | INDIRECT_RD_DATA_1 | | | | | | | | INDIRECT_RD_DATA_0 | | | | | | | |

**INDIRECT_RD_ADDR (0x0A:0x0B [7:0])**

Address to be used for an extended read.

**EXR (0x0C:0x0D [15])**

Initiate extended read by writing with 1. Sets RIP. Clears RDN. Always reads back 0.

**RIP (0x0C:0x0D [8])**

Extended read is in progress when 1.

**RDN (0x08:0x09 [0])**

Extended read is complete when 1.

**INDIRECT_RD_DATA_3 (0x0E:0x0F [15:8])**

Most significant 8 bits of data returned from the extended space (bits [31:24]).

**INDIRECT_RD_DATA_2 (0x0E:0x0F [7:0])**

Next 8 bits of data returned from the extended space (bits [23:16]).

**INDIRECT_RD_DATA_1 (0x10:0x11 [15:8])**

Next 8 bits of data returned from the extended space (bits [15:8]).

**INDIRECT_RD_DATA_0 (0x10:0x11 [7:0])**

Least-significant 8 bits of data returned from the extended space (bits [7:0]).



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 14: I²C Only Registers**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x12 | 0x13 | I2C_LOOP_BACK | I2C_LOOP_BACK_16B | | | | | | | | | | | | | | | |
| 0x14 | 0x15 | I2C_X_Y_8B | Y_CHANNEL_8B | | | | | | | | X_CHANNEL_8B | | | | | | | |
| 0x16 | 0x17 | I2C_T_Z_8B | TEMPERATURE_8B | | | | | | | | Z_CHANNEL_8B | | | | | | | |
| 0x18 | 0x19 | I2C_ANGLE_RADIUSSQ_8B | ANGLE_8B | | | | | | | | RADIUS_SQ_8B | | | | | | | |
| 0x1A | 0x1B | I2C_SIN_COS_8B | SIN_8B | | | | | | | | COS_8B | | | | | | | |
| 0x34 | 0x35 | I2C_LOOPB_CONF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | I2C_LOOPBACK_CH_SEL | | | | | | | |

NOTE: The registers listed here are exclusively for use in I²C device modes. In SPI mode, these registers are to be considered "do not read," and any results read from these registers is considered invalid. The digital ports (I²C/SPI) differ in how they interface to the internal registers to accommodate different data speeds and other configurations. For SPI modes, see the SPI Protocol section.

### I2C_LOOP_BACK_16B (0x12:0x13 [15:0])

This register provides the 16-bit result of the last channel read per the loopback configuration register. See the I2C_LOOPBACK_CH_SEL (0X34:0X35 [7:0]) description.

### Y_CHANNEL_8B (0x14:0x15 [15:8])

This register provides a fast, partial, result of the Y-axis channel data. The upper 8 bits of the 15-bit register (Y_CHANNEL_15B) provides the user with the values of up to ±127 counts for the channel data.

### X_CHANNEL_8B (0x14:0x15 [7:0])

This register provides a fast, partial result of the X-axis channel data. The upper 8 bits of the 15-bit register (X_CHANNEL_15B) provides the user with the values of up to ±127 counts for the channel data.

### TEMPERATURE_8B (0x16:0x17 [15:8])

This register provides a fast, partial result of the temperature sensor output data. The upper 8 bits of the 12-bit register (TEMPERATURE_12B) are provided for the user.

### Z_CHANNEL_8B (0x16:0x17 [7:0])

This register provides a fast, partial result of the Z-axis channel data. The upper 8 bits of the 15-bit register (Z_CHANNEL_15B) provides the user with the values of up to ±127 counts for the channel data.

### ANGLE_8B (0x18:0x19 [15:8])

This register provides a fast, partial result of the angle output register. The upper 8-bits of unsigned data are stored here from the 15-bit unsigned register (ANGLE_15B). The angle register provides an output of 0 to 255 counts to represent either true angle (1.41176 degrees per LSB) or linear position (0.39215% per LSB).

### RADIUS_SQ_8B (0x18:0x19 [7:0])

This register provides a fast, partial result of the magnitude output register. The upper 8 bits of unsigned data are stored here from the 15-bit unsigned register (RADIUS_15B). The radius-squared register provides a magnitude of sensed field, granting the user the capability of producing angle-vectors numerically without additional computational requirements for the host microcontroller.

### SIN_8B (0x1A:0x1B [15:8])

This register provides a fast, signed output for the sine channel input to the angle calculation. The upper 8 bits of unsigned data is stored here from the 15-bit signed register (SINE_15B).

### COS_8B (0x1A:0x1B [7:0])

This register provides a fast, signed output for the cosine channel input to the angle calculation. The upper 8 bits of unsigned data is stored here from the 15-bit signed register (COSINE_15B).

### I2C_LOOPBACK_CH_SEL (0x34:0x35 [7:0])

This register serves to configure the power-saving options of the A31331. Here, the operational mode (active, low-power duty-cycling, sleep) is configured, and any subsequent options pertaining to the configured mode are set.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 15: Output Registers**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x1C | 0x1D | TEMPERATURE | 0 | 0 | 0 | 0 | TEMPERATURE_12B | | | | | | | | | | | |
| 0x1E | 0x1F | X_CHANNEL | 0 | X_CHANNEL_15B | | | | | | | | | | | | | | |
| 0x20 | 0x21 | Y_CHANNEL | 0 | Y_CHANNEL_15B | | | | | | | | | | | | | | |
| 0x22 | 0x23 | Z_CHANNEL | 0 | Z_CHANNEL_15B | | | | | | | | | | | | | | |
| 0x24 | 0x25 | ANGLE | 0 | ANGLE_15B | | | | | | | | | | | | | | |
| 0x26 | 0x27 | RADIUS | 0 | RADIUS_15B | | | | | | | | | | | | | | |
| 0x28 | 0x29 | SINE | 0 | SINE_15B | | | | | | | | | | | | | | |
| 0x2A | 0x2B | COSINE | 0 | COSINE_15B | | | | | | | | | | | | | | |
| 0x2C | 0x2D | X_RAW_FILT_OUT | 0 | X_RAW_FILT_OUT_15B | | | | | | | | | | | | | | |
| 0x2E | 0x2F | Y_RAW_FILT_OUT | 0 | Y_RAW_FILT_OUT_15B | | | | | | | | | | | | | | |
| 0x30 | 0x31 | Z_RAW_FILT_OUT | 0 | Z_RAW_FILT_OUT_15B | | | | | | | | | | | | | | |

**TEMPERATURE_12B (0x1C:0x1D [11:0])**

This register holds the 12-bit signed temperature sensor output.

**X_CHANNEL_15B (0x1E:0x1F [14:0])**

This register holds the 15-bit signed output of the X-axis sensor output.

**Y_CHANNEL_15B (0x20:0x21 [14:0])**

This register holds the 15-bit signed output of the Y-axis sensor output.

**Z_CHANNEL_15B (0x22:0x23 [14:0])**

This register holds the 15-bit signed output of the Z-axis sensor output.

**ANGLE_15B (0x24:0x25 [14:0])**

This register holds the unsigned output of the calculated angle. When used as an angle, the register output is 0.0109863°/LSB. When used as a linear position output, each bit holds a value of 0.0030518%/LSB.

**RADIUS_15B (0x26:0x27 [14:0])**

This register provides a magnitude (squared) of the sensed field, granting the user the capability to produce angle vectors numerically without additional computational requirements for the host microcontroller.

**SINE_15B (0x28:0x29 [14:0])**

This register provides a signed output for the sine channel input to the angle calculation set by CORDIC_SEL.

**COSINE_15B (0x2A:0x2B [14:0])**

This register provides a signed output for the cosine channel input to the angle calculation set by CORDIC_SEL.

**X_RAW_FILT_OUT_15B (0x2C:0x2D [14:0])**

This register provides the raw output of the X-channel before any trim is applied. This can be useful to debug issues with expected output in the X_CHANNEL_15B output.

**Y_RAW_FILT_OUT_15B (0x2E:0x2F [14:0])**

This register provides the raw output of the Y-channel before any trim is applied. This can be useful to debug issues with expected output in the Y_CHANNEL_15B output.

**Z_RAW_FILT_OUT_15B (0x30:0x31 [14:0])**

This register provides the raw output of the Z-channel before any trim is applied. This can be useful to debug issues with expected output in the Z_CHANNEL_15B output.



ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 16: Control Registers**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x32 | 0x33 | OP_MODE_CONF | 0 | 0 | 0 | START_SAMPLE | INTERRUPT_FLAG | STATUS_READY | 0 | 0 | 0 | SLEEP_CNT | | | OP_MODE | | | 0 |
| 0x36 | 0x37 | INT_THR_CONF_DIR | 0 | 0 | 0 | 0 | INTERRUPT_THR_MSB_DIR | | | | INTERRUPT_THR_LSB_DIR | | | | | | | |
| 0x38 | 0x39 | INT_XYZ_CONF_DIR | 0 | 0 | AFE_CHAN_DIS_Z_DIR | AFE_CHAN_DIS_Y_DIR | AFE_CHAN_DIS_X_DIR | POL_F_Z_DIR | POL_F_Y_DIR | POL_F_X_DIR | 0 | INTERRUPT_SEL_DIR | | | | INTERRUPT_SIGN_DIR | INTERRUPT_FLAG_LATCH_DIR | SAMPLE_INT_POLARITY_DIR |
| 0x3A | 0x3B | CIC_CORDIC_CONF_DIR | 0 | 0 | 0 | 0 | 0 | CIC_BW_SEL_LPM_DIR | | | 0 | CIC_BW_SEL_DIR | | | CORDIC_POL_DIR | CORDIC_SEL_DIR | | |

**START_SAMPLE (0x32:0x33 [12])**

If the STATUS_READY parameter is cleared, the START_SAMPLE parameter triggers the start of an internal conversion. The device is in standby mode until this parameter is set or until the INT/SAMPLE pin is pulled to the active state.

**INTERRUPT_FLAG (0x32:0x33 [11])**

This is a latched bit that asserts to 1 when an interrupt occurs. The interrupt functionality is set by INTERRUPT_SEL_DIR in the direct space or INT_SEL in the indirect space. This bit must be set to 0 by a write from the host.

**STATUS_READY (0x32:0x33 [10])**

This is a latched bit that indicates a new sample is ready after the START_SAMPLE bit is set to start a new conversion. This bit must be set to 0 by a write from the host.

**SLEEP_CNT (0x32:0x33 [6:4])**

The SLEEP_CNT parameter controls the inactive time of the low-power duty cycle mode. For decode information, see the Operation Modes section.

**OP_MODE (0x32:0x33 [3:1])**

OP_MODE sets the operation configuration of the A31331 with respect to power use. The different options are described in the Operation Modes section.

**INTERRUPT_THR_MSB_DIR (0x36:0x37 [11:8])**

This parameter sets the MSBs of the programmable threshold for the interrupt functionality. For more information, see the Interrupt Mode description in the Special Function Pin INT/SAMPLE section.

**INTERRUPT_THR_LSB_DIR (0x36:0x37 [7:0])**

This parameter sets the LSBs of the programmable threshold for the interrupt functionality. For more information, see the Interrupt Mode description in the Special Function Pin INT/SAMPLE section.

**AFE_CHAN_DIS_Z_DIR (0x38:0x39 [13])**

This Z-channel disable parameter is a direct-space copy of the AFE_CHAN_DIS_Z bit from indirect space. If the Z-channel is not used, this feature can be used to shut off the Z-channel to reduce power and processing time.

**AFE_CHAN_DIS_Y_DIR (0x38:0x39 [12])**

This Y-channel disable parameter is a direct-space copy of the AFE_CHAN_DIS_Y bit from indirect space. If the Y-channel is not used, this feature can be used to shut off the Y-channel to reduce power and processing time.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**AFE_CHAN_DIS_X_DIR (0x38:0x39 [11])**

This X-channel disable parameter is a direct-space copy of the AFE_CHAN_DIS_X bit from indirect space. If the X-channel is not used, this feature can be used to shut off the X channel to reduce power and processing time.

**POL_F_Z_DIR (0x38:0x39 [10])**

This is a direct-space copy of the POL_F_Z bit from indirect space. This feature flips the polarity of the Z-channel output.

**POL_F_Y_DIR (0x38:0x39 [9])**

This is a direct-space copy of the POL_F_Y bit from indirect space. This feature flips the polarity of the Y-channel output.

**POL_F_X_DIR (0x38:0x39 [8])**

This is a direct-space copy of the POL_F_X bit from indirect space. This feature flips the polarity of the X-channel output.

**INTERRUPT_SEL_DIR (0x38:0x39 [6:3])**

This is a direct-space copy of the INT_SEL parameter from indirect space. This selects the signal to compare to the programmed threshold in INTERRUPT_THR_MSB/LSB_DIR, as shown in the table in the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**INTERRUPT_SIGN_DIR (0x38:0x39 [2])**

This is a direct-space copy of the INT_SIGN parameter from indirect space. This selects the sign of the comparison to the threshold to set the interrupt from signal less than the programmed threshold (0, default) to signal greater than the programmed threshold (1). For more information, see the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**INTERRUPT_FLAG_LATCH_DIR (0x38:0x39 [1])**

This is a direct-space copy of the INT_FLAG_LATCH parameter from indirect space. This sets the latch assertion behavior of the INT/SAMPLE pin when the condition is removed. In the default, 0, case, the INT/SAMPLE pin output does not remain asserted. For more information, see the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**SAMPLE_INT_POLARITY_DIR (0x38:0x39 [0])**

This direct-space copy of SMPL_INT_POL controls the polarity of the special function bin: 0 (default) = active low; 1 = active high.

**CORDIC_BW_SEL_LPM_DIR (0x3A:0x3B [10:8])**

This direct-space copy of the CIC_BW_SEL_LPM parameter in indirect space is used to set the BW in low-power mode (OP_MODE = 3,4). The amount of time the part is awake making conversions for each active channel before returning to sleep is set by this parameter. For more information, see the Bandwidth Selection and Low-Power Duty Cycle Mode (LPDCM) sections.

**CORDIC_BW_SEL_DIR (0x3A:0x3B [6:4])**

This is a direct-space copy of the CIC_BW_SEL parameter in indirect space. This sets the BW in active mode (OP_MODE = 0,1, or 2). For more information, see the Bandwidth Selection section.

**CORDIC_POL_DIR (0x3A:0x3B [3])**

This is a direct-space copy of the CORIC_POL parameter in indirect space. This sets the output to be increasing in code or decreasing in code for an increasing magnetic angle input. For more information, see the Magnetic Sensor(s) Output section.

**CORDIC_SEL_DIR (0x3A:0x3B [2:0])**

This is a direct-space copy of the CORIC_SEL parameter in indirect space. This sets the two channels used for the ATAN angle calculation. For more information, see the Magnetic Sensor(s) Output section.

**Table 17: Reserved Register**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x3C | 0x3D | RESERVED | RESERVED | | | | | | | | | | | | | | | |

**RESERVED (0x3C:0x3D [15:0])**

This register is reserved for factory use. To maintain device functionality, leave this register as zero.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 18: Access Register**

| MSByte Address | LSByte Address | Register Name | MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x3E | 0x3F | ACCESS | ACCESS_KEY | | | | | | | | | | | | | | | |

**ACCESS_KEY (0x3E:0x3F [15:0])**

Location for sending the access code to the device. For instructions, see the Memory Access section.

## Indirect Extended Space

**ECC_*** parameters contain ECC error flags in the event of a single- or multi-bit error being detected in a row.

**UNUSED_*** parameters are empty space in the memory that have no function.

**Table 19: EEPROM/Shadow Memory: ID Parameters**

| EEPROM Address | Shadow Address | bit | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 31 to 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 | N/A | ECC_0 | FACTORY_ID_0 | | | | Y_DIE_LOC | | | | | | | | X_DIE_LOC | | | | | | | | EEPROM_REV | | | | | |
| 0x1 | N/A | ECC_1 | FACTORY_ID_1 | | | | FACTORY_LOT | | | | | | | | | | | | | | | | FACTORY_WAFER | | | | | |

**FACTORY_ID_0 (EEPROM: 0x00, Shadow: None [25:22])**

Factory-use identification parameter.

**Y_DIE_LOC (EEPROM: 0x00, Shadow: None [21:14])**

Die location on wafer in Y-dimension.

**X_DIE_LOC (EEPROM: 0x00, Shadow: None [13:6])**

Die location on wafer in X-dimension.

**EEPROM_REV (EEPROM: 0x00, Shadow: None [5:0])**

EEPROM revision.

**FACTORY_ID_1 (EEPROM: 0x01, Shadow: None [25:22])**

Factory-use identification parameter.

**FACTORY_LOT (EEPROM: 0x01, Shadow: None [21:6])**

Factory lot number.

**FACTORY_WAFER (EEPROM: 0x01, Shadow: None [5:0])**

Factory wafer number in lot.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 20: EEPROM/Shadow Memory: Trim Parameters**

| EEPROM Address | Shadow Address | bit | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 31 to 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x7 | 0x27 | ECC_7 | UNUSED_07 | | | | | | | | | | POL_F_X | AFE_CHAN_DIS_X | SENS_F_X | | | | | | | | | | | | | |
| 0x8 | 0x28 | ECC_8 | UNUSED_08 | | | | | | | | | | POL_F_Y | AFE_CHAN_DIS_Y | SENS_F_Y | | | | | | | | | | | | | |
| 0x9 | 0x29 | ECC_9 | UNUSED_09 | | | | | | | | | | POL_F_Z | AFE_CHAN_DIS_Z | SENS_F_Z | | | | | | | | | | | | | |
| 0xD | 0x2D | ECC_D | UNUSED_0D | | | | | | SENSTC_CLD_F_X | | | | | | OFFSTC_CLD_F_X | | | | | | | | | | | | | |
| 0xE | 0x2E | ECC_E | UNUSED_0E | | | | | | SENSTC_CLD_F_Y | | | | | | OFFSTC_CLD_F_Y | | | | | | | | | | | | | |
| 0xF | 0x2F | ECC_F | UNUSED_0F | | | | | | SENSTC_CLD_F_Z | | | | | | OFFSTC_CLD_F_Z | | | | | | | | | | | | | |
| 0x10 | 0x30 | ECC_10 | UNUSED_10 | | | | | | SENSTC_HOT_F_X | | | | | | OFFSTC_HOT_F_X | | | | | | | | | | | | | |
| 0x11 | 0x31 | ECC_11 | UNUSED_11 | | | | | | SENSTC_HOT_F_Y | | | | | | OFFSTC_HOT_F_Y | | | | | | | | | | | | | |
| 0x12 | 0x32 | ECC_12 | UNUSED_12 | | | | | | SENSTC_HOT_F_Z | | | | | | OFFSTC_HOT_F_Z | | | | | | | | | | | | | |

**POL_F_X (EEPROM: 0x07, Shadow: 0x27 [15])**

X-channel polarity bit.

**AFE_CHAN_DIS_X (EEPROM: 0x07, Shadow: 0x27 [14])**

X-channel disable. If the X-channel is not used, this feature can be leveraged to shut off the X-channel to reduce power and processing time.

**SENS_F_X (EEPROM: 0x07, Shadow: 0x27 [13:0])**

X-channel sensitivity adjustment. This parameter is used to align the channels at the factory trim. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: 0× to 8×.
Step Size: $2^{-11}$.

**POL_F_Y (EEPROM: 0x08, Shadow: 0x28 [15])**

Y-channel polarity bit.

**AFE_CHAN_DIS_Y (EEPROM: 0x08, Shadow: 0x28 [14])**

Y-channel disable. If the Y-channel is not used, this feature can be leveraged to shut off the Y-channel to reduce power and processing time.

**SENS_F_Y (EEPROM: 0x08, Shadow: 0x28 [13:0])**

Y-channel sensitivity adjustment. This parameter is used to align the channels at the factory trim. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: 0× to 8×.
Step Size: $2^{-11}$.

**POL_F_Z (EEPROM: 0x09, Shadow: 0x29 [15])**

Z-channel polarity bit.

**AFE_CHAN_DIS_Z (EEPROM: 0x09, Shadow: 0x29 [14])**

Z-channel disable. If the Z-channel is not used, this feature can be leveraged to shut off the Z-channel to reduce power and processing time.

**SENS_F_Z (EEPROM: 0x09, Shadow: 0x29 [13:0])**

Z-channel sensitivity adjustment. This parameter is used to align the channels at the factory trim. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.
Range: 0× to 8×.
Step Size: $2^{-11}$.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**SENSTC_CLD_F_X (EEPROM: 0x0D, Shadow: 0x2D [22:12])**

X-channel sensitivity adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.78%/°C.
Step Size: –7.63e-4%/°C.

**OFFSETC_CLD_F_X (EEPROM: 0x0D, Shadow: 0x2D [11:0])**

X-channel offset adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±64 $LSB_{15}$/°C.
Step Size: –0.0313 $LSB_{15}$%/°C.

**SENSTC_CLD_F_Y (EEPROM: 0x0E, Shadow: 0x2E [22:12])**

Y-channel sensitivity adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.78%/°C.
Step Size: –7.63e-4%/°C.

**OFFSETC_CLD_F_Y (EEPROM: 0x0E, Shadow: 0x2E [11:0])**

Y-channel offset adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±64 $LSB_{15}$/°C.
Step Size: –0.0313 $LSB_{15}$%/°C.

**SENSTC_CLD_F_Z (EEPROM: 0x0F, Shadow: 0x2F [22:12])**

Z-channel sensitivity adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.78%/°C.
Step Size: –7.63e-4%/°C.

**OFFSETC_CLD_F_Z (EEPROM: 0x0F, Shadow: 0x2F [11:0])**

Z-channel offset adjustment for –40°C ≤ $T_A$ < 25°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±64 $LSB_{15}$/°C.
Step Size: –0.0313 $LSB_{15}$%/°C.

**SENSTC_HOT_F_X (EEPROM: 0x10, Shadow: 0x30 [22:12])**

X-channel sensitivity adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.39%/°C.
Step Size: 3.81e-4%/°C.

**OFFSETC_HOT_F_X (EEPROM: 0x10, Shadow: 0x30 [11:0])**

X-channel offset adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±32 $LSB_{15}$/°C.
Step Size: 0.0156 $LSB_{15}$%/°C.

**SENSTC_HOT_F_Y (EEPROM: 0x11, Shadow: 0x31 [22:12])**

Y-channel sensitivity adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.39%/°C
Step Size: 3.81e-4%/°C

**OFFSETC_HOT_F_Y (EEPROM: 0x11, Shadow: 0x31 [11:0])**

Y-channel offset adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±32 $LSB_{15}$/°C
Step Size: 0.0156 $LSB_{15}$%/°C



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**SENSTC_HOT_F_Z (EEPROM: 0x12, Shadow: 0x32 [22:12])**

Z-channel sensitivity adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to align the channels at the factory trim to a target compensation. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±0.39%/°C.
Step Size: 3.81e-4%/°C.

**OFFSETC_HOT_F_Z (EEPROM: 0x12, Shadow: 0x32 [11:0])**

Z-channel offset adjustment for 25°C < $T_A$ ≤ 85°C temperature segment. This parameter is used to correct the channel offset at the factory trim in the cold temperature segment. When installed in application, it is available for corrections. If this parameter is adjusted in application, factory accuracy is not ensured.

Range: ±32 $LSB_{15}$/°C.
Step Size: 0.0156 $LSB_{15}$%/°C.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 21: EEPROM/Shadow Memory: Device Configuration Parameters**

| EEPROM Address | Shadow Address | bit | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 31 to 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x13 | 0x33 | ECC_13 | UNUSED_13 | | | SMPL_INT_POL | INT_FLAG_LATCH | INT_SIGN | INT_SEL | | | | INT_THR | | | | | | | | | | | | CORDIC_POL | CORDIC_SEL | | |
| 0x14 | 0x34 | ECC_14 | UNUSED_14 | | | | | | | | | | | | | | | | | | | | | | CIC_BW_SEL_LPM | CIC_BW_SEL | | |
| 0x15 | 0x35 | ECC_15 | UNUSED_15 | | | | INT_EDGE_RATE | SPI_EDGE_RATE | SPI_CRC_EN | I2C_CRC_EN | I2C_SLV_ADDR_IGNORE | I2C_SLV_ADDR | | | | | | | I2C_THRESH_SEL | I2C_DIS_SLV_ADDR | SPARE_15 | | | | | DATA_LATCH | INTERFACE_SELECT | |

**SMPL_INT_POL (EEPROM: 0x13, Shadow: 0x33 [22])**

This parameter controls the polarity of the special function bin: 0 (default) = active low; 1 = active high.

**INT_FLAG_LATCH (EEPROM: 0x13, Shadow: 0x33 [21])**

This parameter sets the latch assertion behavior of the INT/SAMPLE pin when the condition is removed. In the default, 0, case, the INT/SAMPLE pin output does not remain asserted. For more information, see the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**INT_SIGN (EEPROM: 0x13, Shadow: 0x33 [20])**

This parameter selects the sign of the comparison to the threshold to set the interrupt from signal less than the programmed threshold (0, default) to signal greater than the programmed threshold (1). For more information, see the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**INT_SEL (EEPROM: 0x13, Shadow: 0x33 [19:16])**

This parameter selects the signal to compare to the threshold programmed in INTERRUPT_THR_MSB/LSB_DIR, as shown in the table in the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**INT_THR (EEPROM: 0x13, Shadow: 0x33 [15:4])**

This parameter sets the threshold value for the interrupt comparison that is loaded into INTERRUPT_THR_MSB/LSB_DIR upon a reset. For more information, see the Interrupt Mode topic in the Special Function Pin INT/SAMPLE section.

**CORDIC_POL (EEPROM: 0x13, Shadow: 0x33 [3])**

This parameter sets the output to be increasing in code or decreasing in code for an increasing magnetic angle input. For more information, see the Magnetic Sensor(s) Output section.

**CORDIC_SEL (EEPROM: 0x13, Shadow: 0x33 [2:0])**

This parameter sets the two channels used for the ATAN angle calculation. For more information, see the Magnetic Sensor(s) Output section.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**CIC_BW_SEL_LPM (EEPROM: 0x14, Shadow: 0x34 [5:3])**

This parameter sets the BW in low-power mode (OP_MODE = 3,4). This parameter sets the amount of time the part is awake making conversions for each active channel before returning to sleep. For more information, see the Bandwidth Selection and Low-Power Duty Cycle Mode (LPDCM) sections.

**CIC_BW_SEL (EEPROM: 0x14, Shadow: 0x34 [2:0])**

Sets the BW in active mode (OP_MODE = 0, 1, or 2). For more information, see the Bandwidth Selection section.

**INT_EDGE_RATE (EEPROM: 0x15, Shadow: 0x35 [21])**

Interrupt output pin edge rate. For a faster edge and higher-speed communications, set to 0; for a slower edge for power savings, set to 1.

**SPI_EDGE_RATE (EEPROM: 0x15, Shadow: 0x35 [20])**

SPI output edge filtering. For a faster edge and higher-speed communications, set to 0; for a slower edge for power savings, set to 1.

**SPI_CRC_EN (EEPROM: 0x15, Shadow: 0x35 [19])**

This parameter enables the CRC on the SPI message. When set, the SPI packet is 20 bits: 16 bits of data and 4 bits of CRC. For more information, see the SPI Error Checking section.

**I2C_CRC_EN (EEPROM: 0x15, Shadow: 0x35 [18])**

This parameter enables the CRC on the I²C message frame. When set, the 8-bit CRC is added to the read transaction. For more information, see the I²C CRC Byte section.

**I2C_SLV_ADDR_IGNORE (EEPROM: 0x15, Shadow: 0x35 [17])**

When this parameter is set, the device responds to any I²C command, and it ignores the address.

**I2C_SLV_ADDR (EEPROM: 0x15, Shadow: 0x35 [16:10])**

This parameter is used to set the peripheral address for I²C communications when either the external pins are set high or the I2C_DIS_SLV_ADDR is set to one. For more information, see the I²C CRC Byte section.

**I2C_THRESH_SEL (EEPROM: 0x15, Shadow: 0x35 [9])**

This parameter sets the input thresholds for the I²C communication to either 3.0 V compatible (0, default) or 1.8 V compatible (1).

**I2C_DIS_SLV_ADDR (EEPROM: 0x15, Shadow: 0x35 [8])**

This parameter disables the external I²C address pins and latches the current address. The address pins are constantly scanned after power on to check for a change in address. If this bit is set, the last detected address becomes latched. If this is set at power on, the address is set to 96.

**SPARE_15 (EEPROM: 0x15, Shadow: 0x35 [7:2])**

Unused space in the EEPROM.

**DATA_LATCH (EEPROM: 0x15, Shadow: 0x35 [1])**

This parameter allows the latch feature of the output registers to be disabled. When set to zero, the registers continuously update as soon as a new sample is ready for each independent register. When set to 1, the output registers latch from the same point in time, and the host can read each register without the need for a register update upon each register read. To initiate a new latch of the data when DATA_LATCH = 1, the STATUS_READY bit must be cleared.

**INTERFACE_SELECT (EEPROM: 0x15, Shadow: 0x35 [0])**

Sets the active interface to I²C when 0, and to SPI when 1.



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

**Table 22: Indirect Volatile Parameters**

| Address | bit | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x44 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EE_LOOP | EE_TEST_ADDR | | | | | EE_USE_TEST_ADDR | MARGIN_MIN_MAX_FAIL | MARGIN_STATUS | | MARGIN_NO_MIN | MARGIN_NO_MAX | MARGIN_START |
| 0x47 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LBIST_PASS1_FAIL0 | BIST_DONE | BIST_START |
| 0x48 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ACCESS BITS | | | | | | | | | | | |

**EE_LOOP (0x44 [12])**

This parameter causes margin or pattern testing to loop until an error is found.

**EE_TEST_ADDR (0x44[11:7])**

If EE_USE_TEST_ADDR is set, the start of margining or pattern testing occurs at the address programmed in EE_TEST_ADDR. If the test fails, this parameter contains the failing address.

**EE_USE_TEST_ADDR (0x44 [6])**

This parameter sets the starting address for margining to EE_TEST_ADDR when set to 1. If EE_LOOP is set, this bit is ignored, and the testing always starts at 0x00.

**MARGIN_MIN_MAX_FAIL (0x44 [5])**

If margining fails, this bit indicates if the minimum or maximum reference failed. If MARGIN_STATUS = 2 and MARGIN_MIN_MAX = 0, the minimum threshold failed. If MARGIN_STATUS = 2 and MARGIN_MIN_MAX = 1, the maximum threshold failed.

**MARGIN_STATUS (0x44 [4:3])**

This parameter indicates the status of the margining testing. For more information, see the EEPROM Margin Checking section.

**MARGIN_NO_MIN (0x44 [2])**

This parameter disables the check of the minimum threshold when running margining. For typical use, this is not recommended.

**MARGIN_NO_MAX (0x44 [1])**

This parameter disables the check of the maximum threshold when running margining. For typical use, this is not recommended.

**MARGIN_START (0x44 [0])**

This parameter starts the margining test. For more information, see the EEPROM Margin Checking section.

**LBIST_PASS1_FAIL0 (0x44 [2])**

This bit contains the result of the logic built-in self-test (LBIST) testing. If 1, the testing passed; if 0, the testing failed or was not run.

**BIST_DONE (0x44 [1])**

This bit is set to 1 when LBIST is complete.

**BIST_START (0x44 [0])**

This bit is used to start the internal LBIST testing.

**ACCESS_BITS (0x48 [11:0])**

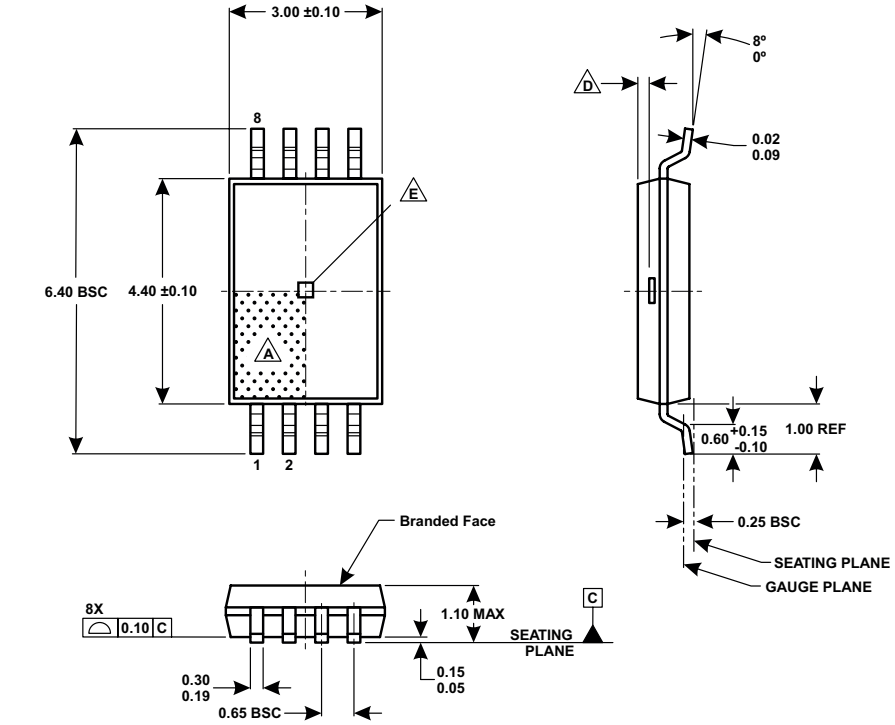
This bit contains flags that indicate the internal access modes. It is for factory use only.

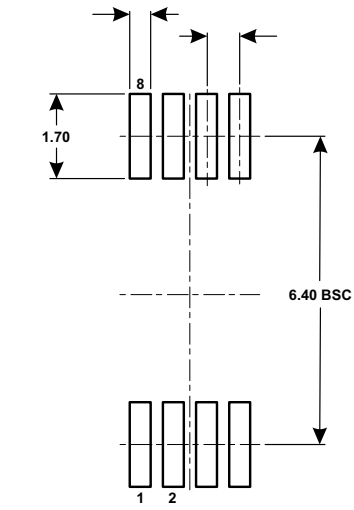


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

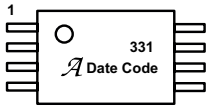
## PACKAGE OUTLINE DRAWING
### For Reference Only – Not for Tooling Use

**(Reference MO-153AA)**
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown




B PCB Layout Reference View




C Standard Branding Reference View

Line 1 = 3 characters
Line 2 = 6 characters

Line 1: Pin 1 dot, last 3 digits of Part Number
Line 2: Logo A, 4 digit Date Code

Bottom Mark: Assembly Lot Number, first 10 digits
equally split into 2 rows

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Active Area Depth = 0.36 mm REF

E Hall element; not to scale

**Figure 13: TSSOP-8 (LE) Package Drawing**



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

## Revision History

| Number | Date | Description |
|---|---|---|
| – | March 13, 2025 | Initial release |





Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com