A33023

Stray Field Immune, High-Speed, Hall-Effect Angle Sensor IC

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC for angular position, rotational speed, and direction measurement
  - Hall-effect technology
  - End of shaft
  - Stray field immune
- Designed to meet ASIL D top-level safety requirements in a single-die package when used in conjunction with appropriate system-level control
- 11.2 bits noise-free resolution with 300 G field and 12.5 kHz bandwidth at 25°C
- Default 25 µs latency with 12.5 kHz bandwidth
  - Programmable from 15 µs to 45 µs
- Wide operating voltage (3.7 V to 18 V) enables direct connection to vehicle battery
- Linearization to reduce error from misalignment between the sensor and target magnet.
- SPI interface allows use of multiple independent sensors for applications requiring redundancy
- 5-bit CRC on SPI messages
- ABI and UVW interfaces provide high resolution and lowest latency angle information
- EEPROM with Error Correction Control (ECC) for trimming calibration
- EEPROM programmable angle reference (0°) position and rotation direction (CW or CCW)
- AEC-Q100 grade 0 qualification

DESCRIPTION

The A33023 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic sensing technology. The A33023 is a system-on-chip (SoC) architecture that includes angle sensing, digital signal processing, and various output options: SPI, PWM, motor commutation (U,V,W), and encoder outputs (A, B, I). Also integrated in the device is on-chip EEPROM technology, capable of supporting a high number of read/write cycles, for flexible end-of-line programming of calibration parameters.

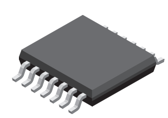
The low 25 µs latency of the A33023 makes it ideal for automotive applications requiring fast 0° to 360° angle measurements, such as electronic power steering (EPS), seatbelt motor systems, transmission actuators, shift-by-wire systems, electronic braking systems, and throttle systems.

The A33023 is targeting single-die ASIL D compliance when used in conjunction with appropriate system level controls.

The A33023 also includes integrated linearization features. This allows the A33023 to correct for misalignment between the IC and the target magnet with minimal added latency.

The A33023 is available in a single-die 14-pin TSSOP package. The package is lead (Pb) free with 100% matte-tin lead frame plating. The A33023 is qualified to AEC-Q100 grade 0.

PACKAGE:



14-pin TSSOP
(Suffix LE)

Not to scale

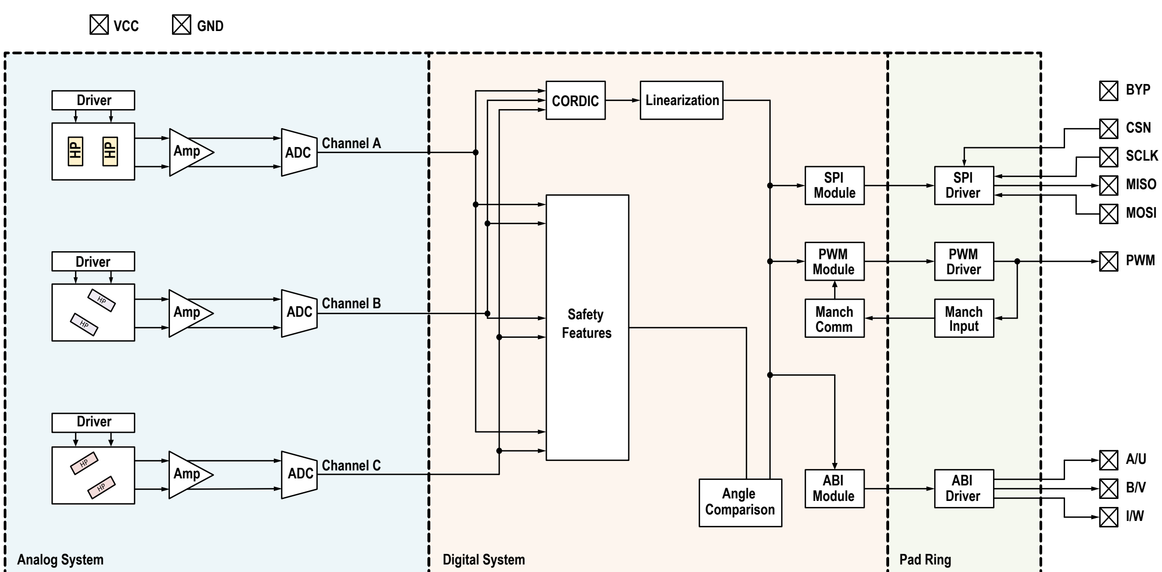


Figure 1: Functional Block Diagram

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SELECTION GUIDE

Part Number	Target Magnet Field Range (G)	Interface Voltage (V)	Package	Packing
A33023LLEATR-300	200 to 400	3.3	14-pin TSSOP	4000 pieces per 13-in. reel
A33023LLEATR-600	300 to 600	3.3		
A33023LLEATR--300-5	200 to 400	5		
A33023LLEATR-600-5	300 to 600	5		

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	38	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
Digital I/O Forward Voltage (MOSI, MISO, SCLK, CS, A/U, B/V, I/W, WAKE, BYP)	V_{DIG}	3.3 V or 5 V interface selected	5.65	V
Digital I/O Reverse Voltage	V_{RDIG}		–0.5	V
PWM Forward Voltage	V_{PWM}		18	V
PWM Reverse Voltage	V_{RPWM}		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{STG}		–65 to 170	°C
ESD Rating	V_{HBM}	HBM testing per AEC-Q100	>4	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Operating Characteristics section.

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package, measured on JEDEC JESD51-7 2s2p board	82	°C/W

*Additional thermal information available on the Allegro website.

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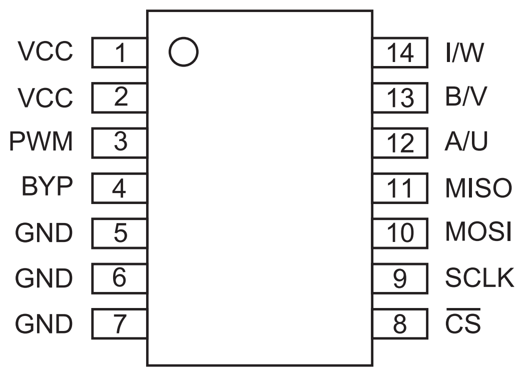
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LE 14-pin TSSOP Pinout Drawing

Terminal List Table

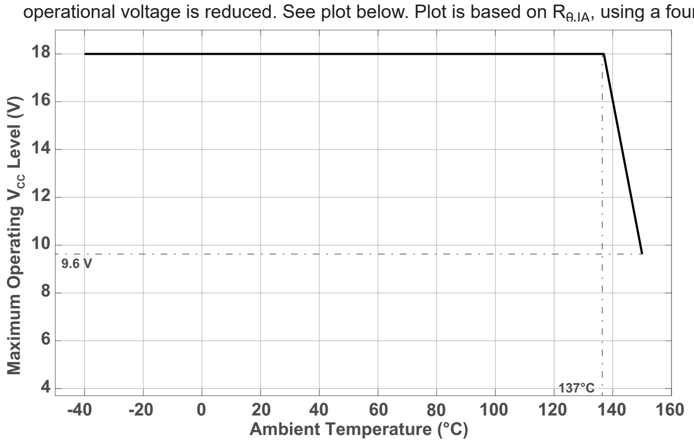
Number	Name	Function
1,2	VCC	Power supply
3	PWM	PWM output and Manchester Communications
4	BYP	External bypass capacitor terminal for internal regulator
5, 6, 7	GND	Device ground terminal
8	$\overline{\text{CS}}$	SPI Chip Select terminal (active low input)
9	SCLK	SPI Clock terminal input
10	MOSI	SPI Master Output / Slave Input
11	MISO	SPI Master Input / Slave Output
12	A/U	Option 1: Quadrature A output signal Option 2: U output signal
13	B/V	Option 1: Quadrature B output signal Option 2: V output signal
14	I/W	Option 1: Quadrature I (index) output signal Option 2: W output signal

CHARACTERISTIC PERFORMANCE

OPERATING CHARACTERISTICS: Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1][5]	V_{CC}	Interface voltage 3.3 V	3.7	–	18	V
		Interface voltage 5.0 V	4.8	–	18	V
Supply Current	I_{CC}	Sampling angles, $T_A \geq 25°C$	–	–	19	mA
		Sampling angles, $T_A < 25°C$	–	–	22	mA
Clock Frequency	f_{CLK}	Main oscillator, ADC Signal Processing oscillator	13.6	16	18.4	MHz
		2 MHz oscillator	1.7	2	2.3	MHz
		250 kHz oscillator	212.5	250	287.5	kHz
Undervoltage Flag Threshold	$V_{UVD(HIGH)}$	Maximum V_{CC}, dV/dt = +1 V/ms, T_A = 25°C, A33023 sampling enabled	–	–	3.75	V
	$V_{UVD(LOW)}$	Maximum V_{CC}, dV/dt = –1 V/ms, T_A = 25°C, A33023 sampling disabled	3.4	–	–	V
Overvoltage Flag Threshold [4]	$V_{OVD(HIGH)}$	V_{CC} rising	21	22	–	V
	$V_{OVD(LOW)}$	V_{CC} falling	20	21	–	V
Forward Supply Zener Clamp Voltage	V_{ZUP}	$I_{CC} = I_{CC(max)}$ + 3 mA	38	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RZUP}	$I_{CC} = I_{RCC(min)}$	–	–	–18	V
Reverse Battery Current	I_{RCC}	V_{CC} = –18 V	–5	–	–	mA
Power-On Time [2][3]	t_{PO}		–	1	–	ms

[1] Conditions of maximum supply voltage and ambient temperature must not exceed maximum junction temperature. At elevated ambient temperatures, the maximum operational voltage is reduced. See plot below. Plot is based on $R_{\theta JA}$, using a four-layer JEDEC standard PCB.



[2] During the power-on phase, the SPI transactions will be valid within ≈ 500 µs of power on. Angle reading requires full t_{PO} to stabilize (typical expected approximately 1 ms). Angle is considered valid once ang_rdy (bit 0 of serial address 0xC is set to '1', and no error flags are present).
[3] Parameter is not measured at final test. Determined by design
[4] Contact Allegro for additional OVLO threshold options
[5] Supply voltage ramp rate should be no slower than 1 V/ms when first energizing. Once device is powered on, the rate of change on V_{CC} must be limited to less than 1 V/µs.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Bandwidth	BW	iir_bw_sel = 0b00	–	6.25	–	kHz
		iir_bw_sel = 0b01	–	12.5	–	kHz
		iir_bw_sel = 0b10	–	25	–	kHz
		iir_bw_sel = 0b11	–	50	–	kHz
Bypass Pin Output Voltage [1]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V Interface Voltage	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5 V Interface Voltage, V_{CC} ≥ 6 V	4.35	5	5.65	V
SPI AND ABI /UVW INTERFACE SPECIFICATIONS [2]						
Load Resistance	R_L		100	–	–	kΩ
Load Capacitance	C_L	Loading on digital output (MISO and ABI/UVW) pin with frequency up to 10 MHz	–	–	20	pF
		Loading on digital output (MISO and ABI/UVW) pin with frequency up to 1 MHz	–	–	50	pF
SPI AND ABI/UVW INTERFACE VOLTAGE SPECIFICATIONS (3.3 V MODE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, /CS pins, I_{OUT} ≤ 70 µA	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, /CS pins, I_{OUT} ≤ 70 µA	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20pF, T_A = 25°C	2.93	3.3	3.63	V
Digital Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20pF, T_A = 25°C	–	0.3	0.5	V
SPI AND ABI/UVW INTERFACE VOLTAGE SPECIFICATIONS (5 V MODE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, /CS pins, V_{CC} ≥ 6 V, I_{OUT} ≤ 70 µA	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, /CS pins, V_{CC} ≥ 6 V, I_{OUT} ≤ 70 µA	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF, T_A = 25°C, V_{CC} > 6 V	4	5	5.5	V
Digital Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF, T_A = 25°C, V_{CC} > 6 V	–	0.3	0.5	V
SPI INTERFACE TIMING SPECIFICATIONS [2]						
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	t_{SPI}	SPI message is 32 bits	3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from CS going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time CS must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge, C_L ≤ 20 pF	–	–	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before CS rising edge	5	–	–	ns

[1] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.
[2] Parameter is not measured at final test. Determined by design.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	PWM Frequency Min. Setting, T_A in specification	–	125	–	Hz
		PWM Programmable options	–	16	–	steps
		PWM Frequency Max. Setting, T_A in specification	–	16	–	kHz
PWM Output Leakage Current		Output voltage ≤ 5.5 V, output FET off	–	–	100	µA
PWM Output Low Clamp [1]	$D_{PWM(min)}$	2% corresponds to pwm_porch_sel EEPROM field sets to 000; 8% corresponds to pwm_porch_sel EEPROM field sets to 110	2	–	8	%
PWM Output High Clamp [1]	$D_{PWM(max)}$	92% corresponds to pwm_porch_sel EEPROM field sets to 110; 98% corresponds to pwm_porch_sel EEPROM field sets to 000	92	–	98	%
PWM Output Clamp Step Size [1]	$D_{PWM(step\_size)}$	pwm_porch_sel EEPROM field	–	1	–	%
PWM Saturation Voltage	$V_{PWMSAT(LOW)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.35	V
PWM Maximum Operational Pull-Up Voltage	V_{SPWM}		–	–	5.65	V
PWM Output Current Limiter	$I_{PWMLIMIT}$	Output FET on, T_A = 25°C; Short circuit protection	20	–	50	mA
PWM Max. Operational Current [1]	$I_{PWMSC(SINK)}$	Recommended max. operational PWM current	–	–	20	mA
PWM Load Capacitance [1]	C_{PWMLX}		–	–	4.7	nF
Output Load Resistance	$R_{P(PULLUP)}$		–	1500	–	Ω
INCREMENTAL OUTPUT SPECIFICATIONS [1]						
ABI and UVW Output Angular Hysteresis	hys_{ANG}	Programmable	0	–	1.41	degrees
AB Channel Resolution	RES_{AB}	Programmable via EEPROM, 4-bit field, specified in pulses per revolution, PPR	1	–	2048	PPR
AB Quadrature Resolution	RES_{AB_INT}	Equal to 4 × RESAB, specified in counts per revolution, CPR	4	–	8192	CPR
UVW Poles Pairs	N_{pole}	DC commutation signals; programmable via EEPROM, 4-bit field	1	–	16	pole pairs

[1] Parameter is not measured at final test. Determined by design.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
MAGNETIC CHARACTERISTICS						
Input Magnetic Flux Density [1]	B_{IN}	For “300” part variant	–	300 [2]	–	G
		For “600” part variant	–	450 [2]	–	G
Differential Input Magnetic Flux Density [1]	ΔB	For “300” part variant	–	–	400	G
		For “600” part variant	–	–	600	G
ANGLE CHARACTERISTICS						
Number of Angle Bits	N_{SPI}	Length of angle word	–	16	–	bits
Response Time [3][5]	$t_{RESPONSE}$	Angular latency, bandwidth = 6.25 kHz	39	45	51	μs
		Angular latency, bandwidth = 12.5 kHz	21.5	25	28.5	μs
		Angular latency, bandwidth = 25 kHz	17.5	20	22.5	μs
		Angular latency, bandwidth = 50 kHz	13	15	17	μs
Refresh Rate [4]	t_{ANG}	ABI Angle update rate with 8× interpolation (interpolator_bypass = 0, interpolator_rate = 0)	–	0.25	–	μs
		ABI Angle update rate with 4× interpolation (interpolator_bypass = 0, interpolator_rate = 1)	–	0.5	–	μs
		ABI Angle update rate; no interpolation (interpolator_bypass = 1)	–	2	–	μs
Angle Error [6]	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, RPM = 0	–1.0	±0.5	1.0	degrees
		T_A = 150°C, ideal magnet alignment, target RPM = 0	–2.0	±0.9	2.0	degrees
Angle Error Due to DC Stray Field [3]		T_A = 25°C, B_{stray} = 50 G DC, B_{IN} = 300 G	–	±0.1	±0.4	degrees
Angle Error Due to AC Stray Field [3]		T_A = 25°C, AC stray field according to ISO11452-8 Test Level IV, B_{IN} = 300 G	–	±0.1	±0.4	degrees
Angle Error Due to Temperature Drift [6]	$ANGLE_{DRIFT}$	Change in angle from 25°C; T_A = 150°C, ideal magnet alignment, target RPM = 0	–1.2	±0.5	1.2	degrees
		Change in angle from 25°C; T_A = –40°C, ideal magnet alignment, target RPM = 0	–	±0.5	–	degrees
Angle Drift Over Lifetime	$ANGLE_{DRIFT\_Life}$	B_{IN} = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] The Input Magnetic Flux Density B_{IN} and the Differential Input Magnetic Flux ΔB are defined in the “Input Magnetic Flux Density Definitions” section.
[2] There is no strict minimum value for B_{IN} as a smaller input field will only lead to a fairly low resolution: therefore, it is not recommended to operate below 200 G for the 300 part variant and below 300 G for the 600 part variant.
[3] Parameter is not measured at final test. Determined by design.
[4] The rate at which a new angle reading will be ready.
[5] Response time is measured at the time between the magnet crossing a given angle and the part reporting that angle.
[6] Angle Error and Drift inferred through channel characterization and signal path testing. Not directly measured at final test.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions			Min	Typ	Max	Unit
Angle Noise [3][4]	N_{ANG}	Target RPM = 0, 3 sigma; 300 G for "300" part variant; 450 G for "600" part variant	BW = 6.25 kHz	T_A = 25°C	–	0.065	–	degrees
				T_A = 150°C	–	0.110	–	degrees
			BW = 12.5 kHz	T_A = 25°C	–	0.075	–	degrees
				T_A = 150°C	–	0.160	–	degrees
			BW = 25 kHz	T_A = 25°C	–	0.100	–	degrees
				T_A = 150°C	–	0.180	–	degrees
			BW = 50 kHz	T_A = 25°C	–	0.120	–	degrees
				T_A = 150°C	–	0.240	–	degrees
ANGLE CHARACTERISTICS								
Noise Free Number of Bits [2][4]	b_{NOISE_FREE}	Target RPM = 0, 6 sigma; 300 G for "300" part variant; 450 G for "600" part variant	BW = 6.25 kHz	T_A = 25°C	–	11.4	–	bits
				T_A = 150°C	–	10.7	–	bits
			BW = 12.5 kHz	T_A = 25°C	–	11.2	–	bits
				T_A = 150°C	–	10.1	–	bits
			BW = 25 kHz	T_A = 25°C	–	10.8	–	bits
				T_A = 150°C	–	10.0	–	bits
			BW = 50 kHz	T_A = 25°C	–	10.6	–	bits
				T_A = 150°C	–	9.6	–	bits
TEMPERATURE SENSOR [1]								
Temperature	$TEMP_{BITS}$	Main and redundant			–	12	–	bits
Temperature Resolution		1°C = 8 counts			–	0.125	–	°C
Overtemperature Threshold	OVT				–	170	–	°C
	UVT				–	–60	–	°C

[1] Parameter is not measured at final test. Determined by design.
[2] The Noise Free Number of Bits is defined as: $log_2(360/(6×σ))$ where σ is the rms angle noise.
[3] This value represents 3-sigma or three times the standard deviation of the measured samples.
[4] Based on characterization data, not measured at final test.

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FUNCTIONAL DESCRIPTION

Overview

The A33023 is an automotive-qualified four channel rotary position sensor. The four channels provide redundant angle sensing within a single monolithic surface mount device.

This device is an advanced, programmable system-on-chip (SoC), incorporating six planar Hall-effect, analog signal conditioning, high-speed sampling A-to-D converters, digital filtering, digital signal processing (which includes two separate signal paths, primary and secondary), and multiple output options. Available outputs options include SPI, PWM, and motor commutation outputs (U, V, W) or encoder outputs (A, B, I).

The primary (or main) channel is comprised of six planar Hall plates measuring the magnetic field perpendicular to the package. The three secondary channels are each a subset of four Hall plates out of the six from the main channel (see Angle Measurements section below for more details). The information from each channel is processed in parallel to compute an angle measurement based on the input magnetic fields. The resulting angle information, primary and secondary, is passed through additional processing and made available as four independent outputs. In addition, the A33023 compares the primary angle to the secondary angles to monitor the integrity of the angle information.

Zero angle, filtering, linearization, and diagnostic adjustment options are available in the A33023. These options are configurable in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurements

The A33023 is capable of rejecting common-mode stray fields, based on the calculation of the equivalent center of mass of the measured magnetic fields. The concept of center of mass is an analogy to understand how the A33023 is a stray field immune sensor: if the same additional mass is applied to a group of weights, the angular position of the center of mass is unchanged. The A33023 has six planar Hall plates equally spaced in a 2 mm diameter circle (Figure 2, not to scale). The magnetic center is attracted toward a given Hall plate if it measures a positive magnetic field or repelled if it measures a negative magnetic field. While placed in front of the right rotating magnet, the magnetic center follows the same rotation as the magnet. The A33023 measures the position of this magnetic center and returns its angular position.

To evaluate the magnet angle position δ_{MAIN}, the A33023 realizes the following calculation:

$$\delta_{MAIN} = atan2\left(\frac{\frac{\sqrt{3}}{2}(CH_B + CH_C)}{CH_A + \frac{1}{2}(CH_B - CH_C)}\right)$$

Equation 1: Magnet angle position calculation

with:

- CH_A = HP1-HP4
- CH_B = HP2-HP5
- CH_C = HP3-HP6

HPi is the magnetic field measured by the Hall plate i along the direction Z, perpendicular to the surface of the chip.

The A33023 also measures three redundant angles using the functions f_1, f_2 and f_3:

- $\delta_{AB} = f_1(CH_A, CH_B)$
- $\delta_{BC} = f_2(CH_B, CH_C)$
- $\delta_{CA} = f_3(CH_C, CH_A)$

The A33023 compares the main and redundant angles at each clock cycle and switches to safe state if a sufficiently high mismatch is detected.

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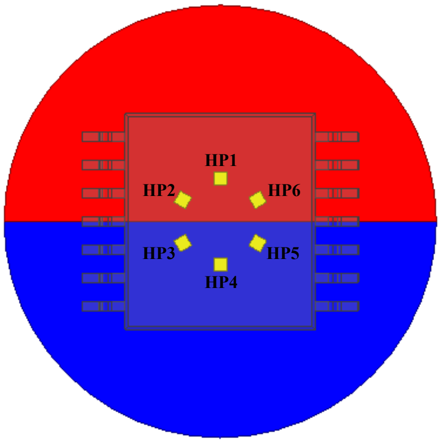

Figure 2: Axial view of the A33023 and the cylinder magnet with diametrical magnetization

The A33023 is intended to work as an end-of-shaft angle sensor in front of a rotating magnet. To achieve 360° absolute angle position, the magnet can be:

- A two poles ring, cylinder, or block magnet with a diametrical magnetization (Figure 3). The typical magnetic field seen by these channels is shown in Figure 4.
- A four poles ring, cylinder, or block magnet with the magnetization parallel to the axis of rotation (Figure 5).

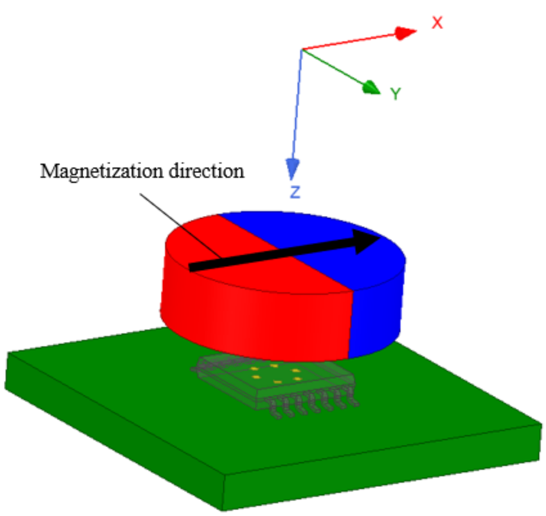

Figure 3: Isometric view of the A33023 and the cylinder magnet with diametrical magnetization

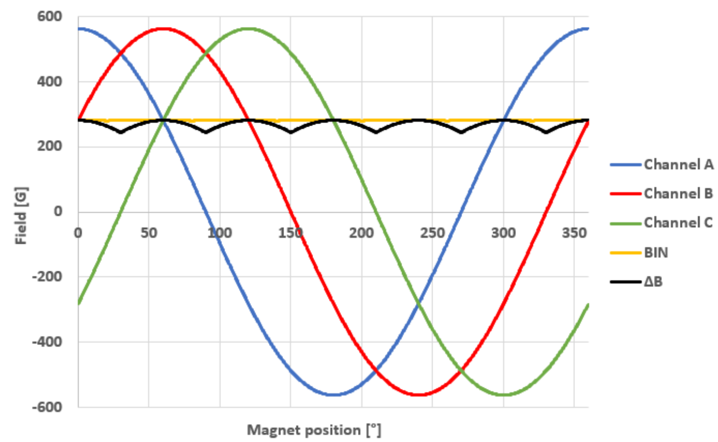

Figure 4: Differential channels CH, input magnetic field B_{IN} and input differential field ΔB versus magnet position, with ideal IC positioning versus the magnet rotation axis

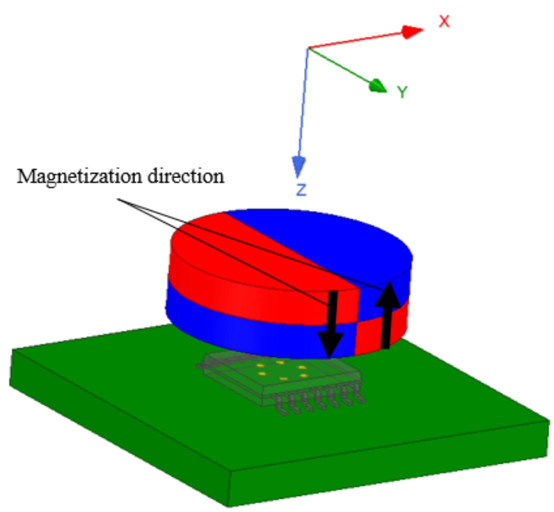

Figure 5: Isometric view of the A33023 and the cylinder magnet with four poles axial magnetization

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Input Magnetic Flux Density Definitions

The Input Magnetic Flux Density B_{IN} is defined below:

$$B_{IN} = \frac{1}{3} \times \sqrt{\left(\frac{\sqrt{3}}{2}(CH_B + CH_C)\right)^2 + \left(CH_A + \frac{1}{2}(CH_B - CH_C)\right)^2}$$

Equation 2: Input magnetic flux density

This input field is the value that defines the actual resolution of the system: the higher B_{IN}, the better the resolution.

The Differential Input Magnetic Flux Density ΔB is defined below:

$$\Delta B = \frac{1}{2} \times \max\left(|CH_A|, |CH_B|, |CH_C|\right)$$

It corresponds to half the maximum absolute value of any of the three differential channels.

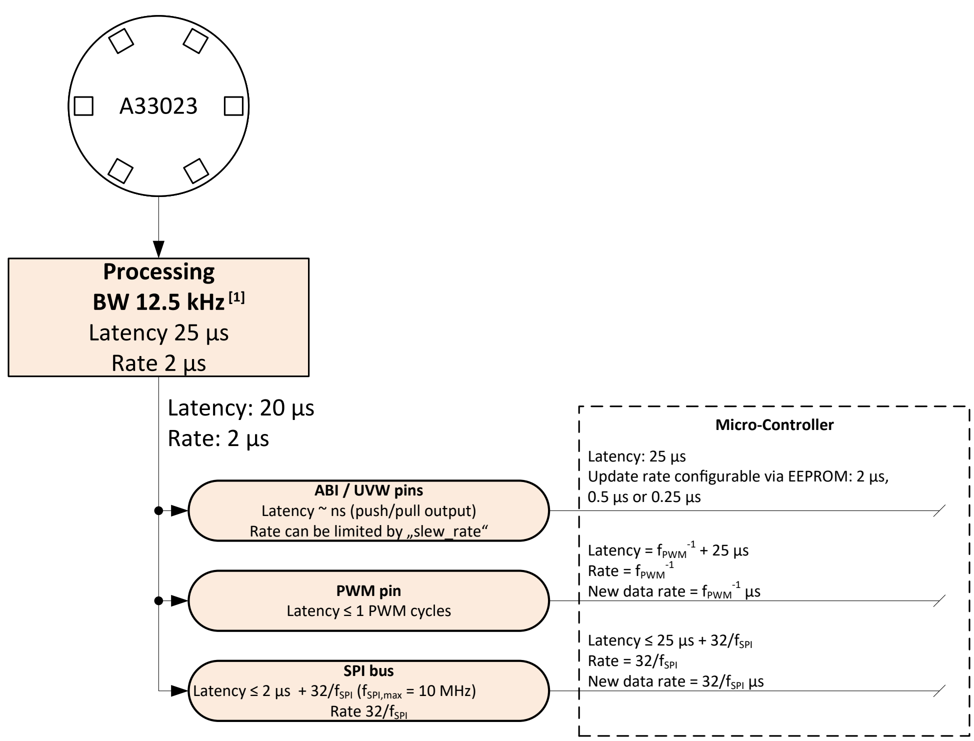
Note that, by definition, with the A33023 perfectly centered over a cylindrical magnet diametrically magnetized, and only in this case, B_{IN} is equal to the max single ended field over a 360° rotation.

$$B_{IN} = \max(\Delta B) = \max(HPi)\ with\ i = 1{:}6$$

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. The delay from time of the input until generation of a processed angle value is $t_{RESPONSE}$. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. Register values transmitted are latched on the first SCLK edge of the SPI response frame. This results in a variable age of the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$.



[1] Bandwidth adjustable via EEPROM.

Figure 6: Signal Path Block Diagram Corresponding to Bandwidth 12.5 kHz

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Impact of High-Speed Sensing

Due to signal path latency, the angle information is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e., a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm) and is referred to as angular lag.

The lag is directly proportional to rpm, and may be compensated for externally, if the velocity is known.

Operational Modes

PWM OUTPUT

The A33023 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to the main channel angle output. The PWM output is enabled by setting the parameter pwm_enable (extended: 0x3F [17])

The PWM period is defined as shown in Figure 7. The PWM period may be measured by observing the rising edge to rising edge time. The PWM duty cycle is the rising edge to falling edge time as a percent of the PWM period. The fixed front porch and back porch are configurable by the EEPROM parameter pwm_porch_sel (extended: 0x3F [13:11]). The front and back porches are used to identify the PWM frame by the host. The parameter pwm_period (extended: 0x3F [10:7]) configures the PWM carrier frequency.

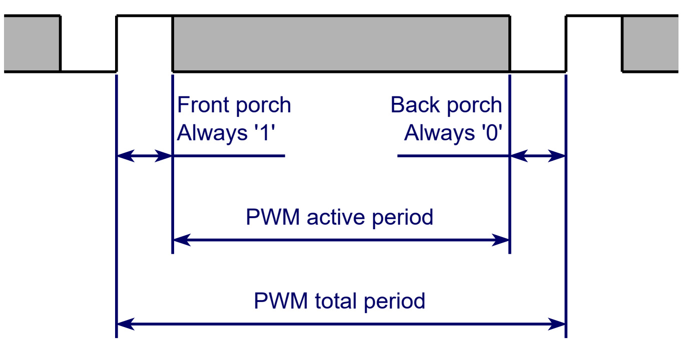

Figure 7: PWM Terms Definition

Table 1: pwm_porch_sel

Value	Fixed Time (% Duty Cycle) (Fixed Time = Front Porch = Back Porch)
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	0

Table 2: pwm_period

Value	Frequency (Hz)
0	125
1	167
2	250
3	333
4	500
5	667
6	800
7	1000
8	1333
9	1600
10	2000
11	2667
12	4000
13	5333
14	8000
15	16000

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Incremental Output Interface (ABI)

The A33023 offers an incremental output mode in the form of quadrature A/B and Index outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per magnetic revolution, giving a cycle resolution of $(360 / 2^N)$ degrees per cycle. B is offset from A by ¼ of the cycle period. The "I" signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown in Figure 8.

Since A and B are offset by ¼ of a cycle, they are in quadrature and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

Table 3: Quadrature States

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a gray coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4
Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2→ Q1

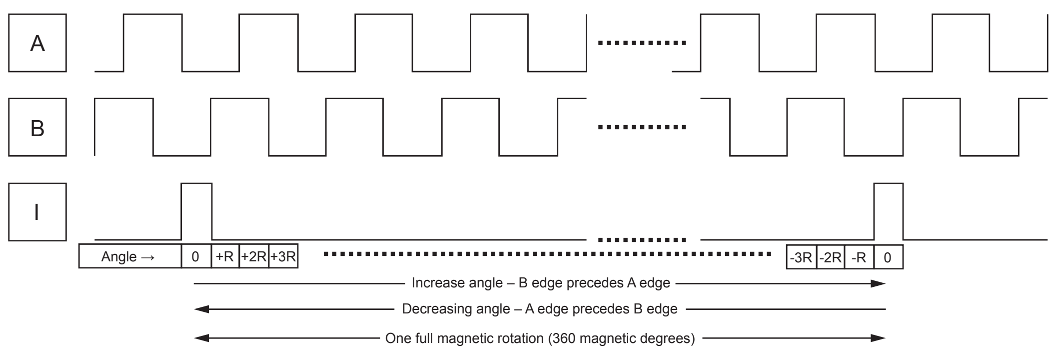

Figure 8: One Full Magnetic Revolution

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The duration of one cycle is referred to as 360 electrical degrees, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior.

Ideally, the A and B cycle would be as shown below for a constant velocity:

Practically, the edge rate of the A and B signals, and the switching threshold of the receiver I/Os, will affect the quadrature periods. Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

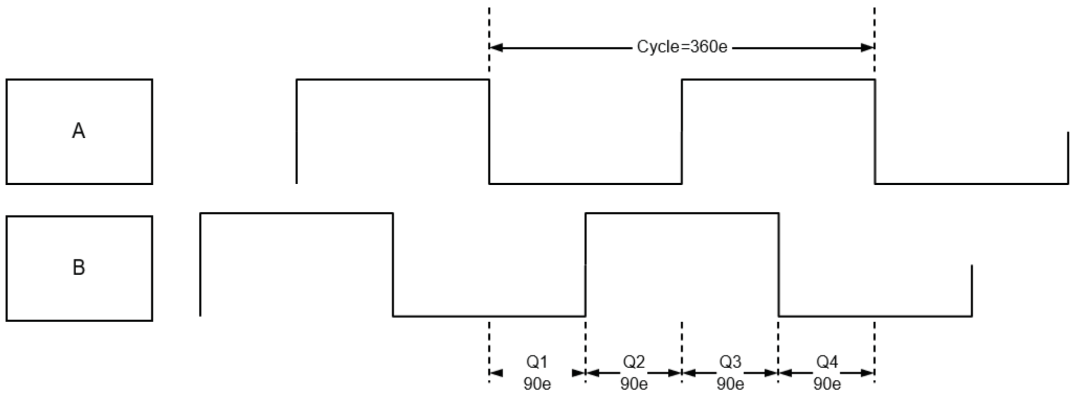

Figure 9: Electrical Cycle

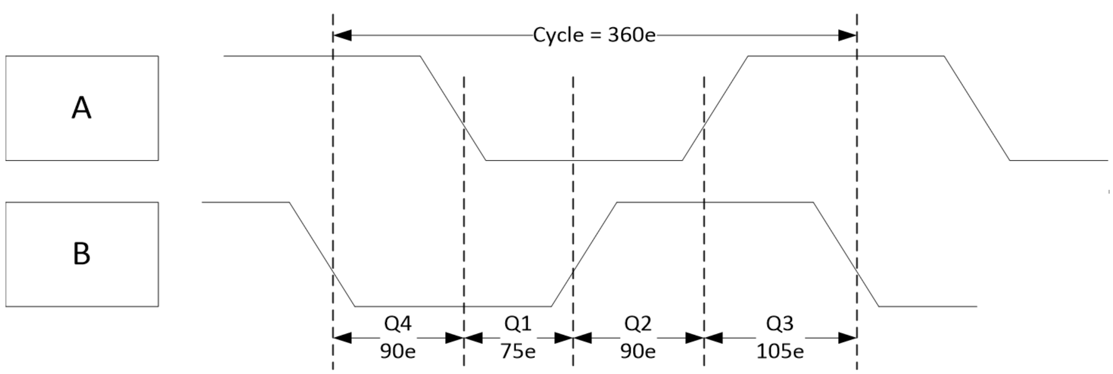

Figure 10: Electrical Cycle

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ABI/UVW OUTPUT CONFIGURATION

The A33023 uses three pins to output either ABI information or UVW information. The main angle is used to generate the ABI signals. The parameter abi_0_uvw_1 (extended: 0x25 [0]) selects the protocol ABI or UVW. The ABI or UVW outputs are enabled or disabled by setting the parameter abi_uvw_en (extended: 0x25 [15]).

The A33023 ABI output resolution and quantity of UVW pole pairs is configurable by setting the parameter abi_uvw_resolution (extended: 0x25 [5:2]) The options for ABI Cycle Resolution and Quadrature State Resolution are shown in Table 4.

Figure 11 shows the maximum RPM for a given ABI resolution. A rotation rate faster than that shown in the figure will result in a skipped ABI step. In this case slew rate limiting (see Slew Rate Limiting Section) will be required to maintain absolute angle position via ABI.

Table 4: ABI/UVW Cycle Resolution and Quadrature State Resolution

abi_uvw_resolution	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = N+2)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)	UVW Quantity of Poles-Pairs	UVW Cycle Width (Mechanical Degrees)
0*	14	16	16384	65536	0.0220	0.0055	1	360.00
1*	13	15	8192	32768	0.0439	0.0110	2	180.00
2*	12	14	4096	16384	0.0879	0.0220	3	120.00
3	11	13	2048	8192	0.1758	0.0439	4	90.00
4	10	12	1024	4096	0.3516	0.0879	5	72.00
5	9	11	512	2048	0.7031	0.1758	6	60.00
6	8	10	256	1024	1.4063	0.3516	7	51.43
7	7	9	128	512	2.8125	0.7031	8	45.00
8	6	8	64	256	5.6250	1.4063	9	40.00
9	5	7	32	128	11.2500	2.8125	10	36.00
10	4	6	16	64	22.5000	5.6250	11	32.73
11	3	5	8	32	45.0000	11.2500	12	30.00
12	2	4	4	16	90.0000	22.5000	13	27.69
13	1	3	2	8	180.0000	45.000	14	25.71
14	0	2	1	4	360.0000	90.000	15	24.00
15	N/A	N/A	N/A	N/A	N/A	N/A	16	22.50

* Not recommended for use with ABI.

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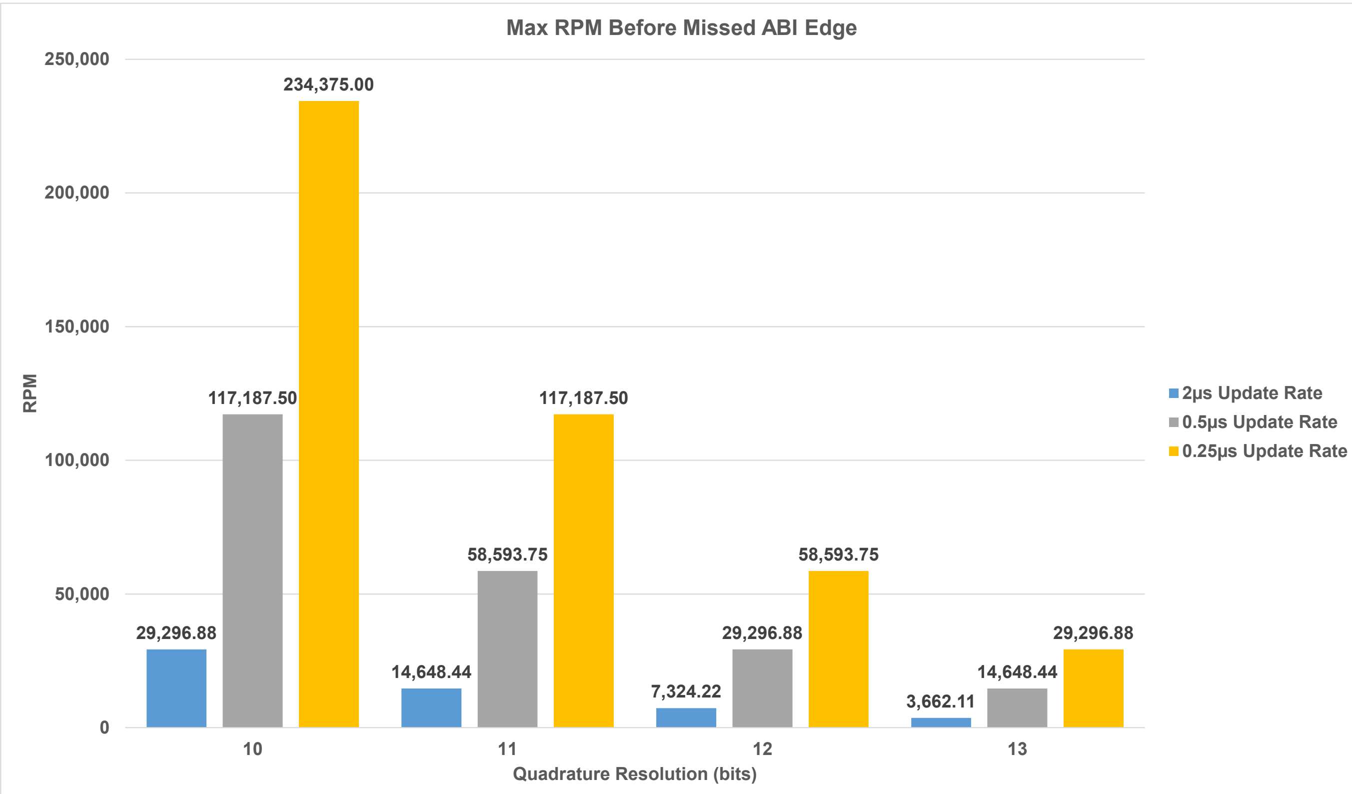

Figure 11: A33023 / abi_uvw_resolution selection

ABI INVERSION

The logic levels of the ABI pins may be inverted by setting the abi_uvw_invert_out_en (extended: 0x25 [1]) bit within EEPROM. This also applies if using the UVW output logic.

INDEX PULSE

The index pulse I (or Z in some descriptions) marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the "I" pulse has four widths, defined by the abi_index_mode EEPROM field (extended: 0x25 [13:12]):

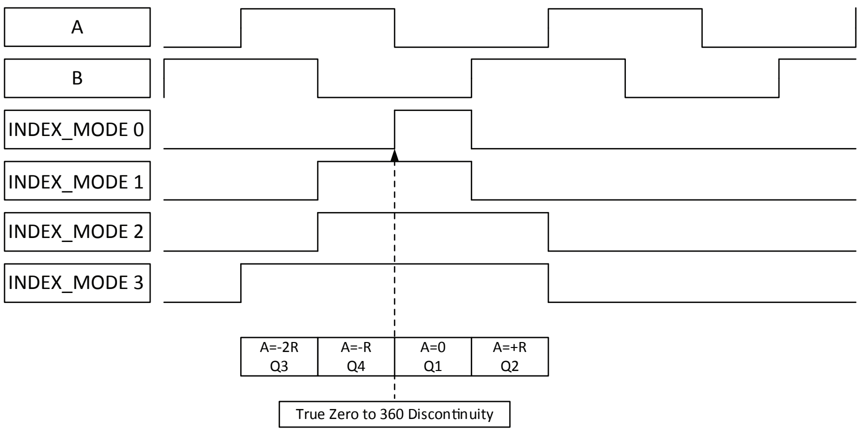

Figure 12: Index Pulse

ABI Behavior at Power-Up

ABI interface can be configured to communicate the current absolute angle position at power-on. The behavior at start-up is the following.

- During t_{PO_D} the interface is determined by the error reporting on ABI and PWM.
  - Depending on the error reporting mode and PWM frequency, this state may require ≈16 ms to clear.
- The interface will catch-up with the actual measured angle by moving in a positive or negative direction, whichever is faster. The time for catching up is at most:

$$t_{SETTLE(MAX)} = \frac{180°}{R} \times \text{ABI\_slew\_time}$$

- After catching up with the measured angle, the sensor will operate normally.

If abi_slew_rate is set to 0, there is no catch-up phase. The output will jump to the final position immediately.

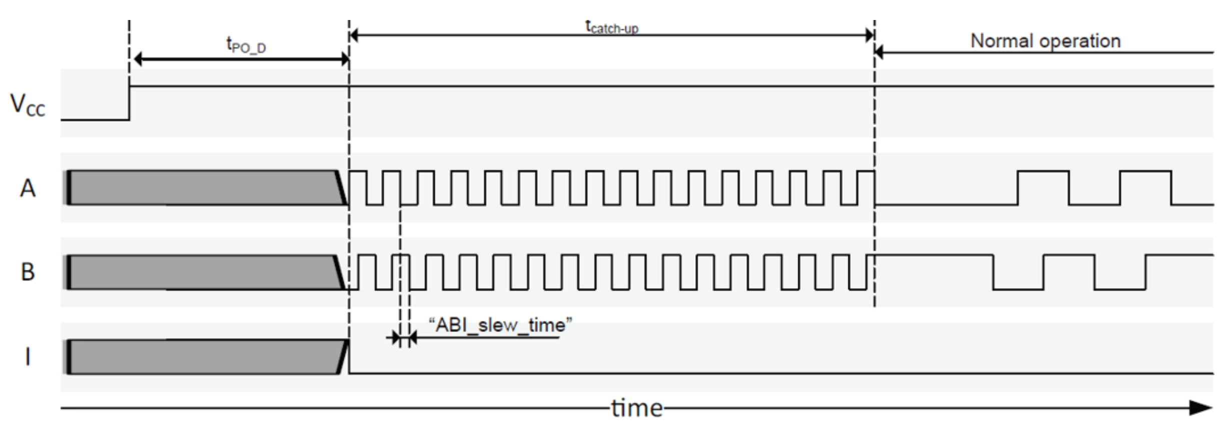

Figure 13: ABI Startup Behavior

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Zero Degree Position Indication

The edge of the index pulse corresponding to the zero position, as observed by the sensor, will change based on rotation direction, as shown in Figure 14.

With the magnet rotating such that the observed angle is increasing, the 0° position will be indicated by the rising edge of the Index pulse. If the magnet is rotated in the opposite direction (or if rot_dir_p and rot_dir_s are changed) to produce a decreasing angle value, the 0° position will be represented by the falling edge of the Index pulse.

The ABI resolution and "I" pulse mode selection (described above in Figure 13) determine the width of the Index pulse and the corresponding shift zero position indication.

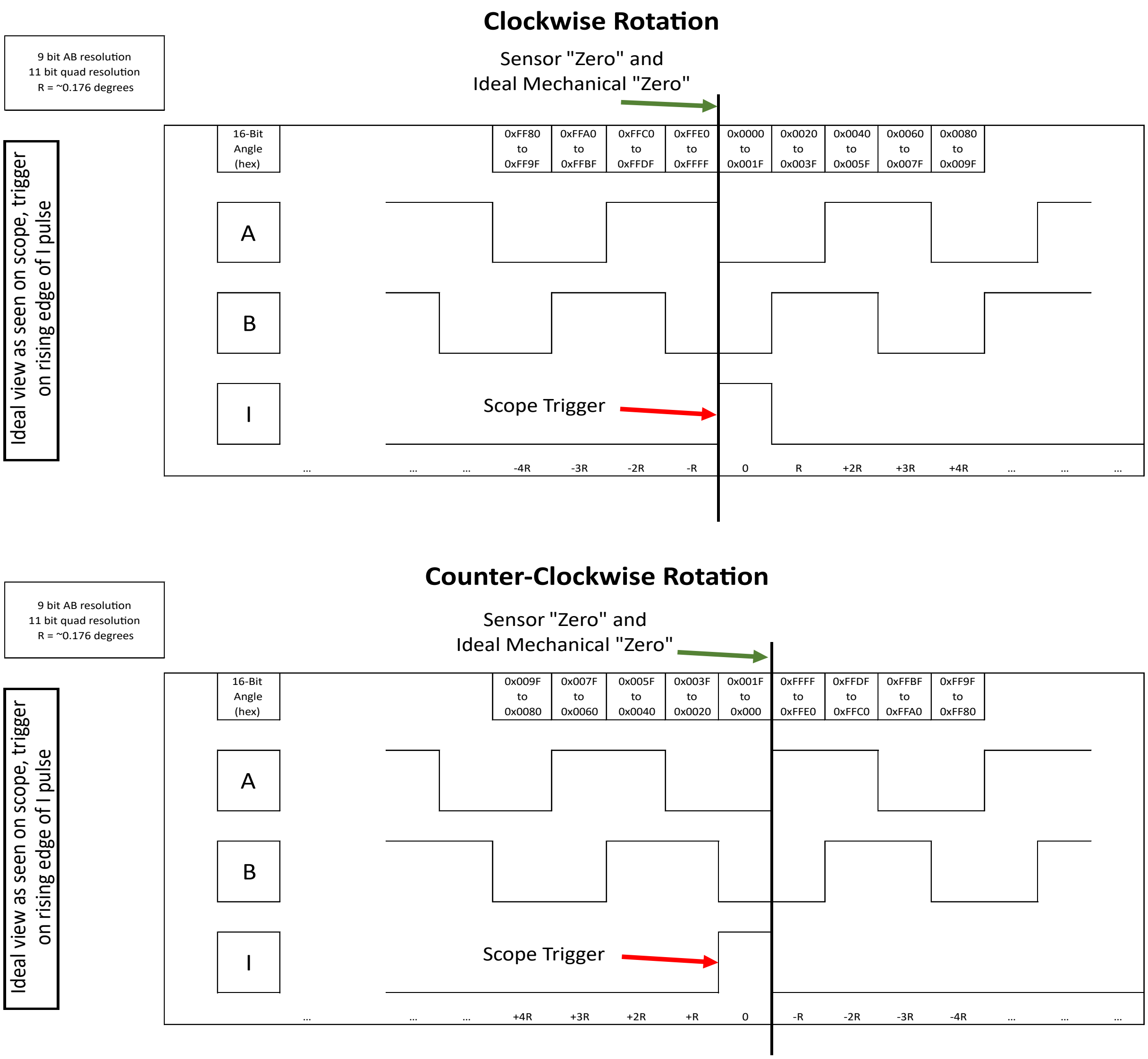

Figure 14: Index Pulse Corresponding to "Zero" Position

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Slew Rate Limiting for ABI

Slew rate limiting feature may be used to reduce quadrature state errors. The feature is enabled by setting a non-zero value to the parameter abi_slew_rate (extended: 0x25 [11:6]). The slew time sets the minimum amount of time that the output must remain in its current state before changing to the next state. This prevents the output from skipping states and can ensure controllers are able to read the state before it changes. This option separates the sensor's observed angle change from the ABI output rate and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby skipping one or more quadrature states. In this case, the slew rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output catches up with the angle samples, at which point the normal sample rate output resumes. This skipping will most likely occur either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 0.25 µs (default refresh rate for ABI). The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation would not on average require ABI transitions greater than the angle sample rate.

In both cases, the ABI output will correctly track the rotation position; however, the speed of the ABI edges will be accomplished at the slew rate limit set in EEPROM. Whenever slew rate limiting occurs, the slr flag (primary: 0x0C [4]) asserts to inform the system of the occurrence.

Figure 13 illustrates the difference between a bad ABI without slew rate limiting and the corrected output via slew rate limiting.

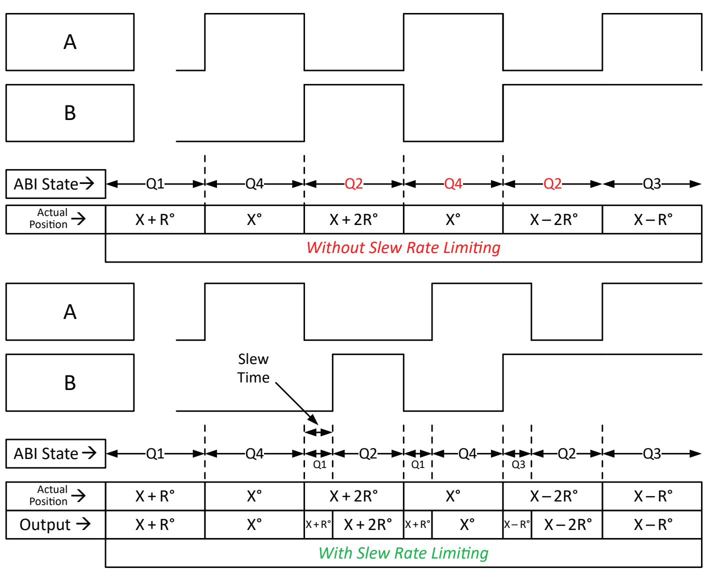

Figure 15: Slew Rate Limiting

Effective Speed of Slew Time

When slew rate limiting occurs, the ABI update rate is no longer dependent on the observed rotation rate, but instead occurs at a period set by the following EEPROM parameters. This change in the edge rate is observed as a change in the target velocity, and this perceived velocity depends on the following parameters:

- abi_slew_rate (extended: 0x25 [11:6])
- abi_uvw_resolution (extended: 0x25 [5:2])

Table 5 shows the equivalent rpm for select combinations of slew time and ABI resolution. abi_slew_rate sets to 0 disables the slew rate limiting.

When designing a system, it is important to note these rpm will occur for any change in rotation direction (i.e., motor transitioning from CW to CCW rotation), when both hysteresis and ABI slew rate limiting are enabled, as the IC back fills the ABI edges for the programmed hysteresis window angle_hyst (extended: 0x25 [22:20]).

Table 5: Equivalent RPMs for select combinations of slew time and ABI resolution

EEPROM Setting		Equivalent Velocity (rpm) based on AB Quadrature Resolution		
abi_slew_rate (Decimal)	Slew Time (µs)	12-Bit Quadrature	11-Bit Quadrature	10-Bit Quadrature
1	0.25	58593.8	117187.5	234375.0
2	0.375	39062.5	78125.0	156250.0
3	0.5	29296.9	58593.8	117187.5
4	0.625	23,437.5	46875.0	93750.0
5	0.75	19531.3	39062.5	78125.0
6	0.875	16741.1	33482.1	66964.3
7	1	14648.4	29296.9	58593.8
8	1.125	13020.8	26041.7	52083.3
…	…	…	…	…
62	7.875	1860.1	3720.2	7440.5
63	8	1831.1	3662.1	7324.2

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Brushless DC Motor Output (UVW)

The A33023 features U, V, and W output signals for stator commutation of brushless DC (BLDC) motors. The output is mode-selectable for 1 to 16 pole-pairs. The BLDC signals (U, V, and W) are generated based on the quantity of pole-pairs and on angle information from either the primary or secondary channel.

The U, V, and W outputs switch when the measured mechanical angle crosses the value where a change should occur. If hysteresis is used, then the UVW edges will update based off the rotation direction and hysteresis window. Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. Figure 17 and Figure 18 below show the U, V, and W example waveforms for three and five pole-pair BLDC motors.

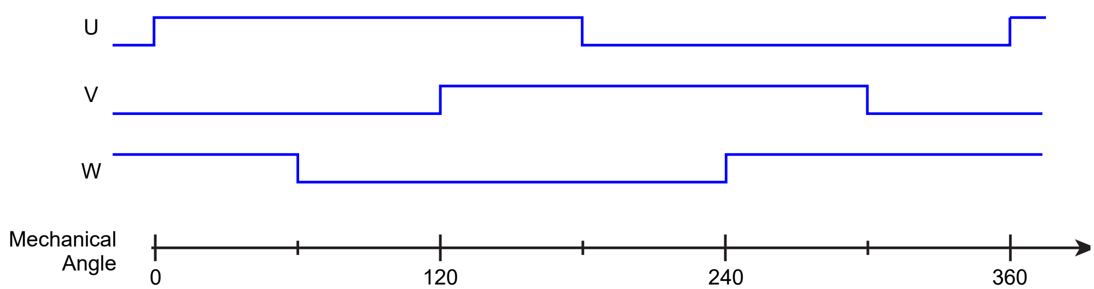

Figure 16: U, V, W Outputs for a 1 Pole-Pair BLDC Motor

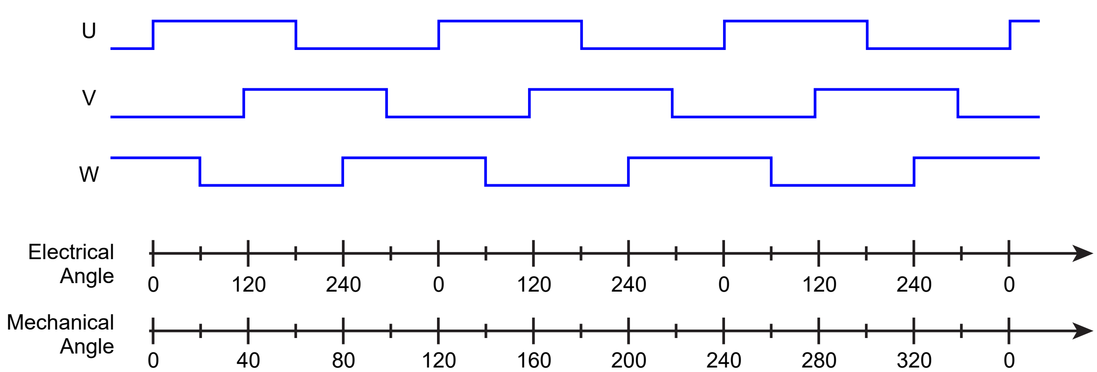

Figure 17: U, V, and W Outputs for Three Pole-Pair BLDC Motor

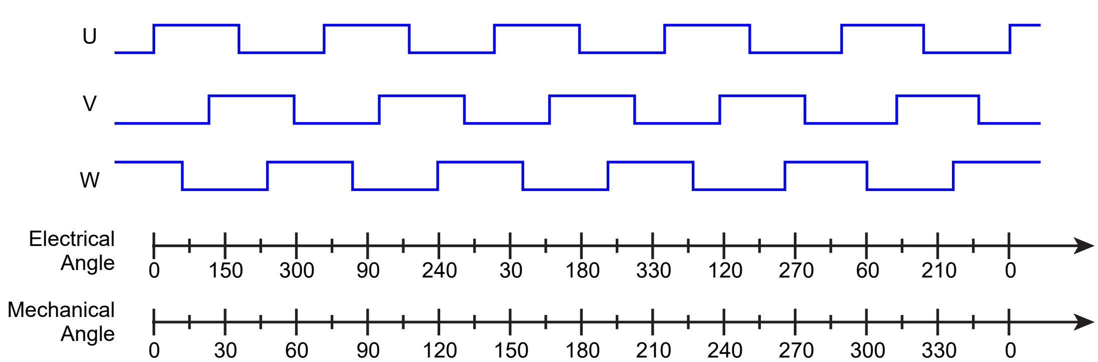

Figure 18: U, V, and W Outputs for Five Pole-Pair BLDC Motor

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. The parameter angle_hys (extended: 0x25 [22:20]) defines the width of an angle window at 16 bits. Mathematically, the width of this window in degrees is:

$$\textit{Angle Hysteresis} = \frac{360}{2^{16}} \times 2^{(angle\_hys+1)}$$

The parameter angle_hys is a 3-bit EEPROM field, allowing a range of ≈0.01° to ≈1.41° of hysteresis to be applied. The hysteresis compensated angle is applied to the UVW/ABI output. This same angle populates the abi_uvw_angle field (primary: 0x14 [15:0]) within the primary serial register space and may be read via SPI.

The effect of the hysteresis is shown in Figure 19. The current angle position as measured by the sensor is at the “head” of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the hysteresis-compensated angle is equal to the channel angle output, minimizing latency. If the sensor angle reverses direction, the hysteresis-compensated angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the “head” was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or head for the purposes of hysteresis, is reported by the parameter rot_h (primary: 0xC [1]).

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle will skip consecutive resolution steps.
   A. To prevent skipped ABI steps, a non-zero slew rate should be set whenever hysteresis is applied.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle will tend to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current head) rather than to the average position of the jitter.

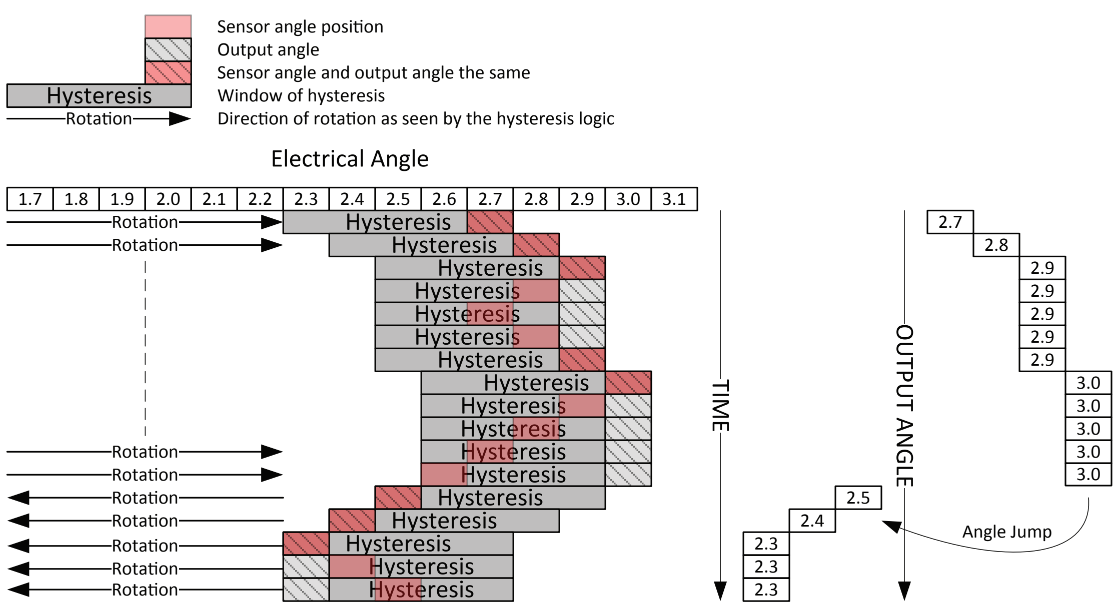

Figure 19: Effect of Hysteresis

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Linearization Feature

The A33023 contains sixteen fixed segments linearization for the main and all three redundant signal paths. Linearization allows for the conversion of the sensor measured magnetic field data into a customer desired output. This can be used to correct minor imperfections in the magnet or mounting tolerances.

Linearization converts the measured angle (sensed by the IC) into a corrected output angle. Typically, this is used to align the measured angle to the mechanical angle (the actual magnet position).

The IC performs linearization by taking the measured angle and adding / subtracting a correction factor. This correction factor will differ over measured angle and is based on linearization coefficients stored in EEPROM. There are 16 coefficients, or y entries (16 for each main and redundant channels), corresponding to 16 measured angles corresponding to [0° 22.5° 45° … 315° 337.5°]. For electrical angles not matching an entry in the EEPROM table, the correction factor is calculated by linearly interpolating between the two closest coefficients.

The y linearization EEPROM fields are 8-bit signed values, each coefficient has a range of –128 to 127 LSB, corresponding to a correction of –11.25 to +11.25 degrees (0.088° step size). The EEPROM fields name are XX_linearization_YY with XX standing for ab, bc, ca or main and YY ranging from 0 to 15. YY = 0 corresponds to the angle correction for the measured position 0°. YY = 1 corresponds to the angle correction for the measured position 22.5°. See Table 6 for more details. For example, main_linearization_7 is the angle correction applied to the measured main_angle = 157.5°.

Figure 20 is shown as an example or a nonlinear curve that is corrected by the sensor. In this example, the y values contained within EEPROM fields YY = 3, 4, and 8 are positive numbers while the y values within EEPROM fields YY = 6 and 7 are negative numbers (5 is basically no correction).

The A33023 sample programmer can be used to calculate the linearization coefficients or, alternatively, a Matlab function is given in the corresponding appendix at the end of this datasheet.

Note that, in case of a short stroke (Rotation < 360°), it is recommended to calibrate with a linearization point beyond both ends of the stroke, in order to have a proper linearization at the range ends. Alternatively, if previous proposal is not possible, it is recommended in the calculation to extrapolate the measured angles at the first neighbor calibration angles. For example, if the range is [20 100°], it is recommended to program XX_linearization_0 and XX_linearization_5 in addition to XX_linearization_1 to XX_linearization_4.

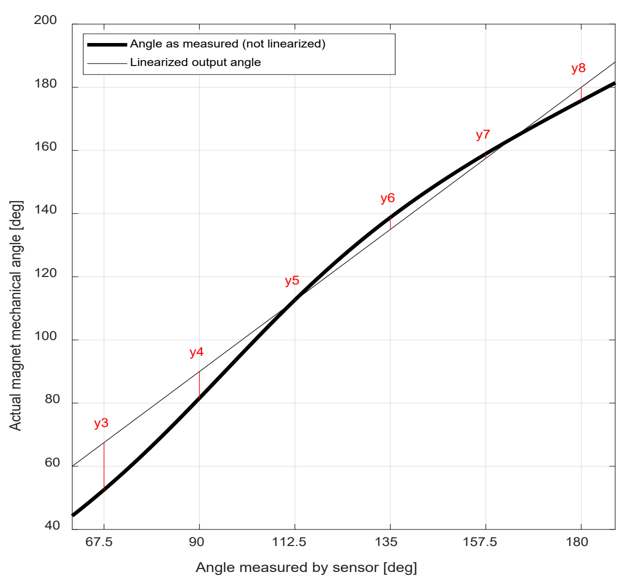

Figure 20: Schematic view of output angle linearization

Table 6: EEPROM Names and Angles

EEPROM Field XX stands for ab, bc, ca, or main	Corresponding measured angle to be corrected (deg)
XX_linearization_0	0
XX_linearization_1	22.5
XX_linearization_2	45
XX_linearization_3	67.5
XX_linearization_4	90
XX_linearization_5	112.5
XX_linearization_6	135
XX_linearization_7	157.5
XX_linearization_8	180
XX_linearization_9	202.5
XX_linearization_10	225
XX_linearization_11	247.5
XX_linearization_12	270
XX_linearization_13	292.5
XX_linearization_14	315
XX_linearization_15	337.5

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DEVICE PROGRAMMING INTERFACES

The A33023 can be programmed in two ways:

- Using the *SPI interface* for input and output
- Using a *Manchester protocol* on the PWM pin to send and receive data

The A33023 does not require special supply voltages to write to the EEPROM.

All accessible fields of the IC may be read and written using both protocols. If EEPROM locking is used, write access using either protocol may be limited.

Interface Structure

The A33023 consists of two memory blocks: direct memory (primary serial registers) and extended memory (EEPROM, shadow memory, volatile registers). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information (for example, angle data, warning flags, field strength, and temperature). All forms of communication (including the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers provide data and address location for accessing extended memory locations. Accessing these extended locations is done in an indirect fashion: the controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed and the result is again presented in the primary interface.

This concept is shown in Figure 21 below.

For writing extended locations, the primary interface registers indirect_wr_address (primary: 0x1), indirect_wr_data_msb (primary: 0x2), and indirect_wr_ data_lsb (primary 0x3) are used for writing extended memory locations. indirect_wr_address holds the address of the target extended memory location to be written. indirect_wr_data_msb and indirect_wr_data_lsb contain the two high bytes and the two low bytes for the extended location contents. The indirect_wr_status (primary: 0x4) register is used for commands and status information. Refer to the section "Read Transaction from EEPROM" for further information and other register fields associated with indirect memory transactions.

For reading extended locations, the primary interface registers indirect_rd_address (primary: 0x5), indirect_rd_data_msb (primary: 0x7), and indirect_rd_ data_lsb (primary 0x8) are used for reading extended memory locations. indirect_rd_address holds the address of the target extended memory location to be read. indirect_rd_data_msb and indirect_rd_data_lsb contain the two high bytes and the two low bytes for the extended location contents. The indirect_ rd_status (primary: 0x6) register is used for commands and status information. Refer to the section "Read Transaction from EEPROM" for further information and other register fields associated with indirect memory transactions.

For more information on EEPROM and shadow memory read and write access, see EEPROM and Shadow Memory section.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the following sections.

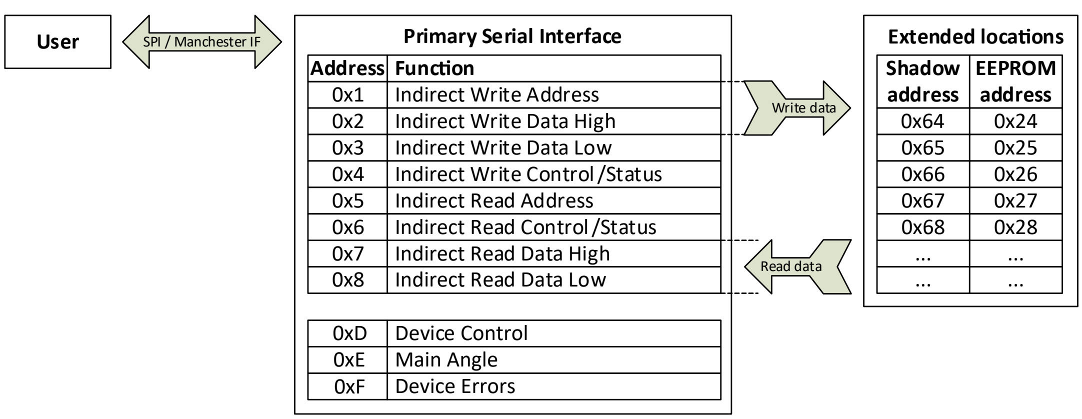

Figure 21: Serial Registers allow access to extended memory (EEPROM and Shadow) SPI

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SPI

The A33023 provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1).

The sensor responds to commands received on the MOSI (Controller-Out Peripheral-In), SCLK (Serial Clock), and $\overline{\text{CS}}$ (Chip Select) pins, and outputs data on the MISO (Controller-In Peripheral-Out) pin. All three input pins are 3.3 V SPI compatible. MISO output voltage level will conform to 3.3 V SPI levels.

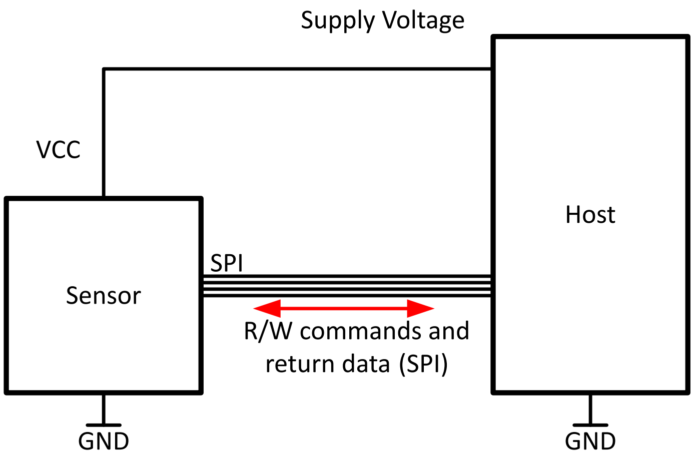

Figure 22: SPI Interface Programming Setup

TIMING

The interface timing parameters from Table 7 are displayed in Figure 23 and Figure 24 below.

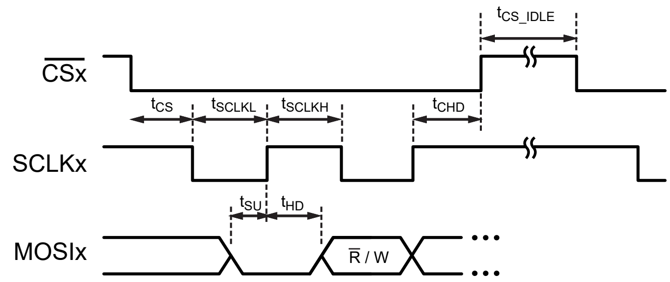

Figure 23: SPI Interface Timings Input

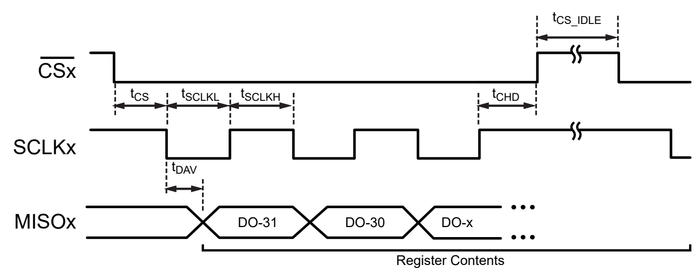

Figure 24: SPI Interface Timings Output

Table 7: SPI Interface

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC} (defines t_{SCLKL} t_{SCLKH})	40	–	60	%
SPI Frame Rate	t_{SPI}		3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{\text{CS}}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{\text{CS}}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge	–	30	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before $\overline{\text{CS}}$ rising edge	5	–	–	ns
Load Capacitance [1]	C_L	Load on Digital output pin MISO and ABI / UVW pins, with $f_{SCLCK} \leq 10$ MHz	–	–	20	pF
		Load on Digital output pin MISO and ABI / UVW pins, with $f_{SCLCK} \leq 1$ MHz	–	–	50	pF

[1] Parameter is not measured at final test. Limits based on design simulations.

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MESSAGE FRAME

The SPI interface uses a 32-bit packet and is designed to provide a high level of confidence for data for data integrity. There are three possible SPI transactions: Write Cycle, Read Request (from the controller) and Read Response (from the peripheral).

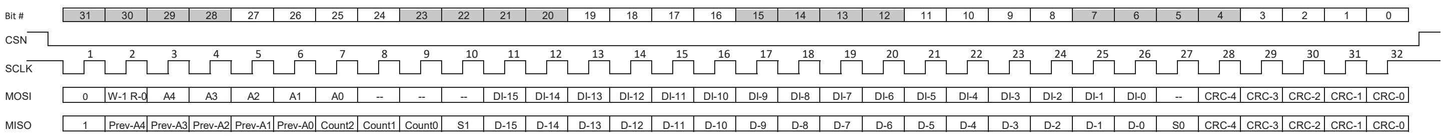

Figure 25: 32-Bit SPI Frame

Write Cycle or Read Request Cycle

The write cycle and read request frame structure is shown in Figure 26 and Figure 27. The frames consist of the following:

- Start Bit [31]: Static bit with a logic value of 0. This bit is not used in the CRC calculation.
- R/W[30]: Read/Write bit set to a logic value of 1 to signify a write cycle and 0 to signify a read request.
- Address [29:25]: Address bits for accessing primary registers.
- Data[21:6]: Data bit for writing primary registers. Considered don't care for a read request.
- CRC [4:0]: CRC bits calculated on the frame bits [30:5].
- Do not care bits [24:22, 5]: Value can be 1 or 0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	Address [4:0]					—			Data [15:0]																—	CRC [4:0]				

Figure 26: Write Cycle SPI Frame

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	Address [4:0]					—			Data [15:0] (Don't Care)																—	CRC [4:0]				

Figure 27: Read Request Cycle Frame

Read Response Cycle

The read response cycle frame, sent from the IC, as shown in Figure 28. The frame consists of the following:

- Start Bit [31]: Start bit is set to a value of 1. This bit is not used in the CRC calculation.
- Previous Address [30:26]: Register address corresponding to the read request data.
- Frame Count [25:23]: Frame counter, increments with each SPI frame.
- S1 [22]: Status/Error Flag
  - Logical OR of all unmasked error flags. Set to 1 if any unmasked error flag is asserted. Will clear once presented on the SPI bus following a read, assuming error condition has cleared.
  - ABI and SLR reported via S1.
- S0 [5]: Status/Error Flag
  - Logical OR of all unmasked error flags. Set to 1 if any unmasked error flag is asserted. Will clear once presented on the SPI bus following a read, assuming error condition has cleared.
- Data [21:6]: Data contents from primary register.
- CRC [4:0]: CRC bits calculated over the frame [30:5].

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Previous Address [4:0]					Frame Count [2:0]			S1	Data [15:0]																S0	CRC [4:0]				

Figure 28: Read Response Cycle Frame

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SPI CRC

Each SPI frame includes a 5-bit CRC, calculated using the polynomial: $x^5 + x^2 + 1$ with a seed value of 11111_2.

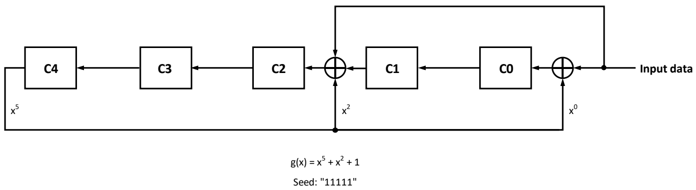

Figure 29: CRC Calculation with Left Shift Register

The outgoing CRC is calculated by the A33023 and transmitted on the MISO pin. The incoming CRC must be calculated by the Controller and included on the MOSI pin. The A33023 checks the CRC on every incoming frame, an invalid frame is ignored. The CRC achieves a hamming distance of 3 for secure data transmission.

The CRC may be calculated with the following Python code:

```python
def spi_crc(data_frame):
    """
    SPI CRC: Takes 27 bit input and generates 5 bit CRC.
    Polynomial = x^5 + x^2 + 1
    Initial CRC value set to all 1s

    Input:
        data_frame: a string representing 27 bit binary data
    """
    crc = list('11111')  #CRC seed = 11111
    # MSB of SPI frame is not used during CRC calculation.
    for j in range(1, 27):
        old_crc = crc
        aux_crc_1 = crc[1]
        aux_crc_4 = crc[4]
        crc[4] = int(old_crc[3])
        crc[3] = int(old_crc[2])
        crc[2] = int(aux_crc_1) ^ int(aux_crc_4) ^ int(data_frame[j])
        crc[1] = int(old_crc[0])
        crc[0] = int(aux_crc_4) ^ int(data_frame[j])
    #flips calculated CRC around to obtain value in proper order
    crc = crc[::-1]
    return crc
```

MISO RESPONSE ON RECEIPT OF BAD CRC

Following receipt of a bad CRC the IC will return a special SPI packet to indicate to the Controller a problem has occurred. Changes to the MISO packet are:

- Previous Address [30:26]: Set to 0x11.
- Data[21:6]: Contains the contents of the error register (primary: 0x0F).
- S0 [5]: Set to 1.

This packet is shown in Figure 30.

MISO RESPONSE FOLLOWING A WRITE

Following a write operation, the MISO packet will contain predetermined values within the Previous Address and Data Fields.

- Previous Address [30:26]: Set 0x10.
- Data [21:6]: Main Angle Value (angle_out_main from primary 0xE).

This packet is shown in Figure 31.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	1	Frame Count [2:0]			0	IER	XEE	BSY	SME	EUE	ESE	POF	OVC	UVC	MSH	MSL	SMM	OFE	SAT	TSE	VCF	0	CRC [4:0]				

Figure 30: First MISO Response Following Bad CRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	0	Frame Count [2:0]			S1	angle_out_p																S0	CRC [4:0]				

Figure 31: MISO Response Following a Write Operation

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SPI POWER ON RESPONSE

After a reset event, the S1 and S0 bits are set to 1 until the angle_rdy (primary: 0xC [0]) bit is set, and no other errors are locked in. Once the angle_rdy flag is set, the S1 and S0 bits will be asserted until a SPI read (of any location) is accomplished. The angle_rdy flag is an indication to the controller that the signal chain has stabilized, and angle is valid. In addition, transitioning S1 and S0 from a 1 to a 0 allows for the detection of a stuck diagnostic bit.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1	Address					Frame Cnt			S1	Data																S0	CRC				
Binary	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Figure 32: Initial SPI Response Frame Following Power-On

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Manchester Interface

To facilitate addressable device programming when using the unidirectional PWM, ABI, or UVW protocols, without requiring four additional SPI connections, the A33023 incorporates an additional serial communication using the PWM line.

This interface allows an external controller to read and write registers in the A33023 EEPROM and volatile memory. The point-to-point communication protocol is based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first.

The setup for communication using the Manchester interface is given in Figure 33.

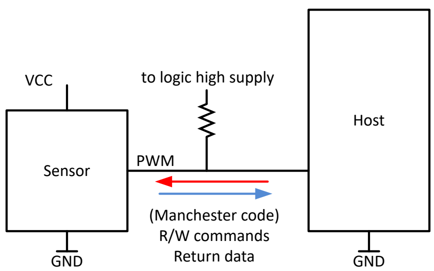

Figure 33: Manchester Programming Interface Setup

The Manchester interface allows programming and readout with a minimal number of pins involved. A valid auxiliary request command recognized by the sensor places the device into communications mode. In this mode, serial data is transmitted or received on the PWM pin. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate requested by the Master. The high and low logic level for the Manchester serial data is determined by the Manchester High and Low Voltage parameters. The PWM output consists of an open drain type circuit. A sufficient pull-up resistor and external supply voltage are required.

ENTERING MANCHESTER COMMUNICATION MODE

The A33023 continuously monitors the PWM line for a valid Auxiliary command. The Auxiliary command, shown in Figure 34, is initiated by the main controller pulling the PWM output line low for at least two PWM periods. When the controller releases the PWM line, there is a limited time window to start transmission of the Manchester Access Code (t_{msgRX}). Once a valid Access code is received, the A33023 enters programming mode, and customer EEPROM/Shadow memory may be read/written.

The communication enable, manch_comm_e, bit (extended: 0xA6 [15]) controls the state of the PWM output. When set to a logic 1, the PWM output is disabled, allowing Manchester communication on the PWM line. Setting manch_comm_e to 0 re-enables the PWM output, disabling Manchester communication.

Table 8: Auxiliary Command Parameters

Parameter	Mode	Min.	Max.	Units
t_{hold}	PWM, Auxiliary Command	2 × PWM period	–	µs
t_{gate}	–	0.7	–	µs
t_{msgRX}	–	1.4	300	µs

Table 9: Programming Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
Bit Rate	Communication rate	4	–	100	kbps
Manchester High Voltage	Data pulses on V_{OUT}	2.8	–	V_{CC}	V
Manchester Low Voltage	–	0	–	1.2	V

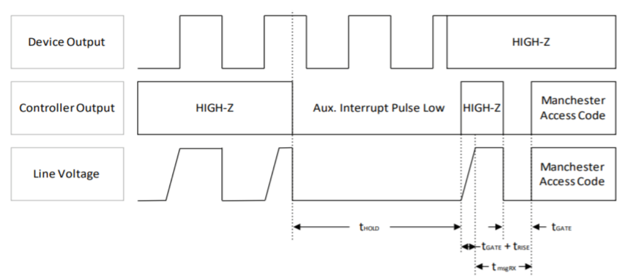

Figure 34: Auxiliary Interrupt Pulse Waveform

TRANSACTION TYPES

The A33023 receives all Manchester communication commands and responds with data on the PWM pin. Each transaction is initiated by a command from the controller; the sensor does not initiate any transactions. Two commands are recognized: Write and Read.

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Manchester Command Frame General Format

The general format of a Manchester command message frame is shown in Figure 35. Serial binary data is encoded using a Manchester encoding scheme, where a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A33023 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 10.

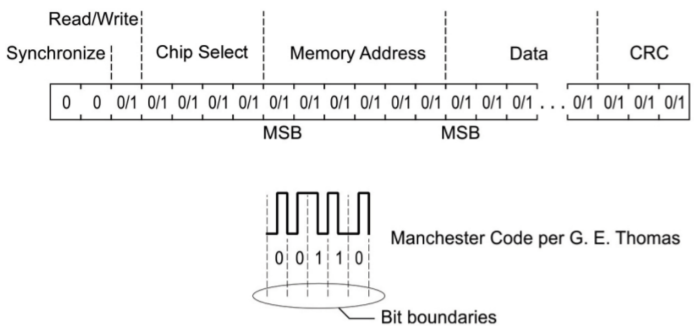

Figure 35: Manchester Message Format

Table 10: A33023 Bit Read

Quantity of Bits	Name	Values	Description
2	Synchronization	0	Used to identify the beginning of a serial interface command and communication bit time.
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
5	Address	0x-0x1F	[Read/Write] Register address (volatile memory or EEPROM)
16	Data	0/1	Only for writes: 16 bits write data. Omit for read commands.
3	CRC	0/1	Bits to check the validitiyvalidity of frame.

Manchester Communication CRC

The Manchester serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored by the check). The CRC algorithm is based on the following polynomial and the calculation is represented graphically in Figure 36. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 0b111.

$$g(x) = x^3 + x + 1$$

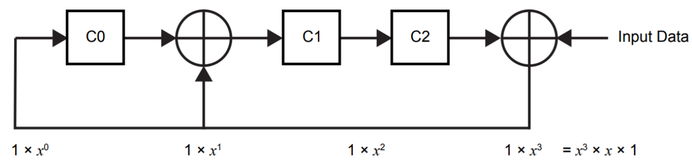

Figure 36: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the Manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
        bool C0 = false;
        bool C1 = false;
        bool C2 = false;
        bool C0p = true;
        bool C1p = true;
        bool C2p = true;
        uint64_t bitMask = 1;

        bitMask <<= numberOfBits - 1;

        // Calculate the state machine
        for (; bitMask != 0; bitMask >>= 1)
        {
                C2 = C1p;
                C0 = C2p ^ ((data & bitMask) != 0);
                C1 = C0 ^ C0p;

                C0p = C0;
                C1p = C1;
                C2p = C2;
        }

        return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```


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EEPROM AND SHADOW MEMORY USAGE

The A33023 device features include integrated EEPROM to permanently store configuration parameters for operation. EEPROM is customer programmable and retains data, or parameter values, to configure the device for the application requirements. After a reset, or EEPROM write operation, parameter data is copied from EEPROM to shadow (volatile) memory. Parameter data in shadow memory, can be overwritten by performing an extended write to the shadow addresses. Access of device parameters through shadow memory is faster than access through EEPROM. In situations where it is desired to test many parameters quickly before permanently programming, use of shadow memory is recommended. The shadow memory registers have the same format as EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Some bits do not impact device operation and are not copied into shadow memory. Shadow registers do not contain the ECC bits and may have read or write protection restrictions similar to EEPROM.

Enabling EEPROM Access

Writes to indirect memory, EEPROM, and shadow memory are restricted and require an unlock code (reading is allowed without unlocking the device). The unlock code is written to the primary serial register “access” (primary: 0x1E [15:0]). This involves two write commands, which should be executed after each other:

For SPI communication:
  Write 0xC418 to register primary 0x1E [15:0]
  Write 0x0E80 to register primary 0x1E [15:0]
For Manchester communication:
  Write 0xC418 to register primary 0x1E [15:0]
  Write 0x0E81 to register primary 0x1E [15:0]

Writing the communication enable bit, manch_comm_e (extended 0xA6 [15]) to a value of 0 or a reset event disables the communications mode.

The access status is indicated by the direct serial register access. A read of primary 0x1E [1], set to a value of 1 indicates the customer unlock code is set.

The customer unlock code is not required for write and read operations to all the direct serial registers.

Device must be unlocked when performing EEPROM margin checking.

EEPROM and Shadow Access Protections

The A33023 contains features to protect against unwanted EEPROM access.

- Setting the EEPROM parameter mem-lock (extended: 0x24 [21:18]) to a value of 0xC (1100 binary) restricts write access to prevent changes the EEPROM registers. Temporary changes to device configuration settings are still possible by writing to the indirect volatile and shadow memory. Note, any changes to the indirect volatile memory are reset after a device reset event. Read access of the EEPROM is still possible.
- Setting the EEPROM parameter mem-lock (extended: 0x24 [21:18]) to a value of 0x3 (0011 binary) restricts write access to prevent changes to EEPROM, indirect volatile, and shadow memory. Once set the parameter settings in indirect memory are read only. Read access is still possible.
- Writes to the mem-lock parameter with the above values are one time access only and are not erasable through subsequent write commands.

Write Transactions to Extended Memory: EEPROM, Shadow, and Volatile

Invoking an extended write access is a three-step process:

1. Write the target extended address to the primary register indirect_wr_address (primary: 0x1 [7:0]).
2. Write the desired data, for the target extended register, to the primary registers indirect_wr_data_msb (primary: 0x2 [15:0]) and indirect_wr_data_lsb (primary: 0x3 [15:0]). The register indirect_wr_data_lsb corresponds to the data bits [15:0] of the target extended memory address. The register indirect_wr_data_msb corresponds to the data bits [31:16] of the target extended memory address.
3. Execute the extended memory write by setting the extended memory execute write bit, exw (primary: 0x4 [15]), to a value of 1.

When the bit exw is set the 32 bits of data contained in indirect_wr_data_lsb and indirect_wr_data_lsb are written to the indirect memory address specified by indirect_wr_address. The status of the write may be interrogated by polling the primary register indirect_wr_status (primary: 0x4). The bit wip (primary: 0x4 [8]), when set, indicates write transaction in progress. The bit wdn (primary: 0x4 [0]), when set, indicates write transaction done, or complete. The error status bit xee (primary: 0x0F [14]), when set, indicates an error occurred when executing the write. For example, if a write is attempted without the proper access enabled the xee bits indicates an error.

Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the indirect_rd_address (primary: 0x5) register (using SPI or Manchester direct access). indirect_rd_address is the 8-bit extended address that determines which extended memory address will be accessed.
2. Invoke the extended access by writing the exr bit (primary: 0x6 [15] with a value of 1. The address specified in indirect_rd_address is then read, and the data is loaded into the indirect_rd_data_msb (primary: 0x7) and indirect_rd_data_lsb (primary: 0x8) registers.
3. Read the indirect_rd_data_msb and indirect_rd_data_lsb registers (using SPI or Manchester direct access) to get the full data contents of the extended read address. The register indirect_rd_data_lsb corresponds to the data bits [15:0] of the target extended memory address. The register indirect_rd_data_msb corresponds to the data bits [31:16] of the target extended memory address.

EEPROM read accesses may take up to 2 µs to complete. The rdn (primary: 0x6 [0]) bit can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the indirect_rd_data_msb and indirect_rd_data_lsb) registers if the read access is in progress (rip primary: 0x6 [8] = 1), as it could change during the serial access and the data will be inconsistent. It is also possible that an SPI CRC error will be detected if the data changes during the serial read via the SPI interface.

Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, one must address to the Shadow Extended addresses, which are located at an offset of 0x40 above the EEPROM. Refer to the EEPROM Table 11, Table 12, and Table 13 for all addresses.

EEPROM Margin Check

The A33023 contains a test mode, EEPROM Margining, to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with customer access. The EEPROM margining is selectable to check all logic 1, logic 0, or both. The results of the test are reported back in extended memory registers 0x85, 0x83, and 0x82. Note that a fail of the margin test does not force the outputs to a diagnostic state or trigger a diagnostic error flag. See section Extended Memory Table 12 addresses 0x82, 0x83, and 0x85 for more information on EEPROM margining.

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PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 11: Direct Serial Interface Registers Bits Map

Address (0x00)	Register Symbol	Access	Primary Addressed Byte (MSB)								Primary Addressed Byte (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	null_reg	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1	indirect_wr_address	RW	0	0	0	0	0	0	0	0	indirect_wr_addr							
0x2	indirect_wr_data_msb	RW	indirect_wr_data_3								indirect_wr_data_2							
0x3	indirect_wr_data_lsb	RW	indirect_wr_data_1								indirect_wr_data_0							
0x4	indirect_wr_status	WO/RO	exw	0	0	0	0	0	0	wip	0	0	0	0	0	0	0	wdn
0x5	indirect_rd_address	RW	0	0	0	0	0	0	0	0	indirect_rd_addr							
0x6	indirect_rd_status	WO/RO	exr	0	0	0	0	0	0	rip	0	0	0	0	0	0	0	rdn
0x7	indirect_rd_data_msb	RO	indirect_rd_data_3								indirect_rd_data_2							
0x8	indirect_rd_data_lsb	RO	indirect_rd_data_1								indirect_rd_data_0							
0x9	hp_a_reg	RO	hp_a															
0xA	hp_b_reg	RO	hp_b															
0xB	hp_c_reg	RO	hp_c															
0xC	status_reg	RO/RC	0	0	0	0	0	0	ecc_self_test_failed_flag		poks_self_test_failed_flag	mask_active		slr	abi	acd	rot_h	ang_rdy
0xD	ctrl	RW	0	0	0	0	0	0	0	0	0	0	0	0	full_rst	soft_rst		
0xE	main_angle	RO	angle_out_main															
0xF	error	RO/RC	ier	xee	bsy	sme	eue	ese	por	ovcc	uvcc	msh	msl	smm	ofe	sat	tse	vcf
0x10	temp12b_p	RW	0	0	0	0	temp_out_p											
0x11	temp12b_s	RW	0	0	0	0	temp_out_s											
0x12	field_reg	RO	field_mag															
0x14	angle_with_hyst	RO	abi_uvw_angle															
0x15	angle_diag_ab	RO	angle_out_ab															
0x16	angle_diag_bc	RO	angle_out_bc															
0x17	angle_diag_ca	RO	angle_out_ca															
0x18	angle_diag_latch	RO	angle_out_diag_latch															
0x1E	access	RO/WO	access_key		free_reg_lock_rd	free_reg_lock_wr	fact	fact	cust_ref_lock_rd	cust_ref_lock_wr	fact	fact	cust_ee_lock_rd	cust_ee_lock_wr	fact	fact	cust_access	factory_access
0x1F	loopback_reg	RW	loopback															

RO: Read only

WO: Write only

RW: Read and write

RC: Read and clear bit after reading

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Address 0x00 (nop) – Null Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Address 0x01 - (indirect_wr_address) Extended Write Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	indirect_wr_addr							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

indirect_wr_addr [7:0]

Target address to be used for an extended memory write. Address ranges:

0x00 - 0x3F: EEPROM (requires ≈24 ms following execution of a write)

0x40 - 0x7F: Shadow (Volatile)

0x80 – 0xAA: Miscellaneous (Volatile)

Address 0x02 (indirect_wr_data_msb) Extended Write Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	indirect_wr_data_3								indirect_wr_data_2							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

indirect_wr_data_3 [15:8]

Upper forth byte of data for an extended write operation, corresponds to bit [31:24] of the extended write address.

indirect_wr_data_2 [7:0]

Third byte of data for an extended write operation, corresponds to bit [23:16] of the extended write address.

Address 0x03 (indirect_wr_data_lsb) Extended Write Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	indirect_wr_data_1								indirect_wr_data_0							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

indirect_wr_data_1 [15:8]

Second byte of data for an extended write operation, corresponds to bit [15:8] of the extended write address.

indirect_wr_data_0 [7:0]

Lower first byte of data for an extended write operation, corresponds to bit [7:0] of the extended write address.

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Address 0x04 (indirect_wr_status) Extended Write Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXW [15]
Initial extended write by writing 1. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP [8]
Indicates write in progress when set to 1.

WDN [0]
Write operation complete when to a value of 1, clears when EXW is set to 1.

Address 0x05 (indirect_rd_address) Extended Read Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	indirect_rd_addr							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

indirect_rd_addr [7:0]
Address to be used for an extended read. Address ranges:

0x00 – 0x3F: EEPROM (requires ≈ 2µs)

0x40 – 0x7F: Shadow (Volatile)

0x80 – 0xAA: Miscellaneous (Volatile)

Address 0x06 (indirect_rd_status) Extended Read Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXR [15]
Initial extended read by writing 1. Sets RIP, clears RDN. Write-only, always reads back ‘0’.

RIP [8]
Indicates read in progress when set to 1.

RDN [0]
Read operation complete when to a value of 1, clears when EXR is set to 1.

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Address 0x07 (indirect_rd_data_msb) Extended Read Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	indirect_rd_data_3								indirect_rd_data_2							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

indirect_rd_data_3 [15:8]
Upper fourth byte of data for an extended read operation, corresponds to bit [31:24] of the extended read address after execution of a read operation.

indirect_rd_data_2 [7:0]
Third byte of data for an extended read operation, corresponds to bit [23:16] of the extended read address after execution of a read operation.

Address 0x08 (indirect_rd_data_lsb) Extended Read Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	indirect_rd_data_1								indirect_rd_data_0							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

indirect_rd_data_1 [15:8]
Second byte of data for an extended read operation, corresponds to bit [15:8] of the extended read address after execution of a read operation.

indirect_rd_data_0 [7:0]
Lower first byte of data for an extended read operation, corresponds to bit [7:0] of the extended read address after execution of a read operation.

Address 0x09 (hp_a_reg) Channel A Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hp_a															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

hp_a [15:0]
Channel A CH_A = HP1-HP4 reading. Value is a 16-bit signed integer.

The LSB read value is converted to gauss with $CH_A(G) = CH_A(LSB)/S$, with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600. The returned gauss value is indicative only.

Address 0x0A (hp_b_reg) Channel B Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hp_b															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

hp_b [15:0]
Channel B CH_B = HP2-HP5 reading. Value is a 16-bit signed integer.

The LSB read value is converted to gauss with $CH_B(G)= CH_B(LSB)/S$, with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600. The returned gauss value is indicative only.

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Address 0x0B (hp_c_reg) Channel C Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hp_c															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

hp_c [15:0]

Channel C CH_C = HP3-HP6 reading. Value is a 16-bit signed integer.

The LSB read value is converted to gauss with CH_C(G)= CH_C(LSB)/S, with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600. The returned gauss value is indicative only.

Address 0x0C (status_reg) Device Status Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	ecc_self_test_failed_flag		poks_self_test_failed_flag	mask_active		slr	abi	acd	rot_h	ang_rdy
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RC	RC	RC	RO	RO

ecc_self_test_failed_flag [9]

Indicates ECC (Error Corrector Code) self-test failed. ECC self-test checks the ECC mechanism of the EEPROM memory system.

poks_self_test_failed_flag [7]

Indicates POK/IOKs (Power OK / Current OK) self-test failed.

mask_active [6]

Indicates that at least one fault masking bit is active.

slr [4]

ABI slew rate warning. An abi warning pulse is emitted every time the slew rate is used to track the angle.

abi [3]

It reflects an ABI integrity error (only if abi_slew_rate=0). An abi error pulse is emitted every time the angle cannot be tracked.

acd [2]

ABI count-up done. If no slew rate limit is provided (slew_rate = 0), the count-up feature is disabled. The ABI output will increment, from 0, following power-up. To reduce the time needed for the counting-up process, the ABI will increment in either CW or CCW direction, whichever is shortest, towards the current angle position. For example, if the current angle position is 270 degrees, the ABI will increment in the CW direction (effectively counting down from 360 degrees) towards this value. When this process is done this flag is set. If EEPROM bit abi_sr_dly_en is set, ABI count-up done will be disabled although slew_rate limit is provided. Note that the count-up feature occurs at start-up or after a fault clear.

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rot_h [1]

Current rotation direction value. It reflects a magnet rotation direction calculated in main path: it will depend on the rot_dir_p (extended: 0x3E [0]) configuration bit (0 is counterclockwise).

rot_h calculation is enabled according to the table below:

abi_uvw_enable	interpolator_bypass	rot_h calculation
0	0	No (default value is 0)
0	1	Yes
1	0	Yes
1	1	Yes

ang_rdy [0]

Angle ready informational flag: this flag is set when the first angle calculated in the main, ab, bc, and ca paths are ready.

Address 0x0D (ctrl) Control register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	full_ rst	soft_ rst		
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

full_rst [3]

Full Reset. Writing at value of one to this bit triggers a full reset of the device logic, including a full load of the EEPROM, reset of all the status and error registers, reset of the signal processing, reset of the outputs and communication protocols, and a reset of the main controller. This function includes all functions performed in a soft_rst. After the reset is complete the POR flag (primary: 0xF [9]) is asserted.

soft_rst [2]

Soft Reset. Writing at value of one to this bit triggers a full reset of the device logic, reset of all the status and error registers, reset of the signal processing, and reset of the outputs and communication protocols. After the reset is complete the POR flag (primary: 0xF [9]) is asserted.

Address 0x0E (main_angle) Main Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	angle_out_main															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

angle_out_main [15:0]

Register indicates the calculated angle from the three differential channels δ_{MAIN}. The parameter is a 16-bit unsigned integer with value of angle_out_main × $360/2^{16}$ in degrees. A read of this register latches the data in angle_out_diag_latch (primary: 0x18 [15:0]), turns_count_latch_p (primary: 0x19 [10:0]), turns_count_latch_s (primary: 0x1B [10:0]).

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Address 0x0F (error) Device Error Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ier	xee	bsy	sme	eue	ese	por	ovcc	uvcc	msh	msl	smm	ofe	sat	tse	vcf
Access	RC	RC	RC	RO	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC

ier [15]

Interface error. Invalid SPI packet detected. Packet was discarded. Also indicates an error in the Manchester communication.

Value	Description
0	No interface error
1	Interface error

xee [14]

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute error

bsy [13]

Extended access overflow.

An extended write or extended read was initiated before previous operation is complete.

Value	Description
0	No extended access error
1	Extended access error

sme [12]

Shadow memory error. Indicates detection of a MISR (multiple input signature request) error in the shadow memory. This error requires a reset to clear.

Value	Description
0	No Shadow memory error
1	Shadow memory error

eue [11]

EEPROM uncorrectable error. A multi-bit EEPROM read error occurred. EEPROM bit errors are only checked on EEPROM load (i.e., power-on or reset). This error requires a reset to clear and the condition no-longer persists.

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

ese [10]

EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset). Single-bit errors are detected and corrected in shadow memory by hamming ECC.

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error

por [9]

Reset condition. Indicates a reset event has occurred or a EEPROM load has occurred.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are re-initialized

ovcc [8]

VCC Overvoltage condition. Indicates an overvoltage condition on the supply pin VCC. Will continue to assert until fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Overvoltage error
1	VCC Overvoltage error

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uvcc [7]

VCC Undervoltage condition. Indicates an undervoltage condition on the supply pin VCC. Will continue to assert until fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Undervoltage error
1	VCC Undervoltage error

msh [6]

Magnetic signal high fault. Indicates the magnitude of the magnetic input signal sensed is above the high limit threshold. The high limit threshold is set via EEPROM parameter msh_thr (extended: 0x24 [2:0]).

The msh_thr is compared to field_mag (primary: 0x12 [15:0]).

Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field high fault
1	Magnetic field above the high threshold, msh_thr

msl [5]

Magnetic signal low fault. Indicates the magnitude of the magnetic input signal sensed is below the low limit threshold. The low limit threshold is set via EEPROM parameter msl_thr (extended: 0x24 [5:3]).

The msl_thr is compared to field_mag (primary: 0x12 [15:0]).

Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field low fault
1	Magnetic field below the low threshold msl_thr

smm [4]

Signal mismatch error. Indicates a mismatch between angle_out_main δ_{MAIN} and any of the diagnostic angles (angle_out_ab δ_{AB} or angle_out_bc δ_{BC} or angle_out_ca δ_{CA}). The angle mismatch threshold is set via EEPROM parameter angle_mismatch (extended 0x24 [7:6]).

An error detected by this monitor will continue to assert until the fault condition is removed (and the register is cleared).

smm also reports a BIST error. An error detected by this monitor requires a reset to clear.

Value	Description
0	No angle mismatch or error register BIST failure detected
1	Angle mismatch or error register BIST failure detected

ofe [3]

Oscillator frequency error. One of the oscillator watchdog circuits, monitoring the high frequency and low frequency oscillators has detected a fault. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No oscillator error
1	Oscillator watchdog error

sat [2]

Channel saturation flag. Indicates internal signal have saturated, including the inputs of the ADCs, prior to the angle calculation. May indicate the magnetic input is outside of the specified range. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No saturation detected in the signal path
1	Saturation conditions detected within the channel signal path

tse [1]

Temperature sensor error. The primary or secondary temperature sensor calculated output is below –60°C or above 170°C. Also reports when the calculated temperature output of the primary and secondary temperature sensors differs by more than 20°C. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	Primary and secondary temperature sensors within range
1	Primary or secondary temperature sensor calculated output below -60°C or above 170°C or the primary temperature sensor calculated output differs more than 20°C when compared to the secondary temperature sensor calculated output.

vcf [0]

Voltage check fault. Indicates a failure of an internal reference voltage. Will continue to assert until the fault condition is removed (and the register is cleared).

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Address 0x10 (temp12b_p) Primary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	temp_out_p											
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

temp_out_p [11:0]
Current ambient temperature from the primary channel internal temperature sensor. Value is a 12-bit signed integer, where: temperature [°C] ≈ (temp_out_p / 8) + 25.

Address 0x11(temp12b_s) Secondary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	temp_out_s											
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

temp_out_s [11:0]
Current ambient temperature from the secondary channel internal temperature sensor. Value is a 12-bit signed integer, where: temperature [°C] ≈ (temp_out_p / 8) + 25.

Address 0x12 (field_reg) field_mag

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	field_mag															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

field_mag [15:0]
Indicates the amplitude of the input magnetic flux density B_{IN}. Value is a 16-bit unsigned integer.

The LSB read value is converted to gauss with B_{IN}(G)= field_mag(LSB / (S × 1.304 × 3), with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600. The returned gauss value is indicative only.

Address 0x14 (angle_with_hyst) Hysteresis Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	abi_uvw_angle															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

abi_uvw_angle [15:0]
Angle output from main channel, after hysteresis processing. The hysteresis configuration is set using the parameter angle_hyst (extended: 0x25 [22:20]).

The parameter is a 16-bit unsigned integer with value of abi_uvw_angle × 360 / 2^{16} in degrees.

Address 0x15 (angle_diag_ab) Diagnostic AB Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	angle_out_ab															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

angle_out_ab [15:0]
Angle output from channel AB δ_{AB}.

The parameter is a 16-bit unsigned integer with value of angle_out_ab × 360 / 2^{16} in degrees.

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Address 0x16 (angle_diag_bc) Diagnostic BC Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	angle_out_bc															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

angle_out_bc [15:0]
Angle output from channel BC δ_{BC}.

The parameter is a 16-bit unsigned integer with value of angle_out_bc × 360 / 2^{16} in degrees.

Address 0x17 (angle_diag_ca) Diagnostic CA Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	angle_out_ca															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

angle_out_ca [15:0]
Angle output from channel CA δ_{CA}.

The parameter is a 16-bit unsigned integer with value of angle_out_ca × 360 / 2^{16} in degrees.

Address 0x18 (angle_diag_latch) Latched Main Angle (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	angle_out_diag_latch															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

angle_out_diag_latch [15:0]
Latched angle output from the selected redundant channel (AB, BC or CA).

Selectable channel with diag_channel_sel (Extended 0x3F [19:18]).

The parameter is a 16-bit unsigned integer with value of angle_out_diag_latch × 360 / 2^{16} in degrees.

Address 0x1E (access) Access Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	access_key						customer_ register_lock		factory		customer_ eeprom_lock		factory_ eeprom_lock		customer_ access	factory_ access
Access	WO	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Access_key [15:0]
Writing to register 0x1E is special command to enable access to the extended memory space, EEPROM and Volatile. See section Enabling EEPROM Access for more information.

customer_access [1]
Bit indicates access to customer registers within the extended memory space. A logic value of one indicates access to the customer registers within the extended memory space is enabled.

factory_access [1]
Bit indicates access to factory registers within the extended memory space. A logic value of one indicates access to the factory registers within the extended memory space is enabled.

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Address 0x1F (loopback_reg) Loopback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	loopback															
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

loopback [15:0]

Customer loopback register. The registers allow the external controller to perform a loopback test of the SPI communication between the master and the slave A33023.

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EXTENDED MEMORY TABLE:

EEPROM (NONVOLATILE), SHADOW (VOLATILE), AND MISCELLANEOUS (VOLATILE)

The EEPROM/Shadow register bitmap is shown below. All EEPROM and shadow contents can be read by the user, without unlocking. Writing required device unlock. The shadow memory is a copy of the EEPROM in the address range 0x40 to 0x7F.

Table 12: EEPROM/Shadow Memory Map

EEPROM Address	Bits																										
	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ECC	factory reserved				factory_die_id																factory reserved					
0x01	ECC	factory reserved				factory_lot																factory_wafer					
0x02	ECC	cas_id																factory reserved									
0x03	ECC	customer_id																									
0x04 to 0x23	factory reserved																										
0x24	ECC					mem_lock					block_volatile_output	make_errors_high_z	mask_4	mask_3	mask_2	mask_1	mask_0			angle_mismatch		msl_thr			msh_thr		
0x25	ECC			interpolator_bypass	angle_hyst			abi_err_rpt_mode		abi_sr_dly_en	abi_count_up_rpt_en	abi_uvw_enable	interpolator_rate	abi_index_mode		abi_slew_rate						abi_uvw_resolution				abi_uvw_invert_out_en	abi_0_uvw_1
0x26	ECC			ab_linearization_2								ab_linearization_1								ab_linearization_0							
0x27	ECC			ab_linearization_5								ab_linearization_4								ab_linearization_3							
0x28	ECC			ab_linearization_8								ab_linearization_7								ab_linearization_6							
0x29	ECC			ab_linearization_11								ab_linearization_10								ab_linearization_9							
0x2A	ECC			ab_linearization_14								ab_linearization_13								ab_linearization_12							
0x2B	ECC						ab_lin_en	cust_angle_offset												ab_linearization_15							
0x2C	ECC			bc_linearization_2								bc_linearization_1								bc_linearization_0							
0x2D	ECC			bc_linearization_5								bc_linearization_4								bc_linearization_3							
0x2E	ECC			bc_linearization_8								bc_linearization_7								bc_linearization_6							
0x2F	ECC			bc_linearization_11								bc_linearization_10								bc_linearization_9							
0x30	ECC			bc_linearization_14								bc_linearization_13								bc_linearization_12							
0x31	ECC																		bc_lin_en	bc_linearization_15							
0x32	ECC			ca_linearization_2								ca_linearization_1								ca_linearization_0							
0x33	ECC			ca_linearization_5								ca_linearization_4								ca_linearization_3							
0x34	ECC			ca_linearization_8								ca_linearization_7								ca_linearization_6							
0x35	ECC			ca_linearization_11								ca_linearization_10								ca_linearization_9							
0x36	ECC			ca_linearization_14								ca_linearization_13								ca_linearization_12							
0x37	ECC																		ca_lin_en	ca_linearization_15							
0x38	ECC			main_linearization_2								main_linearization_1								main_linearization_0							
0x39	ECC			main_linearization_5								main_linearization_4								main_linearization_3							
0x3A	ECC			main_linearization_8								main_linearization_7								main_linearization_6							
0x3B	ECC			main_linearization_11								main_linearization_10								main_linearization_9							
0x3C	ECC			main_linearization_14								main_linearization_13								main_linearization_12							
0x3D	ECC																		main_lin_en	main_linearization_15							
0x3E	ECC																				tc_hyst_dis_p	iir_bw_sel		spare_cust			rot_dir_p
0x3F	ECC							diag_channel_sel		pwm_enable	pwm_slw_sel			pwm_porch_sel			pwm_period				tc_hyst_dis_s						rot_dir_s

Note: All EEPROM grey registers are customer Read/Write registers. They have no equivalent in Shadow memory.

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Table 13: Volatile Memory Map

EEPROM Address	Bits 31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x80	Read only. Factory reserved																										
0x81	Read only. Factory reserved																										
0x82							ee_dbe_flag	ee_sbe_flag	ee_ecc						ee_addr						ee_err_status					cp_err	ee_err
0x83		ee_data																									
0x84	Read only. Factory reserved																										
0x85														ee_loop	ee_test_addr						ee_use_test_addr	margin_min_max_fail	margin_status		margin_no_min	margin_no_max	margin_start
0x86	Read only. Factory reserved																										
0x87																							ecc_test_dbe_flag	ecc_test_sbe_flag	ecc_test_status		ecc_test_start
0x88 to 0xA5	Read only. Factory reserved																										
0xA6												manch_comm_e	Reserved														
0xA7 to 0xA9	Read only. Factory reserved																										
0xAA																									lp_comp_test_start	poks_test_running	poks_test_start
0xAB to 0xFF	Unused																										

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EEPROM

Address 0x0

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				factory_die_id																factory reserved					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

factory_id [21:6]

Identification number. When used in combination with factory_lot and factory_wafer create a unique identification for device traceability. The register access is customer read only.

Address 0x1

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				factory_lot																factory_wafer					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

factory_lot [21:6]

Identification number. When used in combination with factory_id and factory_wafer create a unique identification for device traceability. The register access is customer read only.

factory_wafer [5:0]

Identification number. When used in combination with factory_id and factory_lot create a unique identification for device traceability. The register access is customer read only.

Address 0x2

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cas_id																factory reserved									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

cas_id [25:10]

Type identification number. May contain an identification number to distinguish a specific device configuration. For example, the cas_id may be used to distinguish between various device types. The register access is customer read only.

Address 0x3

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	customer_id																									
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

customer_id [25:0]

Customer identification number. The register space is open for customer write access. The contents of the register have no effect on the device operating modes. A common use for the register is to store a unique identification number written by the customer. The register access is customer read and write.

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Address 0x24

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					mem_lock					block_volatile_output	make_errors_high_z	mask_4	mask_3	mask_2	mask_1	mask_0			angle_mismatch		msl_thr			msh_thr		
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

mem_lock [21:18]

Extended memory access lock, EEPROM, Shadow, and Miscellaneous Volatile memory lock. Setting this parameter is permanent and may not be undone.

Value	Description
1100	Writing to EEPROM is locked
0011	Writing to EEPROM and Shadow memory is locked

block_volatile_output [16]

Prevents bits within the volatile memory space, 0x80 through 0xAA, that may impact the output from operating.

Value	Description
0	Volatile bits allowed to function normally
1	Prevents operation of volatile bits, 0x80 through 0xAA, that may impact the output

make_errors_high_z [15]

Option for the PWM to stay in a high-impedance state when an errors flag is set.

Value	Description
0	PWM outputs at ½ frequency and a fixed duty cycle in response to an error flag
1	PWM output goes to a high impedance state in response to an error flag.

mask_4 [14]

Bit to mask error flags reporting on the PWM, ABI and S0/S1 SPI bits. Setting this bit to a logic value of one masks the abi (Primary: 0xC [3]) or slr (Primary: 0xC [4]) error flags.

mask_3 [13]

Bit to mask error flags reporting on the PWM, ABI and S0/S1 SPI bits. Setting this bit to a logic value of one masks the smm (Primary: 0xF [4]) error flag.

mask_2 [12]

Bit to mask error flags reporting on the PWM, ABI and S0/S1 SPI bits. Setting this bit to a logic value of one masks the sat (Primary: 0xF [2]) error flag.

mask_1 [11]

Bit to mask error flags reporting on the PWM, ABI and S0/S1 SPI bits. Setting this bit to a logic value of one masks the tse (Primary: 0xF [1]) error flag.

mask_0 [10]

Bit to mask error flags reporting on the PWM, ABI and S0/S1 SPI bits. Setting this bit to a logic value of one masks the vcf (Primary: 0xF [0]), uvcc (Primary: 0xF [7]), ovcc (Primary: 0xF [8]) and ofe (Primary: 0xF [3]) error flags.

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angle_mismatch [7:6]
Angle mismatch. Sets the threshold for the allowable mismatch between the main and redundant angle outputs. If the main and redundant angle outputs differ more than the threshold the smm flag is set.

Value	Description: Signal path mismatch threshold in degrees
0	3
1	5
2	8
3	12

msl_thr [5:3]
Magnetic Threshold low value. Sets the low threshold of the input magnetic flux density B_{IN}.

If field_mag is below the threshold the msl flag will be set. When msl_thr is set to a value of 0 the low threshold is disabled.

Reminder: field_mag LSB read value is converted to gauss with $B_{IN}(G)$ = field_mag(LSB) / (S × 1.304 × 3), with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600.

For example, if one wants to report a low input magnetic field at 100 G, the corresponding field_mag value is 8998 LSB with part variant 300. The corresponding code would be msl_thr = 1.

Value	Percentage of field_mag register	Description: Corresponding digital value of field_mag register
0	No threshold	0
1	15	9830
2	20	13107
3	30	19661
4	35	22938
5	40	26214
6	45	29491
7	50	32768

msh_thr [5:3]
Magnetic Threshold high value. Sets the high threshold of the input magnetic flux density B_{IN}.

If field_mag is above the threshold the msh flag will be set. When msh_thr is set to a value of 0 the high threshold is disabled.

Reminder: field_mag LSB read value is converted to gauss with $B_{IN}(G)$ = field_mag(LSB) / (S × 1.304 × 3), with S = 23 LSB/G for part variant 300 and S = 15.5 LSB/G for part variant 600.

For example, if one wants to report a high input magnetic field at 400 G, the corresponding field_mag value is 35990 LSB with part variant 300. The corresponding code would be msl_thr = 4.

Value	Percentage of field_mag register	Description: Corresponding digital value of field_mag register
0	No threshold	65535
1	80	52429
2	70	45875
3	60	39322
4	55	36045
5	50	32768
6	45	29491
7	40	26214

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Address 0x25

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			interpolator_ bypass	angle_hyst			abi_ err_ rpt_ mode		abi_ sr_ dly_ en	abi_ count_ up_ rpt_ en	abi_ uvw_ enable	interpolator_ rate	abi_ index_ mode		abi_slew_rate						abi_ uvw_ resolution				abi_ uvw_ invert_ out_ en	abi_ 0_ uvw_ 1
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

interpolator_bypass [23]

Interpolator bypass. See interpolator_rate for more information.

angle_hyst [22:20]

Angle ABI hysteresis. Angle Hysteresis threshold applied to the angle for ABI calculation. Value is 16-bit resolution. Provides ≈0.01 to 1.41° of hysteresis.

$$\text{hysteresis} = 360 \times 2^{(-16)} \times 2^{(\text{angle\_hyst}+1)}$$

Value	Description
0	0.01° of hysteresis
1	0.02° of hysteresis
2	0.04° of hysteresis
3	0.09° of hysteresis
4	0.18° of hysteresis
5	0.35° of hysteresis
6	0.70° of hysteresis
7	1.41° of hysteresis

abi_err_rpt_mode [19:18]

ABI error flag report mode.

ABI fault report strongly depends on PWM report logic.

If PWM is enabled (pwm_enable = 1 (Extended: 0x3F [17])), errors can be reported through ABI using two different methods: in-phase or high-z depending on abi_err_rpt_mode. If only A and B are monitored, in-phase method must be used. If A, B and I are monitored, either method can be used.

With in-phase report method, A and B outputs are in phase and I is high impedance if an error occurs. In this case, A and B mirror the PWM: PWM frequency is divided by two and the error is reported with a specific duty cycle (see the Safety Section at the end of this document or the Safety Manual).

With high-z report method, A, B and I are set to high impedance if an error occurs.

All faults are reported through the ABI pins.

If PWM is disabled (pwm_enable = 0 (Extended: 0x3F [17])) and in-phase report method is selected, when an error occurs after the first frame, A and B outputs are in phase and behaves as a PWM output: frequency is given by pwm_period (Extended 0x3F [10:7]) and the duty cycle represents the actual main measured angle. The first frame after start-up reports error with the right duty cycle value (see the Safety Section at the end of this document or the Safety Manual).

Note that, in any case, no faults are reported through UVW.

Value	Description
0	ABI high-z report mode
1	ABI in-phase report mode
2	Disabled
3	Same as 1

abi_sr_dly_en [17]

ABI Slew Rate Delay Enable. Setting this bit to a logic value of one enables the ABI Slew Rate at start-up and after a fault delayed, to avoid unwanted transitions if the initial angle is not zero. Recommended when abi_err_rpt_mode = 0 or 1, and the absolute angle is taken from PWM output.

abi_count_up_rpt_en [16]

ABI count up feature report enable. When set to a logic value of one, the PWM outputs a special frame to signal when the count up feature is complete. When set to a logic value of zero, the acd error flag is disabled.

Note: the count up feature is disable when abi_slew_rate (extended: 0x25 [11:6]) is set to a value of zero.

Note: ABI conducts the count-up procedure when returning from an error state. Only occurs when ABI error report mode is set to high-z.

abi_uvw_enable [15]

ABI or UVW output enable. Setting this bit to a logic value of one enables the ABI or UVW outputs.

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interpolator_rate [14]

Interpolator rate. Angle output of linearization blocks (both from main and redundant paths) are driven to the interpolator block. This block takes the angle selected to be outputted through ABI/UVW protocol and applies a 2nd order interpolator to get an upsampled angle signal with configurable rate. The interpolator rate applies when interpolator_bypass is set to a logic value of zero.

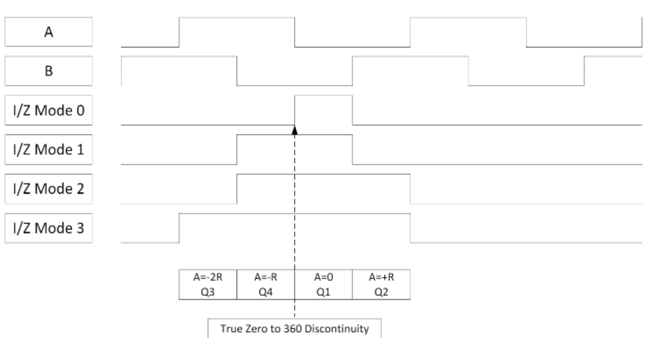
interpolator_rate value	interpolator_bypass value	ABI angle output rate (µs)
0	1	2
1	0	0.5
0	0	0.25

abi_index_mode [13:12]

Defines the width and placement of the "I" pulse in ABI.

Value	Description
0	"I" pulse is set only at 0° to +R
1	"I" pulse is set only at -R to +R
2	"I" pulse is set only at -R to +2R
3	"I" pulse is set only -2R to +2R

"R" indicates the ABI quadrature resolution.



abi_slew_rate [11:6]

ABI slew time rate. "0" disables slew limiting.

Minimum edged-to-edge time for ABI output is defined by:

$$(N+1) \times 125\ ns$$

where "N" is the value of abi_slew_rate.

This limits the maximum ABI velocity. Reducing the ABI resolution can be used to counteract this.

Value	Description
0	Slew limiting disable
1	250 ns of slew control
…	…
63	8 µs of slew control

abi_uvw_resolution [5:2]

Defines resolution of ABI/UVW outputs.

In ABI mode, cycle resolution = $2^{(14-n)}$ where "n" is the abi_uvw_resolution value.

In UVW mode, the number of pole pairs is n + 1.

Value	Cycles per revolution (A or B)	UVW pole pairs
0	2^{14} = 16384	1
1	2^{13} = 8192	2
2	2^{12} = 4096	3
3	2^{11} = 2048	4
…	…	…
14	2^{0} = 1	15
15	N/A	16

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abi_uvw_invert_out_en [1]
Invert ABI/UVW signals.

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>ABI/UVW signals behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at ABI resolution</td></tr>
<tr><td><table><tr><th>State name</th><th>A</th><th>B</th></tr><tr><td>Q1</td><td>0</td><td>0</td></tr><tr><td>Q2</td><td>0</td><td>1</td></tr><tr><td>Q3</td><td>1</td><td>1</td></tr><tr><td>Q4</td><td>1</td><td>0</td></tr></table></td></tr>
<tr><td rowspan="2">1</td><td>ABI/UVW signals are inverted and behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at ABI resolution</td></tr>
<tr><td><table><tr><th>State name</th><th>A</th><th>B</th></tr><tr><td>Q1</td><td>1</td><td>1</td></tr><tr><td>Q2</td><td>1</td><td>0</td></tr><tr><td>Q3</td><td>0</td><td>0</td></tr><tr><td>Q4</td><td>0</td><td>1</td></tr></table></td></tr>
</table>

abi_0_uvw_1 [0]
Defines behavior of the ABI/UVW pins.

Value	Description
0	ABI output mode is selected
1	UVW output mode is selected

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Address 0x26

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ab_linearization_2								ab_linearization_1								ab_linearization_0							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_linearization_2 [23:16]

ab channel linearization table entry 2. Corresponds to the angle correction added to a measured value of 45° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_1 [15:8]

ab channel linearization table entry 1. Corresponds to the angle correction added to a measured value of 22.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_0 [7:0]

ab channel linearization table entry 0. Corresponds to the angle correction added to a measured value of 0° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x27

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ab_linearization_5								ab_linearization_4								ab_linearization_3							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_linearization_5 [23:16]

ab channel linearization table entry 5. Corresponds to the angle correction added to a measured value of 112.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_4 [15:8]

ab channel linearization table entry 4. Corresponds to the angle correction added to a measured value of 90° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_3 [7:0]

ab channel linearization table entry 3. Corresponds to the angle correction added to a measured value of 67.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x28

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ab_linearization_8								ab_linearization_7								ab_linearization_6							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_linearization_8 [23:16]
ab channel linearization table entry 8. Corresponds to the angle correction added to a measured value of 180° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_7 [15:8]
ab channel linearization table entry 7. Corresponds to the angle correction added to a measured value of 157.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_6 [7:0]
ab channel linearization table entry 6. Corresponds to the angle correction added to a measured value of 135° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x29

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ab_linearization_11								ab_linearization_10								ab_linearization_9							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_linearization_11 [23:16]
ab channel linearization table entry 11. Corresponds to the angle correction added to a measured value of 247.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_10 [15:8]
ab channel linearization table entry 10. Corresponds to the angle correction added to a measured value of 225° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_9 [7:0]
ab channel linearization table entry 9. Corresponds to the angle correction added to a measured value of 202.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x2A

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ab_linearization_14								ab_linearization_13								ab_linearization_12							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_linearization_14 [23:16]

ab channel linearization table entry 14. Corresponds to the angle correction added to a measured value of 315° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_13 [15:8]

ab channel linearization table entry 13. Corresponds to the angle correction added to a measured value of 292.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

ab_linearization_12 [7:0]

ab channel linearization table entry 12. Corresponds to the angle correction added to a measured value of 270° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x2B

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ab_lin_en	cust_angle_offset												ab_linearization_15							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ab_lin_en [20]

Set to “1” to enable the redundant channel ab linearization.

Value	Description
0	Disable ab channel linearization
1	Enable ab channel linearization

cust_angle_offset [19:8]

Customer angle offset. Fixed angle offset added to the raw calculated angle.

12-bit unsigned ranging from 0 to 359.9121° with a 0.0879° step size.

ab_linearization_15 [7:0]

ab channel linearization table entry 15. Corresponds to the angle correction added to a measured value of 337.5° by the channel ab.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x2C to address 0x30

Contains the same as 0x26 to 0x2A but for the redundant channel bc.

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Address 0x31

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																		bc_lin_en	bc_linearization_15							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

bc_lin_en [8]

Set to 1 to enable the redundant channel bc linearization.

Value	Description
0	Disable bc channel linearization
1	Enable bc channel linearization

bc_linearization_15 [7:0]

bc channel linearization table entry 15. Corresponds to the angle correction added to a measured value of 337.5° by the channel bc.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x32 to address 0x36

Contains the same as 0x26 to 0x2A but for the redundant channel ca.

Address 0x37

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																		ca_lin_en	ca_linearization_15							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ca_lin_en [8]

Set to 1 to enable the redundant channel ca linearization.

Value	Description
0	Disable ca channel linearization
1	Enable ca channel linearization

ca_linearization_15 [7:0]

ca channel linearization table entry 15. Corresponds to the angle correction added to a measured value of 337.5° by the channel ca.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

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Address 0x38 to address 0x3C

Contains the same as 0x26 to 0x2A but for the main channel.

Address 0x3D

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																		main_lin_en	main_linearization_15							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

main_lin_en [8]

Set to 1 to enable the main channel linearization.

Value	Description
0	Disable main channel linearization
1	Enable main channel linearization

main_linearization_15 [7:0]

main channel linearization table entry 15. Corresponds to the angle correction added to a measured value of 337.5 degrees by the channel main.

8-bit signed coefficient able to compensate for ±11.25° of error, with 0.088° step size.

Address 0x3E

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																				tc_hyst_dis_p	iir_bw_sel		spare_cust			rot_dir_p
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

tc_hyst_dis_p [6]

Disables primary channel turns count hysteresis. A hysteresis of approximately 11.25 degrees applies to the angle for the turns count calculation. There is a ±5.625° area on the turns count boundaries (90, 180, 270, 360 degrees) where the turns count is not updated.

Value	Description
0	Hysteresis applied to primary channel turns count
1	No hysteresis applied to primary channel turns count

iir_bw_sel [5:4]

Differential channel filter bandwidth. Primary effect is on response time.

Value	Bandwidth [kHz]	Typical response time [µs]
0	6.25	45
1	12.5	25
2	25	20
3	50	15

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spare_cust [3:2]

Spare customer bits. Spare EEPROM bits for miscellaneous customer purpose. The value of these bits have no effect on the outputs.

rot_dir_p [0]

Primary turns count rotation direction. Must be set to the same value as rot_dir_s (extended: 0x3F [0]).

Value	Description
0	Rotation direction is counterclockwise
1	Rotation direction is clockwise

Address 0x3F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							diag_channel_sel		pwm_enable	pwm_slw_sel			pwm_porch_sel			pwm_period				tc_hyst_dis_s						rot_dir_s
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

diag_channel_sel [19:18]

Diagnostic channel selector. Defines the redundant channel angle output latched in angle_out_diag_latch (primary: 0x18 [15:0]).

Value	Description: Selected redundant channel
0	AB
1	AB
2	BC
3	CA

pwm_enable [17]

PWM output enable. Setting this bit to a logic value of one enables the PWM output.

pwm_slw_sel [16:14]

PWM fall time control. Controls the fall time of the PWM output. A value of zero sets the PWM output fall time to the fastest rate, a value of seven sets the PWM output fall time to the slowest rate.

Value	Fall time, C_{OUT} = 100 pF (µs)	Fall time, C_{OUT} = 1 nF (µs)
0	0.04	0.12
1	0.10	0.17
2	0.18	0.25
3	0.26	0.33
4	0.67	0.70
5	1.35	1.29
6	2.80	2.58
7	4.02	3.73

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pwm_porch_sel [13:11]
PWM output fixed low and high time selection. This parameter configures the fixed low and high time of the PWM output.

Value	PWM Low Clamp (% Duty Cycle)	PWM High Clamp (% Duty Cycle)
0	2	98
1	3	97
2	4	96
3	5	95
4	6	94
5	7	93
6	8	92
7	0	100

pwm_period [10:7]
PWM output period. Controls the period, or frequency, of the PWM output.

Value	Frequency [Hz]
0	125
1	167
2	250
3	333
4	500
5	667
6	800
7	1000
8	1333
9	1600
10	2000
11	2667
12	4000
13	5333
14	8000
15	16000

tc_hyst_dis_s [6]
Disables secondary channel turns count hysteresis. A hysteresis of approximately 11.25 degrees applies to the angle for the turns count calculation. There is a ±5.625° area on the turns count boundaries (90, 180, 270, 360 degrees) where the turns count is not updated.

Value	Description
0	Hysteresis applied to secondary channel turns count
1	No hysteresis applied to secondary channel turns count

rot_dir_s [0]
Secondary turns count rotation direction. Must be set to the same value as rot_dir_p (extended: 0x3E [0]).

Value	Description
0	Rotation direction is counterclockwise
1	Rotation direction is clockwise

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VOLATILE MEMORY

Address 0x82

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ee_dbe_flag	ee_sbe_flag	ee_ecc						ee_addr						ee_err_status					cp_err	ee_err
Access						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RC	RC

ee_dbe_flag [20]

Error flag indicates detection of an EEPROM dual bit error. The EEPROM ECC logic detects an address with a dual bit error. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM dual bit error detected
1	EEPROM dual bit error detected

ee_sbe_flag [20]

Error flag indicates detection of an EEPROM single bit error. The EEPROM ECC logic detects an address with a single bit error. The ECC logic automatically corrects the faulty bit in the volatile region of memory. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM single bit error detected
1	EEPROM single bit error detected

ee_ecc [18:13]

EEPROM ECC data. After the internal margin test is complete this parameter contains the ECC data bits of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See margin_status (extended: 0x85 [4:3]) for margin results information.

ee_addr [12:7]

EEPROM address data. After the internal margin test is complete this parameter contains the address of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See margin_status (extended: 0x85 [4:3]) for margin results information.

ee_err_status [6:2]

Indicates the error status of the last EEPROM write. Any value greater than zero indicates an error detected during the last EEPROM write.

cp_err [1]

Indicates the error status of the EEPROM write charge pump during the last EEPROM write. A logic value of one indicates an error is detected and sets ee_err_status (extended: 0x82 [6:2]).

ee_err [0]

Indicates detection of an EEPROM write error. The bit is set to a logic value of one when an EEPROM write error is detected. The bit clears after read.

Address 0x83

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ee_data																									
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ee_data [25:0]

EEPROM field data. After the internal margin test is complete this parameter contains information from the data fields of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See margin_status (extended: 0x85 [4:3]) for margin results information.

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Address 0x85

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ee_loop	ee_test_addr						ee_use_test_addr	margin_min_max_fail	margin_status		margin_no_min	margin_no_max	margin_start
Access													RW	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RW	RW	RW

ee_loop [13]

Continuously loop the margin test. When this bit is set to logic value of one the margin test will loop continuously when started and will stop if an error is detected or the margin_start (extended: 0x85 [0]) is cleared.

Value	Description
0	Margin test runs once
1	Margin test loops continuously until an error is detected

ee_test_addr [12:7]

Optional start address for margin test. Defines the starting address for the margin test when ee_use_test_addr (extended: 0x85 [6]) is set to one.

ee_use_test_addr [6]

When set to a logic value of one the margin test will start at the address defined by ee_test_addr (extended: 0x85 [12:7])

Value	Description
0	Margin test starts at address 0x0
1	Margin test starts at address defined by ee_test_addr

margin_min_max_fail [5]

If a margin failure is detected this bit indicates if the failure was detected at the minimum or maximum reference level.

Value	Description
0	Margin test failure detected at minimum threshold
1	Margin test failure detected at maximum threshold

margin_status [4:3]

Indicates the status of the margin test. The bits clear after read or reset event.

Value	Description
0	Reset condition, no result from margin test
1	Pass. No errors detected during margin test
2	Fail. Error detected during margin test
3	In progress. Margin test is still running

margin_no_min [2]

Disable the minimum reference level during margin test. When the bit is set to a logic value of one the margin test does not check for errors at the low reference level.

Value	Description
0	Margin test includes check at the low reference level
1	Margin test does not include check at the low reference level

margin_no_max [1]

Disable the maximum reference level during margin test. When the bit is set to a logic value of one the margin test does not check for errors at the high reference level.

Value	Description
0	Margin test includes check at the high reference level
1	Margin test does not include check at the high reference level

margin_start [0]

Triggers start of margin test. When the bit is set to a logic value of one the margin test begins. The bit clears when the margin test completes and ee_loop (extended: 0x85 [13]) equals zero. If ee_loop equals one the margin test runs until margin_start is set to a value of zero. If margin test detects an error the margin_start bit clears.

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Address 0x87

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																						ecc_test_dbe_flag	ecc_test_sbe_flag	ecc_test_status		ecc_test_start
Access																						RW	RW	RO	RO	RW

ecc_test_dbe_flag [4]
ECC detected the forced DBE (double bit error) error.

Value	Description
0	ECC did not detect the forced DBE error
1	ECC detected the forced DBE error

ecc_test_sbe_flag [3]
ECC detected the forced SBE (single bit error) error.

Value	Description
0	ECC did not detect the forced SBE error
1	ECC detected the forced SBE error

ecc_test_status [2:1]
Indicates the status of the ECC self-test. The bits clear after read or reset event.

Value	Description
0	Reset condition, no result from ECC self-test
1	Pass. No errors detected during ECC self-test
2	Fail. Error detected during ECC self-test
3	ECC self-test is still running

ecc_test_start [0]
Triggers start of ECC self-test. When the bit is set to a logic value of one the ECC self-test begins. The bit clears when the margin test completes.

Address 0xA6

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											manch_comm_e															
Access											RW															

manch_comm_e [15]
Enables Manchester communications mode on the PWM output pin. When this bit is set to a logic value of one, the PWM output stops and the pin becomes and input / output pin for Manchester communication. This bit is set directly with a write operation or indirectly using the access code. To exit Manchester communications mode the bit is set to a logic value of zero.

Address 0xAA

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																									poks_test_running	poks_test_start
Access																									RO	RW

poks_test_running [1]
POKs/IOKs startup test is running.

Value	Description
0	POKs/IOKs startup test is not running.
1	POKs/IOKs startup test is running.

poks_test_start [0]
When set to 1, run the POKs/IOKs self-test. If an error occurs, it is reported in poks_self_test_failed_flag (primary: 0xC [7]).

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SAFETY AND DIAGNOSTICS

The A33023 was developed in accordance with the ASIL design flow (ISO 26262) and incorporates several internal diagnostics and error/warning/status flags, enabling the host microcontroller to assess the operational status of the die.

A short summary of the diagnostics is provided below. A complete listing and discussion of the A33023 safety features may be found in the Safety Manual.

Status, Error, and Warning Flags

The A33023 features include several status, error, and warning flags. These flags allow the external controller to act in response of detected fault condition. Table 14 provides a summary list of the flags. More information is also found in the Primary Serial Interface Register Reference.

All flags may be read through the primary serial registers (primary: 0xF) via SPI or Manchester communication. These error flags remain set until the register is read or reset, and the condition is removed.

OFE Assertion Following Power-On

Following power-on, the OFE flag (direct address 0x0F, bit 3) may assert while the internal oscillators settle. If this occurs, an attempt should be made to clear the flag by performing a second read of the error register (direct 0x0F). If all error flags are clear on the second read the device is operating normally and no further action is required.

Error Reporting Through SPI

There are two error reporting bits, S0 and S1, within the A33023 SPI frame. The value of S0 and S1 represent the logical "or" of the bits within the error register. ABI and SLR related flags are only reported by S1. The S0 and S1 bits clear after a SPI read transaction and the condition for the flag no longer exists. Note, S0 and S1 are set to a value of one after a reset event. If an error flag is masked the result of this flag is not reported by S0 and S1.

Information Flags

The A33023 features a dedicated status register (Primary 0xC), providing informational flags to the external controller. These flags may be useful for the external controller to monitor operation. Table 15 provides a summary list of the information status flags. More information is also found in the Primary Serial Interface Register Reference.

Table 14: Status Register Contents (Primary 0xC)

Bit Value	Status Flag	Description
0	ang_rdy	Angle ready
1	rot_h	Rotation direction
2	acd	ABI count-up procedure complete
3	abi	ABI integrity error detected
4	slr	Slew rate warning
6	mask_active	Mask active
7	poks_ self_ test_ failed_ flag	POK/IOK self-test
9	ecc_self _test_ failed_ flag	Error correction code self-test

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Table 15: Status and Error Flags

Status and Error Flag	Description	Flag Response
VCF	Voltage check failure	vcf = 1 (primary: 0xF [0]
TSE	Temperature sensor error	tse = 1 (primary: 0xF [1]
SAT	Saturation error	sat = 1 (primary: 0xF [2]
OFE	Oscillator frequency discrepancy error	ofe = 1 (primary: 0xF [3]
SMM	Signal path (primary channel versus secondary channel) mismatch error	smm = 1 (primary: 0xF [4]
MSL	Magnet sense low (input condition below low threshold) error	msl = 1 (primary: 0xF [5]
MSH	Magnet sense high (input condition above high threshold) error	msl = 1 (primary: 0xF [6]
UVCC	Undervoltage error	uvcc = 1 (primary: 0xF [7]
OVCC	Overvoltage error	ovcc = 1 (primary: 0xF [8]
POR	Power-on reset event	por = 1 (primary: 0xF [9]
ESE	Single bit EEPROM error (correctable)	ese = 1 (primary: 0xF [10]
EUE	Multi-bit EEPROM error (uncorrectable)	eue = 1 (primary: 0xF [11]
SME	Shadow memory error (multiple input shift register signature error)	sme = 1 (primary: 0xF [12]
BSY	Extended access busy condition	bsy = 1 (primary: 0xF [13]
XEE	Extended execute error condition	exe = 1 (primary: 0xF [14]
IER	Interface error condition	ier = 1 (primary: 0xF [15]
ABI	Abi integrity fault	abi = 1 (primary: 0x0C [3]
SLR	Abi slew rate warning	slr = 1 (primary: 0x0C [4]

Error Reporting Through PWM

The PWM output is configurable to report flags using a special frequency and duty cycle or by going to a high-impedance state. The parameter make_errors_high_z (extended: 0x24 [15]) configures the PWM error reporting function. When set to a value of one, the error flags result in a PWM at high-impedance state for a minimum of two periods. When make_errors_high_z is set to a value of zero, the PWM reports the error flags at a defined duty cycle, shown in Table 16, and at 1/2 the frequency defined by pwm_period (extended: 0x3F [10:7]).

In the event of multiple error flags, when make_errors_high_z equals zero, the PWM output reports the error condition according to priority. Table 16 lists the error flags in the order of priority from highest to lowest. The highest priority error dictates the PWM duty cycle. Error flags OFE, SME and EUE are the highest priority flags and report through the PWM output by a high-impedance state (100% duty cycle).

The parameter pwm_porch_sel (extended: 0x3F [13:11]) configures the PWM minimum and maximum duty cycle and sets the duty cycle used for error reporting.

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Table 16: PWM Error Flag Duty Cycle

pwm_porch_sel		0	1	2	3	4	5	6	7
Error	**Priority**	**Duty Cycle (%)**							
OFE	Highest	100	100	100	100	100	100	100	100
SME	Highest	100	100	100	100	100	100	100	100
EUE	Highest	100	100	100	100	100	100	100	100
POR+ESE	1	78.05	78.20	77.96	78.06	78.13	78.16	78.16	79.22
POR	2	16.31	16.27	16.27	16.29	16.35	16.44	16.24	14.90
UVCC	3	38.89	38.76	38.64	38.88	38.78	38.70	38.64	38.43
VCF	4	33.25	33.23	33.22	33.24	33.26	32.97	33.04	32.55
OVCC	5	72.40	72.67	72.55	72.41	72.60	72.43	72.56	73.33
TSE	6	66.75	66.77	66.78	66.76	66.74	67.03	66.96	67.45
MSH	7	61.11	61.24	61.36	61.12	61.22	61.30	61.36	61.57
SAT	8	56.59	56.45	56.67	56.53	56.73	56.58	56.75	56.86
MSL	9	44.54	44.29	44.41	44.53	44.31	44.44	44.24	44.31
SMM	10	21.95	21.80	22.04	21.94	21.87	21.84	21.84	20.78
ABI or SLR	11	27.60	27.33	27.45	27.59	27.40	27.57	27.44	26.67
ACD	12	84.07	84.10	84.09	84.06	83.99	83.89	84.09	85.49
ESE	13	78.05	78.20	77.96	78.06	78.13	78.16	78.16	79.22

Error Reporting in ABI/UVW

Error reporting when using ABI/UVW requires the transmission of angle information to be interrupted. When using ABI/UVW, it is recommended to use an additional output (PWM or SPI).

For more information on ABI / UVW error reporting, contact Allegro MicroSystems.

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APPLICATION INFORMATION

Once the device is powered on, the rate of change of V_{CC} must be limited to less than 1 V/µs.

Note: It is recommended to leave the ABI pins floating if the ABI output is not used.

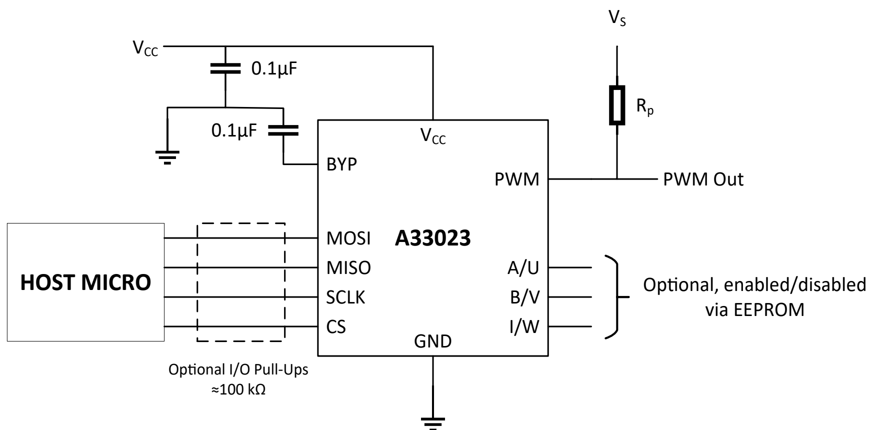

Figure 37: Typical A33023 configuration using SPI interface with PWM enabled

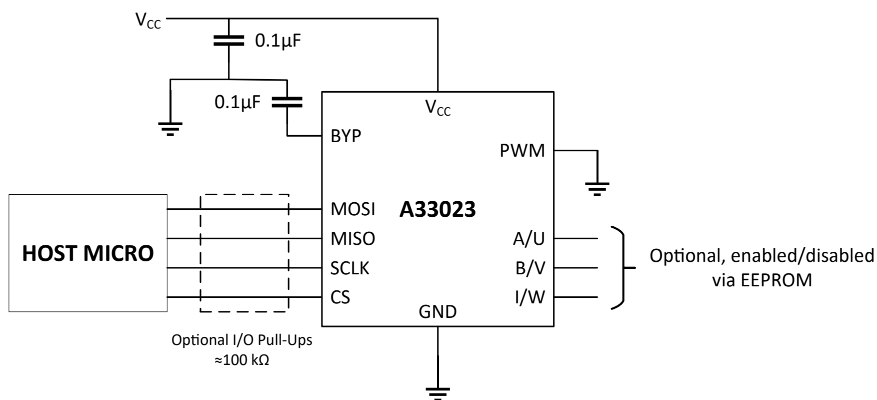

Figure 38: Typical A33023 configuration using SPI interface with PWM disabled

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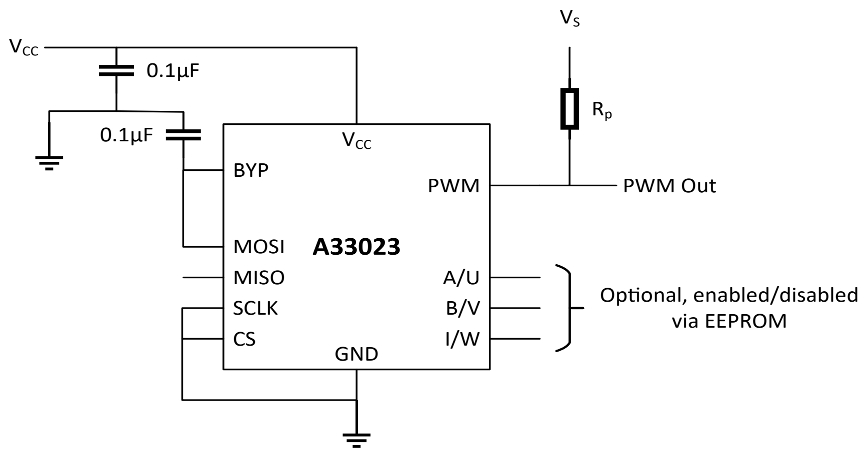

Figure 39: Typical A33023 configuration with PWM enabled and SPI not connected

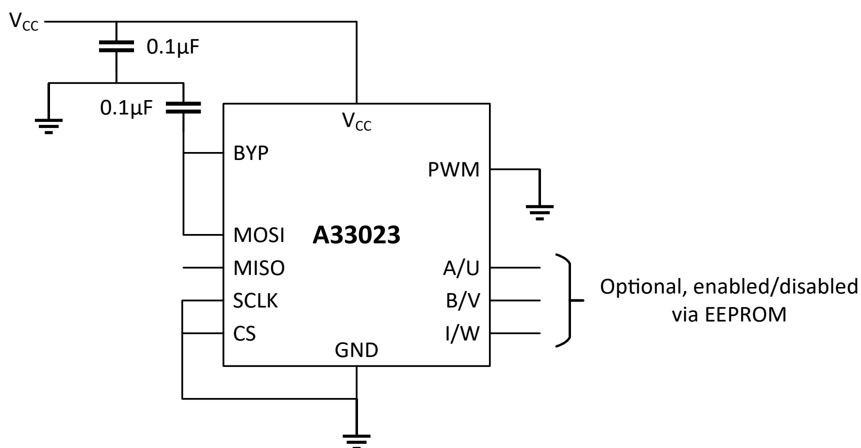

Figure 40: Typical A33023 configuration with PWM disabled and SPI not connected

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PACKAGE OUTLINE DRAWING

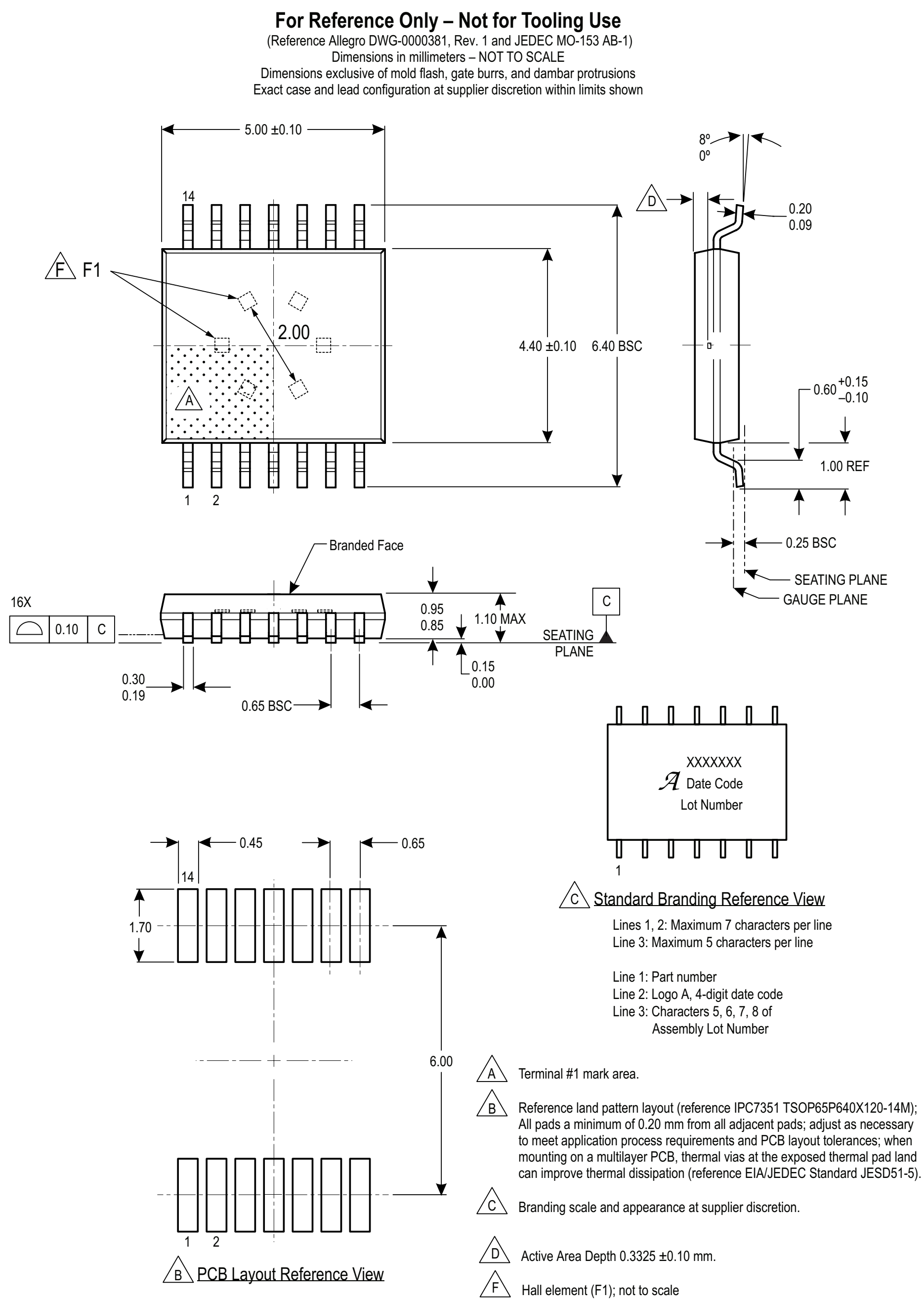

Figure 41: 14-Pin TSSOP Package

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Revision History

Number	Date	Description
–	March 20, 2023	Initial release

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APPENDIX

MATLAB Function to compute the A33023 Linearization Coefficients

```
function [lin_coef,gap]=A33023_calc_lin_coef(angle_mech,angle_meas)
%
% This function computes the linearization coefficients for the A33023.
% Linearization is 16 segments with fixed pivot points (0°, 360°/16, 2*360°/16,..., 15×360°/16).
% The coefficients corresponds to the angle error between the measured angle at the pivot points and the actual magnet position.
%
% Inputs:
%   - angle_mech: n×1 vector: actual magnet position: must be between 0° and 360° and monotically increasing [°]
%   - angle_meas: n×1 vector: A33023 measured position at each angle_mech position (direct output of A33023) [°]
%
% Outputs:
%   - lin_coef: 16×1 vector: contains the linearization coefficients [LSB]
%       o lin_coef(1) corresponds to XXX_linearization_0, lin_coef(2) corresponds to XXX_linear-ization_1, ... , lin_coef(16) corresponds to XXX_linearization_15
%       o coefficients must be converted to 8 bits signed
%   - gap: 16×1 vector: angle error between actual mechanical position and measured position

%% Inspect inputs

% Re-arrange data if necessary
if size(angle_mech,2)>1
    angle_mech=angle_mech';
end
% Only 360° max input range is acceptable
if max(angle_mech)-min(angle_mech)>360
    error('Linearization range must be <=360°')
end
% angle_mech must be increasing
```


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```
if sum(diff(angle_mech)<0)>0
    error('angle_mech must be increasing')
end
% Avoid issues with 360° exact rotation
if wrapTo360(min(angle_mech))==wrapTo360(max(angle_mech))-360
    angle_mech=angle_mech(1:end-1);
    angle_meas=angle_meas(1:end-1);
end

%% Compute the angle error between measurements and actual position

% Re-arrange measured angle
angle_meas_temp=unwrap(wrapTo360(angle_meas)*2*pi/360)*360/2/pi;
angle_meas_temp=unique([angle_meas_temp-360;angle_meas_temp;angle_meas_temp+360],'stable');

% Re-arrange actual position
angle_mech_temp=unwrap(wrapTo360(angle_mech)*2*pi/360)*360/2/pi;
angle_mech_temp=unique([angle_mech_temp-360;angle_mech_temp;angle_mech_temp+360]);

% Interpolate actual position at linearization pivot positions
pivot=[0:360/16:360-360/16]’;
mech_pos=interp1(angle_meas_temp,angle_mech_temp,pivot,'spline','extrap');

% Angle error between measurements and actual position
gap=wrapTo180(pivot-mech_pos);

%% Compute the linearization coefficients

% Select only the measurements inside the range
index=zeros(length(pivot),1);
for i=1:length(pivot)
    if min(abs(wrapTo360(angle_meas)-pivot(i)))<=360/16
```


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```
        index(i)=1;
    end
end
index=logical(index);

% Compute the coefficient (remove the mean offset)
lin_coef=round((gap-mean(gap(index)))/(2*11.25/2^8));

% Bound the linearization coefficients
lin_coef(isnan(lin_coef))=0;
lin_coef(lin_coef>2^7-1)=2^7-1;
lin_coef(lin_coef<-2^7)=-2^7;
```


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