A33115

Precision TMR Angle Sensor IC with Integrated Diagnostics and Low Power Mode

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
- Designed to meet ASIL D requirements when used in conjunction with appropriate system-level control
  - SPI protocol
  - PWM and ABI output protocols
- Dual channel signal path
  - Primary TMR channel capable of 14-bit noise-free resolution
  - Secondary channel capable of 10-bit noise-free resolution
- On-chip Turns Counter tracks motion in 90° increments Wide operating voltage (3.7 to 19 V) enables direct connection to vehicle battery
- Low Power Mode with user-programmable duty cycle reduces power consumption when the IC is not operating in normal operation mode
- Linearization to reduce error from misalignment between the sensor and target magnet
- SPI interface allows use of multiple independent sensors for applications requiring redundancy
  - Allows external interrogation of data from both the primary and secondary channels over SPI. 32-bit SPI message includes a rolling counter and address in every message to protect against stuck-at or masquerading faults
  - 16b precision angle position output over SPI
  - 5-bit CRC on SPI messages
- ABI and UVW interfaces provide high resolution and lowest latency angle information
  - Option to output 2nd channel over ABI/UVW pins to allow external comparison of two channels
- EEPROM with Error Correction Control (ECC) and Data Address Hashing for trimming calibration
- EEPROM programmable angle reference (0°) position and rotation direction (CW or CCW)
- Automatic gain and offset control on internal sine/cosine signals for optimized accuracy over field, temperature, and lifetime drifts
- AEC-Q100 grade 1 qualification planned

DESCRIPTION

The A33115 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic sensing technology. The devices have a system-on-chip (SoC) architecture that includes two angle sensing channels, digital signal processing, and various output options: SPI, PWM, motor commutation (U, V, W), and encoder outputs (A, B, I). Also integrated into the devices are on-chip EEPROM technology, capable of supporting a high number of read/write cycles for flexible end-of-line programming of calibration parameters.

The low 18 µs latency of these devices makes them ideal for automotive applications requiring fast 0° to 360° angle measurements, such as electronic power steering (EPS), seatbelt motor systems, transmission actuators, shift-by-wire systems, electronic braking systems, and throttle systems.

The A33115 was developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications and targeting ASIL D compliance when used in conjunction with appropriate system-level controls.

These devices also include integrated linearization features. This allows for correction of misalignment issues between the IC and the target magnet with minimal added latency.

The A33115 includes an on-chip Turns Counter and Low Power Mode. The Turns Counter tracks motion of the target magnet in increments of 90°. Low Power Mode reduces power consumption to enable direct connection to the vehicle battery, reducing current consumption when the vehicle is in the key-off state.

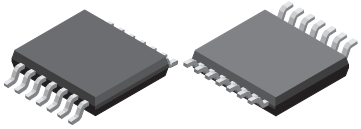
The A33115 supports two communication protocols, SPI and serial Manchester on the PWM pin, for configuration, calibration, and testing.

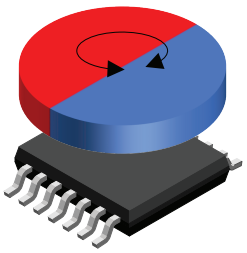
The A33115 is available in a single-die 14-pin TSSOP package. The package is lead (Pb) free with 100% matte-tin leadframe plating. The A33115 is planned for AEC-Q100 grade 1 qualification.

PACKAGE:

14-pin TSSOP
(Suffix LE)

Not to scale





SELECTION GUIDE

Part Number	Primary Transducer	Package	Packing
A33115KLEATR-S	TMR	14-pin TSSOP	4000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	38	V
Reverse Supply Voltage	V_{RCC}		–18	V
Digital I/O Forward Voltage	$V_{IN(DIG)}$	MOSI, MISO, SCLK, CS, A/U, B/V, I/W, BYP	3.65	V
PWM Forward Voltage	$V_{OUT(PWM)}$		18	V
Digital Signal Pins Reverse Voltage	$V_{R(DIG)}$		–0.5	V
PWM Reverse Voltage	$V_{R(PWM)}$		–0.5	V
Operating Ambient Temperature	T_A	K range	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C
External Magnetic Field	B_{MAX}	Continuous $T_J \leq 165°C$	1200	G
		5 hours at $T_A \leq 25°C$	1500	G

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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
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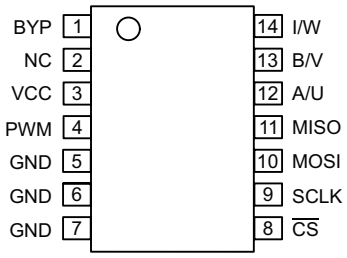
THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package, measured on JEDEC JESD51-7 2s2p board	82	°C/W

[1] Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST

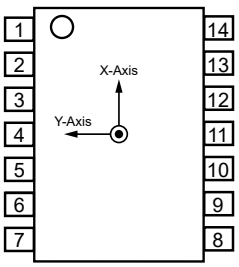
LE 14-Pin TSSOP Pinout Diagram



LE 14-Pin TSSOP Terminal List Table

Pin Name	Pin Number	Function
BYP	1	External bypass capacitor terminal for internal regulator and self-write
NC	2	Not connected; connect to ground in application
VCC	3	Power supply
PWM	4	PWM angle output / Manchester Communication
GND	5, 6, 7	Device ground terminal
$\overline{CS}$	8	SPI: Chip Select terminal, active low input
SCLK	9	SPI Clock terminal input
MOSI	10	SPI: Controller Output, Peripheral Input
MISO	11	SPI Controller Input, Peripheral Output
A/U	12	Option 1: Quadrature A output signal Option 2: U (phase 1) output signal
B/V	13	Option 1: Quadrature B output signal Option 2: V (phase 2) output signal
I/W	14	Option 1: Quadrature I (index) output signal Option 2: W (phase 3) output signal

AXIS DEFINITION



Note: Arrows show the default polarity of each axis. Polarity can be changed with internal settings.

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FUNCTIONAL BLOCK DIAGRAM

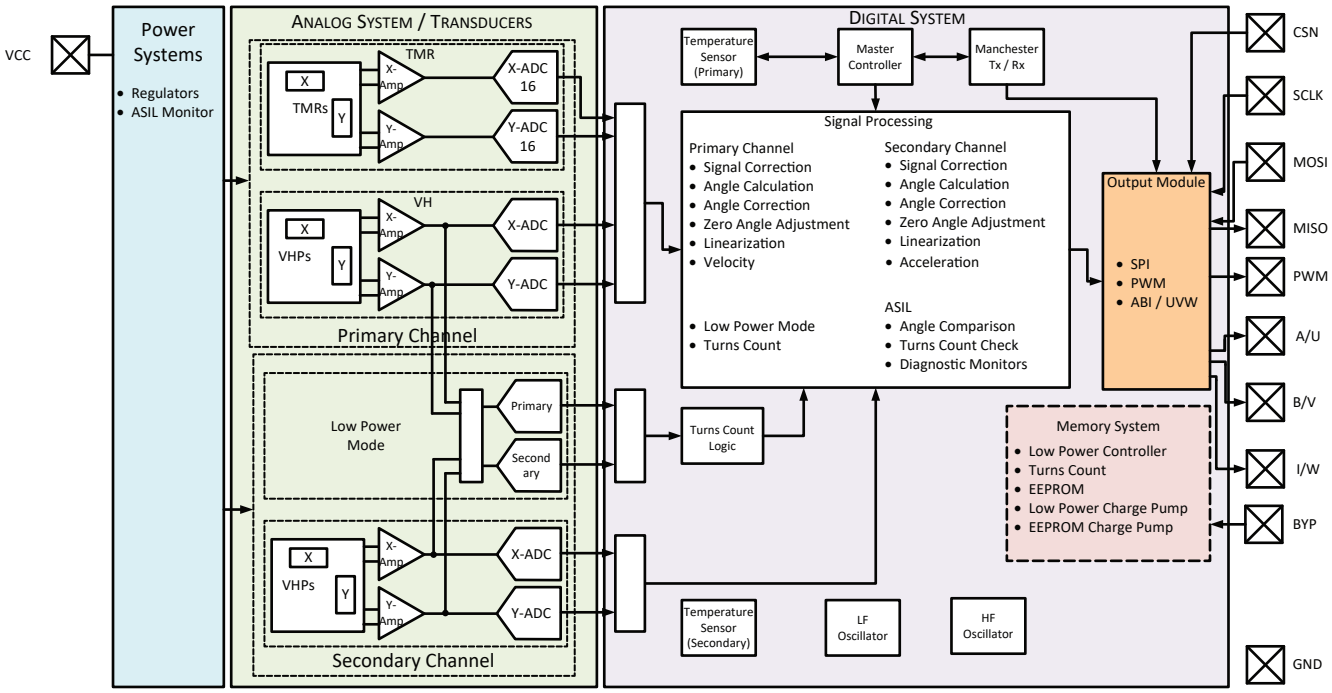

Figure 1: Functional Block Diagram

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OPERATING CHARACTERISTICS: Valid over full operating voltage, V_{CC}, and ambient temperature ranges, T_A, for $T_J < T_J$(max), unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		3.7	–	19	V
Supply Current	I_{CC}	In Normal Power Mode and sampling angles	–	–	22	mA
Transport Mode Supply Current	$I_{CC(TRANS)}$	In Transport mode, sampling disabled; V_{CC} = 12 V, T_A = 25°C	–	23	–	µA
Low-Power Mode Sleep Current	$I_{CC(LP\_SLEEP)}$	I_{CC} in “sleep” state of Low Power Mode; V_{CC} = 12 V, T_A = 25°C	–	27	–	µA
Low-Power Mode Wake Current	$I_{CC(LP\_WAKE)}$	I_{CC} in “wake” state of Low Power Mode; V_{CC} = 12 V, T_A = 25°C	–	3.62	–	mA
Low-Power Mode Average Supply Current	$I_{CC(AVG\_LP)}$	Average I_{CC} in Low Power Mode with default 1.8 ms sleep time; T_A = 25°C	–	50	–	µA
Low-Power Mode Sleep Time [2]	t_{SLEEP_LP}	Programmable Sleep time duration in Low Power Mode	0.5	1.8	100	ms
Low-Power Mode Awake Time	t_{WAKE_LP}	Awake time duration in Low Power Mode with default settings	–	10	–	µs
Low-Power Mode Exit Ramp Rate [2]	SR_{LPM_EXIT}	Slowest ramp rate allowed when exiting LPM; applied to SCLK, MOSI, CS pins	100	–	–	mV/µs
Clock Frequency	f_{CLK}	Main Oscillator	28	32	36	MHz
		Low Power Mode Awake State Oscillator	1.6	2	2.4	MHz
		Low Power Mode Sleep State Oscillator	200	250	300	kHz
		Signal Processing Frequency [2]	14	16	18	MHz
Undervoltage Detection Threshold [3]	$V_{UVD(HIGH)}$	dV/dt = +1 V/ms	–	–	3.7	V
	$V_{UVD(LOW)}$	dV/dt = –1 V/ms	3.25	–	–	V
Overvoltage Detection Threshold	$V_{OVD(HIGH)}$	dV/dt = +1 V/ms	–	–	23	V
	$V_{OVD(LOW)}$	dV/dt = –1 V/ms	20	–	–	V
Forward Supply Zener Clamp Voltage	V_{ZUP}	I_{CC} + 3 mA	38	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RZUP}	$I_{CC} = I_{RCC}$	–	–	–18	V
Reverse Battery Current	I_{RCC}	V_{CC} = –18 V	–5	–	–	mA
Power-On Time [2][4]	t_{PO}		–	5	–	ms
Bypass Pin Output Voltage [5]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF	2.97	3.3	3.63	V

[1] Conditions of maximum supply voltage and ambient must not exceed maximum junction temperature.
[2] Parameter is not measured at final test. Determined by design.
[3] Undervoltage flag indicates V_{CC} level below expected operational range. Degraded sensor accuracy may result.
[4] Angle is considered valid once ANG_RDY bit (bit 0 of serial address 0xE) is set to a 1, and no error flags are present.
[5] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.

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OPERATING CHARACTERISTICS (continued): Valid over full operating voltage, V_{CC}, and ambient temperature ranges, T_A, for $T_J < T_J(max)$, unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI SPECIFICATIONS [1]						
Load Resistance	R_L		100	–	–	kΩ
Load Capacitance	C_L	Loading on digital output (MISO) pin with frequency up to 10 MHz	–	–	20	pF
		Loading on digital output (MISO) pin with frequency up to 1 MHz	–	–	50	pF
Input Leakage Current	I_{L_SPI}	Leakage current into MOSI, SCLK, $\overline{CS}$ pins; Bus voltage ≤ $V_{IH(MAX)}$	–	–	35	µA
SPI AND ABI/UVW INTERFACE VOLTAGE SPECIFICATIONS						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO, ABI/UVW pins	2.93	3.3	3.63	V
Digital Output Low Voltage	V_{OL}	MISO, ABI/UVW pins	–	0.3	0.5	V
SPI INTERFACE TIMING SPECIFICATIONS [1]						
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	C_L ≤ 20 pF	0.1	–	10	MHz
		C_L ≤ 50 pF	0.1	–	1	MHz
SPI Clock Duty Cycle	D_{fSCLK}		40	–	60	%
SPI Frame Rate	t_{SPI}		3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge; C_L ≤ 20 pF	–	30	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to $\overline{CS}$ Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [1]	f_{PWM}	PWM frequency minimum setting	–	125	–	Hz
		PWM programmable options	–	16	–	steps
		PWM frequency maximum setting	–	16	–	kHz
PWM Duty Cycle Low Clamp [1]	$D_{PWM(min)}$	2% = PWM_PORCH_SEL = 000_2 8% = PWM_PORCH_SEL = 110_2	2	–	8	%
PWM Duty Cycle High Clamp [1]	$D_{PWM(max)}$	92% = PWM_PORCH_SEL = 110_2 98% = PWM_PORCH_SEL = 000_2	92	–	98	%
PWM Output Clamp Step Size [1]	$D_{PWM(step\_size)}$	PWM_PORCH_SEL EEPROM field	–	1	–	%
PWM Output leakage Current	I_{OUT}	Output voltage ≤ 5.5 V, output FET off	–	–	100	µA
PWM Output Saturation Voltage	$V_{PWM\_SAT(Low)}$	Output current = –4.7 mA, V_{CC} = 5 V, Output FET on	–	–	0.35	V
PWM Max Operation Pull-Up Voltage [1]	V_{SPWM}		–	–	5.5	V
PWM Output Short-Circuit Current Limiter [1]	$I_{OUTSC(SINK)}$	Internally limited	20	–	50	mA
PWM Max Operation Current [1]	I_{PWM_LIMIT}	Recommended max operation PWM current	–	–	20	mA
PWM Load Capacitance [1]	C_{PWMLX}		–	–	4.7	nF

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INCREMENTAL OUTPUT SPECIFICATIONS [1]						
ABI and UVW Output Angular Hysteresis	hys_{ANG}	Programmable	0	–	1.41	degrees
AB Channel Resolution	RES_{AB}	Programmable via EEPROM, 4-bit field. Specified in pulses per revolution, PPR	1	–	2048	PPR
AB Quadrature Resolution	RES_{AB_INT}	Equal to 4 × RESAB, specified in counts per revolution, CPR	4	–	8192	CPR
UVW Poles Pairs	N_{pole}	DC commutation signals. Programmable via EEPROM, 4-bit field.	1	–	16	pole pairs
Maximum Sourcing Current	I_{SOURCE}	Output voltage ≥ 2.8 V; IO voltage of 3.3 V	–	1.0	–	mA
Maximum Sinking Current	I_{SINK}	Output voltage ≤ 0.5 V; IO voltage of 3.3 V	–	1.0	–	mA

[1] Parameter is not measured at final test. Determined by design.

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MAGNETIC CHARACTERISTICS: Valid at T_A and V_{CC} unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Magnetic Flux Density	B	Absolute peak flux density VH sensing element	330 [1]	–	1000	G
		Absolute peak flux density TMR sensing element; operational limit	330 [1]	–	1000	G
ANGLE CHARACTERISTICS						
Output Resolution [3]	RES_{ANGLE}	Number of bits available	–	16	–	bits
Response Time [2][4]	$t_{RESPONSE}$	Angular latency, bandwidth = 12.5 kHz; Default VH Channel BW	–	24	28	µs
		Angular latency, bandwidth = 25 kHz; Default TMR Channel BW	–	18	21	µs
Refresh Rate [2][5]	t_{ANG}	Angle update rate on ABI with 4× interpolator	–	0.5	–	µs
		Angle update rate on ABI with 2× interpolator	–	1	–	µs
		Angle update rate on ABI with interpolator bypassed; Angle update rate via SPI/PWM	–	2	–	µs
Channel Mismatch Primary to Secondary	$\Delta ANGLE_{CHAN}$	Primary to secondary mismatch error, B = 300 G, target RPM = 0	–	1	5	degrees

[1] The A33115 operates in fields below 300 G but with reduced accuracy. Fields lower than 330 G may result in a Magnetic Signal Low (MSL) flag.
[2] Parameter is not measured at final test. Determined by design.
[3] RES_{ANGLE} represents the number of bits of data available from the direct registers.
[4] Response time is measured at the time between the magnet crossing a given angle and the part reporting that angle via ABI.
[5] Rate at which a new angle value is ready.

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MAGNETIC CHARACTERISTICS (continued): Valid at T_A and V_{CC} unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ANGLE CHARACTERISTICS – TMR CHANNEL							
Angle Error	ERR_{ANG}	Ideal magnet alignment, B = 300 G, target rpm = 0	T_A = 25°C	–1.4	±0.5	+1.4	degrees
			T_A = 125°C	–1.5	±0.75	+1.5	degrees
Angle Drift Due to Temperature	$ANGLE_{DRIFT}$	Change in angle from 25°C; ideal magnet alignment, B = 300 G, target rpm = 0	T_A = 125°C	–0.9	±0.5	+0.9	degrees
			T_A = –40°C	–	±0.5	–	degrees
Angle Noise	N_{ANGLE}	B = 300 G, target rpm = 0, 3 sigma noise, BW = 25 kHz	T_A = 25°C	–	±0.012	–	degrees
			T_A = 125°C	–	±0.013	–	degrees
Noise-Free Number of Bits [1][2]	b_{NOISE_FREE}	T_A = 25°C, B = 300 G, target rpm = 0, 6 sigma noise, BW = 25 kHz	T_A = 25°C	–	13.8	–	bits
			T_A = 125°C	–	13.7	–	bits
Angle Error Drift Over Lifetime	$ANGLE_{DRIFT\_LIFE}$	B = 300 G, average maximum drift observed following AEC-Q100 Grade 1 qualification testing	Drift measured relative to zero hour	–	0.86	–	degrees
			Drift measured following preconditioning	–	0.53	–	degrees
ANGLE CHARACTERISTICS – VH CHANNEL							
Angle Error	ERR_{ANG}	Ideal magnet alignment, B = 300 G, target rpm = 0	T_A = 25°C	–0.8	±0.5	+0.8	degrees
			T_A = 125°C	–1.0	–	+1.0	degrees
Angle Drift Due to Temperature	$ANGLE_{DRIFT}$	Change in angle from 25°C; ideal magnet alignment, B = 300 G, target rpm = 0	T_A = 125°C	–0.9	±0.5	+0.9	degrees
			T_A = –40°C	–	±0.5	–	degrees
Angle Noise	N_{ANGLE}	B = 300 G, target rpm = 0, 3 sigma noise, BW = 12.5 kHz	T_A = 25°C	–	±0.376	–	degrees
			T_A = 125°C	–	±0.478	–	degrees
Noise-Free Number of Bits [1][2]	b_{NOISE_FREE}	B = 300 G, target rpm = 0, 6 sigma noise, BW = 12.5 kHz	T_A = 25°C	–	8.9	–	bits
			T_A = 125°C	–	8.5	–	bits
Angle Error Drift Over Lifetime	$ANGLE_{DRIFT\_LIFE}$	B = 300 G, average maximum drift observed following AEC-Q100 Grade 1 qualification testing	Drift measured relative to to zero hour	–	0.26	–	degrees
			Drift measured following preconditioning	–	0.25	–	degrees

[1] Based on characterization data; not measured at final test.

[2] The Noise-Free Number of Bits is defined as: $\log_2(\frac{360}{6\times\sigma})$ where σ is the standard deviation.

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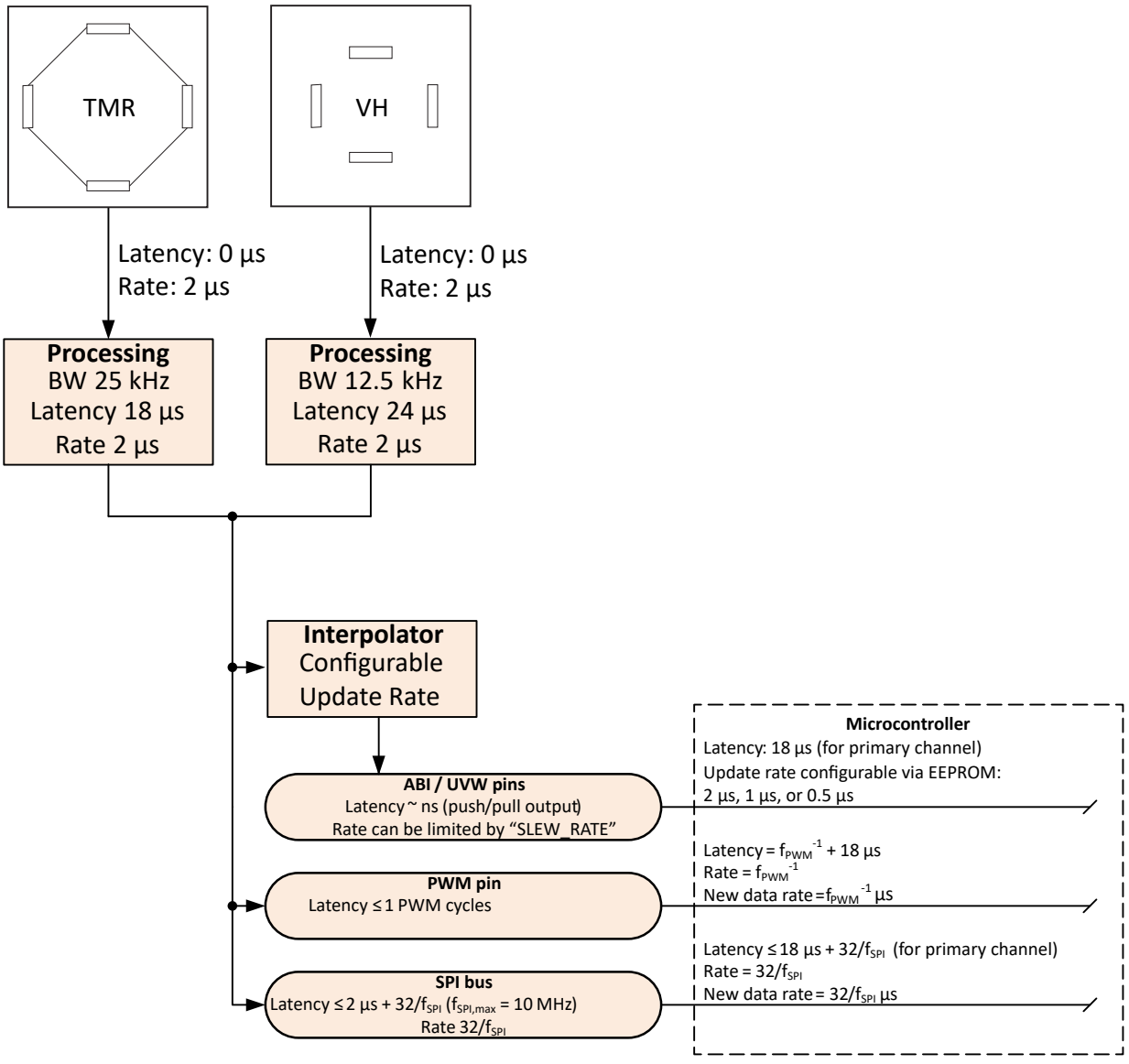

Figure 2: Signal Path Block Diagram Corresponding to default EEPROM settings.

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FUNCTIONAL DESCRIPTION

Overview

The A33115 is a dual channel rotary position device in a surface-mount package, providing solid-state consistency and reliability, and supporting a wide variety of automotive applications. The two channels provide redundant angle sensing within a single device. The primary channel sensing element is comprised of tunnel magnetoresistance, TMR, elements to measure magnetic flux density in the x-y plane (parallel to the branded face of the device). The secondary channel sensing element is comprised of vertical Hall-effect, VH, elements to measure magnetic flux density in the x-y plane (parallel to the branded face of the device). The information from each channel is processed in parallel to compute an angle measurement based on the input x-y vector. The resulting angle information, primary and secondary, is passed through additional processing and made available as two independent outputs. In addition, the A33115 compares the primary angle to the secondary angle to monitor the integrity of the angle information. For high field requirements, contact Allegro MicroSystems for available options.

This device is an advanced, programmable system-on-chip (SoC), incorporating multiple sensing technologies, TMR and vertical Hall-effect, analog signal conditioning, high-speed sampling analog-to-digital converters, digital filtering, digital signal processing (which includes two separate signal paths, primary and secondary), and multiple output options. Available outputs options include SPI, PWM, and motor commutation outputs (U, V, W) or encoder outputs (A, B, I).

Zero angle, filtering, linearization, and diagnostic adjustment options are available in the A33115. These options are configurable in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurement

The A33115 features primary and secondary signal paths to generate high resolution, low latency angle readings. The TMR element offers the highest resolution. The A33115 has an additional feature, low power mode, for angle turns counting. When operating in low power mode, a dedicated signal path monitors angle information, using VH elements for the primary and secondary channels to track the turns count.

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. The delay from time of the input until generation of a processed angle value is $t_{RESPONSE}$. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. Register values transmitted are latched on the first SCLK edge of the SPI response frame. This results in a variable age of the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$.

Figure 2 (page above) shows the update rate and the signal delay of the different angle output paths depending on sensor settings.

Impact of High-Speed Sensing

Due to signal path latency, the angle information is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e., a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm), and is referred to as angular lag.

The lag is directly proportional to rpm, and may be compensated for externally, if the velocity is known.

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Operational Modes

PWM Output

The A33115 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to the angle output. The PWM output is enabled by setting the parameter PWM_ENABLE (extended: 0x25 [24]) The PWM output is configurable, by the parameter PWM_CHANNEL (extend: 0x25 [23]), to output data from the primary or secondary channel.

The PWM period is defined as shown in Figure 3. The PWM period may be measured by observing the rising edge to rising edge time. The PWM duty cycle is the rising edge to falling edge time as a percent of the PWM period. The fixed high and low times are configurable by the EEPROM parameter PWM_PORCH_SEL (extended: 0x2A [25:23]). The parameter PWM_PERIOD (extended: 0x25 [22:19]) configures the PWM carrier frequency.

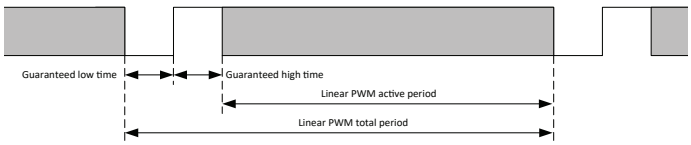

Figure 3: PWM Period

Table 1: PWM_PORCH_SEL

Value	PWM Low Clamp (% Duty Cycle)	PWM High Clamp (% Duty Cycle)
0	2	98
1	3	97
2	4	96
3	5	95
4	6	94
5	7	93
6	8	92
7	2	98

Table 2: PWM_PERIOD

Value	Frequency (Hz)
0	125
1	167
2	250
3	333
4	500
5	667
6	800
7	1000

Value	Frequency (Hz)
8	1333
9	1600
10	2000
11	2667
12	4000
13	5333
14	8000
15	16000

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Manchester, NH 03103-3353 U.S.A.
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Incremental Output Interface (ABI)

The A33115 offers an incremental output mode in the form of quadrature A/B and Index outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per magnetic revolution, giving a cycle resolution of $(360/2^N)$ degrees per cycle, where N is set by the RESOLUTION_PAIRS field in EEPROM; see Table 3. The "B" signal is offset from "A" by ¼ of the cycle period. The "I" signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown below.

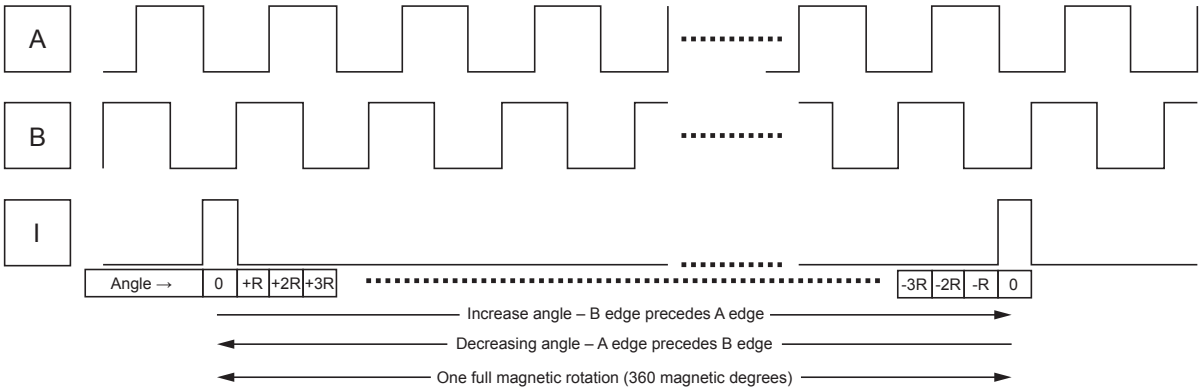

Figure 4: One Full Magnetic Revolution

Since A and B are offset by ¼ of a cycle, they are in quadrature and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

Table 3

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a grey coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4

Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2 → Q1

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The duration of one cycle is referred to as 360 electrical degrees, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior.

Ideally, the A and B cycle would be as shown below for a constant velocity:

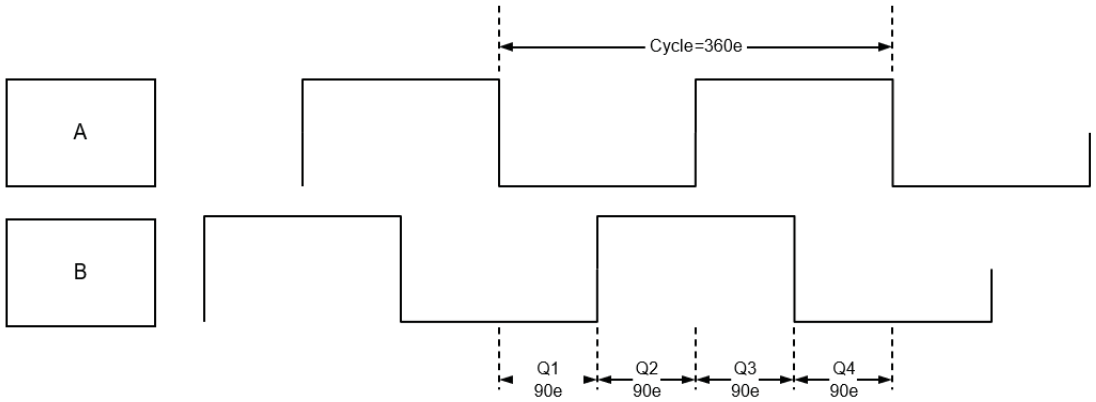

Figure 5: Electrical Cycle

Practically, the edge rate of the A and B signals, and the switching threshold of the receiver I/Os, will affect the quadrature periods:

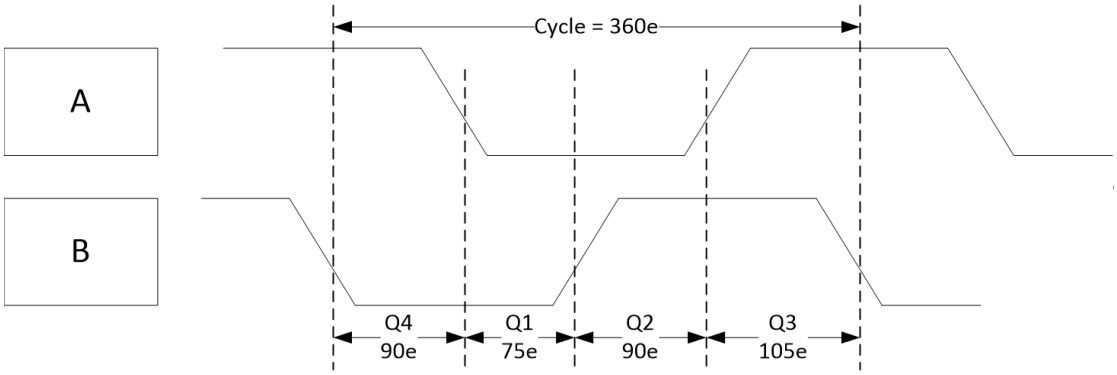

Figure 6: Electrical Cycle

Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

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ABI / UVW OUTPUT CONFIGURATION

The A33115 uses three pins to output either ABI information or UVW information. The parameter ABI_0_UVW_1 (extended: 0x25 [1]) selects the protocol ABI or UVW. The parameter ABI_UVW_CHANNEL (extended: 0x25 [14]) controls the angle data channel reported on the ABI or UVW outputs. The ABI or UVW outputs are enabled or disabled by setting the parameter ABI_UVW_EN (extended: 0x25 [15]).

The A33115 ABI output resolution and quantity of UVW pole pairs is configurable by setting the parameter ABI_UVW_RESOLUTION (extended: 0x25 [5:2]) The options for ABI Cycle Resolution and Quadrature State Resolution and are shown in Table 5.

ABI INVERSION

The logic levels of the ABI pins may be inverted by setting the ABI_UVW_INVERT_OUT_EN (extended: 0x25 [1]) bit within EEPROM. This also applies if using the UVW output logic.

Table 5: ABI / UVW Output Resolution

ABI_UVW_RESOLUTION	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)	UVW Quantity of Pole-Pairs	UVW Cycle Width (Mechanical Degrees)
0	Factory Use Only						1	360.00
1	Factory Use Only						2	180.00
2*	12	14	4096	16384	0.088	0.022	3	120.00
3*	11	13	2048	8192	0.176	0.044	4	90.00
4*	10	12	1024	4096	0.352	0.088	5	72.00
5*	9	11	512	2048	0.703	0.176	6	60.00
6	8	10	256	1024	1.406	0.352	7	51.43
7	7	9	128	512	2.813	0.703	8	45.00
8	6	8	64	256	5.625	1.406	9	40.00
9	5	7	32	128	11.250	2.813	10	36.00
10	4	6	16	64	22.500	5.625	11	32.73
11	3	5	8	32	45.000	11.250	12	30.00
12	2	4	4	16	90.000	22.5	13	27.69
13	1	3	2	8	180.0	45.0	14	25.71
14	0	2	1	4	360.0	90.0	15	24.00
15	n/a	n/a	n/a	n/a	n/a	n/a	16	22.50

* Recommended use for TMR primary channel only.

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INDEX PULSE

The index pulse I (or Z in some descriptions) marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the I pulse has four widths, defined by the ABI_INDEX_MODE EEPROM field (extended: 0x25 [13:12]):

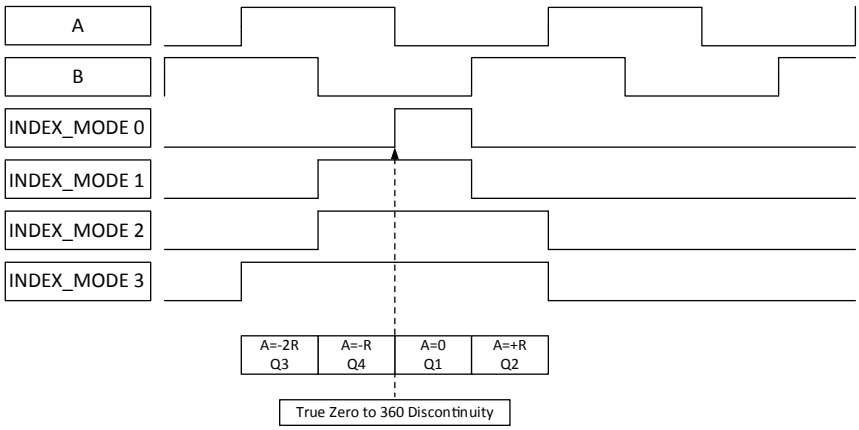

Figure 7: Index Pulse

ABI COUNT-UP FOLLOWING POWER-UP

ABI interface can be configured to communicate the current absolute angle position at power-on. The behavior at start-up is the following.

- During t_{PO_D} the interface is determined by the error reporting on ABI and PWM
  - Depending on the error reporting mode and PWM frequency, this state may require ≈16 ms to clear
- The interface will catch-up with the actual measured angle by moving in a positive or negative direction, whichever is faster. The time for catching up is at most:

$$t_{SETTLE(MAX)} = \frac{180°}{R} \times \text{ABI\_SLEW\_TIME}$$

- After catching up with the measured angle, the sensor will operate normally.

If ABI_SLEW_RATE is set to 0, there is no catch-up phase. The output will jump to the final position immediately.

When ABI_SLEW_RATE is non-zero, the ABI output will automatically count up to the current angle following any power-cycle, reset, or error state (if ABI error reporting is enabled).

ABI count-up following a power-cycle or reset may be disabled by setting ABI_SR_DLY_EN (extended 0x3D [24]), provided ABI error reporting is enabled.

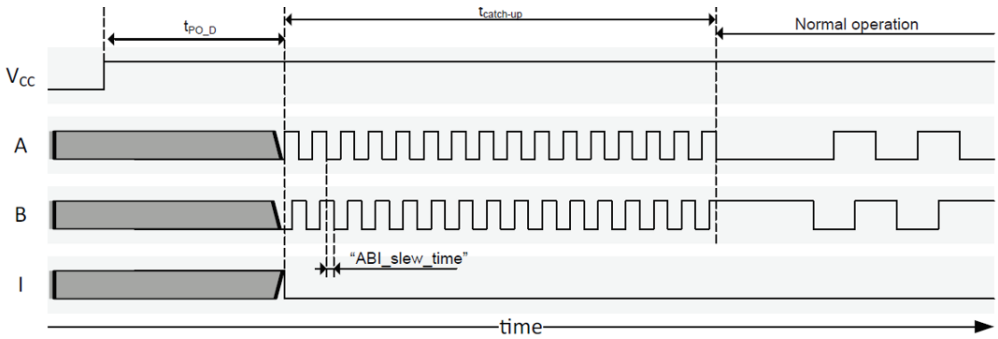

Figure 8: ABI Startup Behavior

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ZERO DEGREE POSITION INDICATION

The edge of the index pulse corresponding to the zero position, as observed by the sensor, will change based on rotation direction, as shown in Figure 9.

With the magnet rotating such that the observed angle is increasing, the 0° position will be indicated by the rising edge of the Index pulse. If the magnet is rotated in the opposite direction (or if ROT_DIR_P and ROT_DIR_S are changed) to produce a decreasing angle value, the 0° position will be represented by the falling edge of the Index pulse.

The ABI resolution and I pulse mode selection (described above) determine the width of the Index pulse and the corresponding shift in zero position indication.

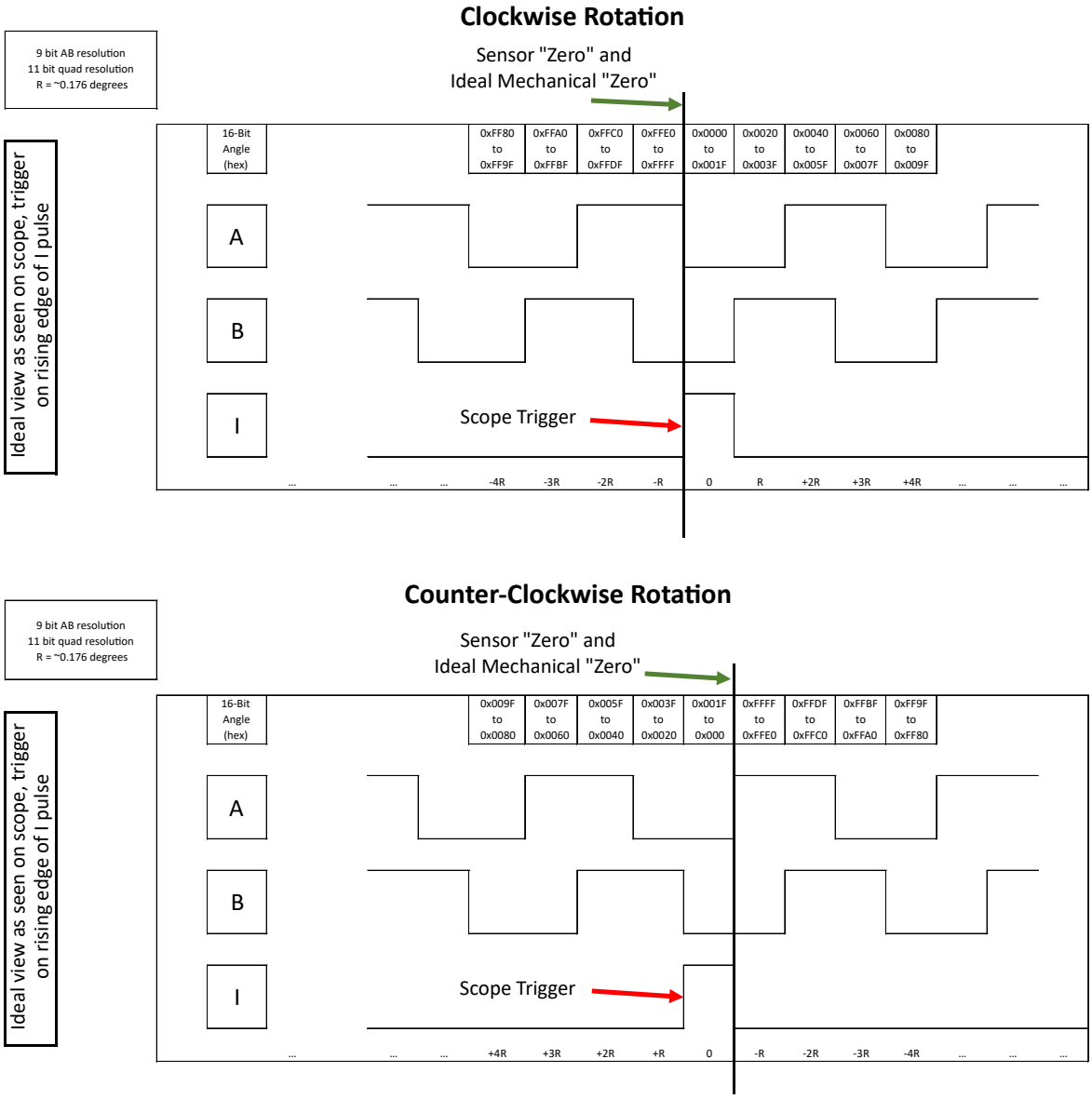

Figure 9: Index Pulse Corresponding to Zero Position

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SLEW RATE LIMITING FOR ABI

Slew rate limiting feature may be used to reduce quadrature state errors. The feature is enabled by setting a non-zero value to the parameter ABI_SLEW_RATE (extended: 0x25 [11:6]). The slew time sets the minimum amount of time that the output must remain in its current state before changing to the next state. This prevents the output from skipping states and can ensure controllers are able to read the state before it changes. This option separates the sensor's observed angle change from the ABI output rate and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby "skipping" one or more quadrature states. In this case, the slew rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output catches up with the angle samples, at which point the normal sample rate output resumes. This skipping will most likely occur either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs. The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation would not on average require ABI transitions greater than the angle sample rate.

In both cases, the ABI output will correctly track the rotation position; however, the speed of the ABI edges will be accomplished at the slew rate limit set in EEPROM. Whenever slew rate limiting occurs, the SLR flag (primary: 0x0E [4]) asserts to inform the system of the occurrence.

Figure 4 illustrates the difference between a bad ABI without slew rate limiting and the corrected output via slew rate limiting.

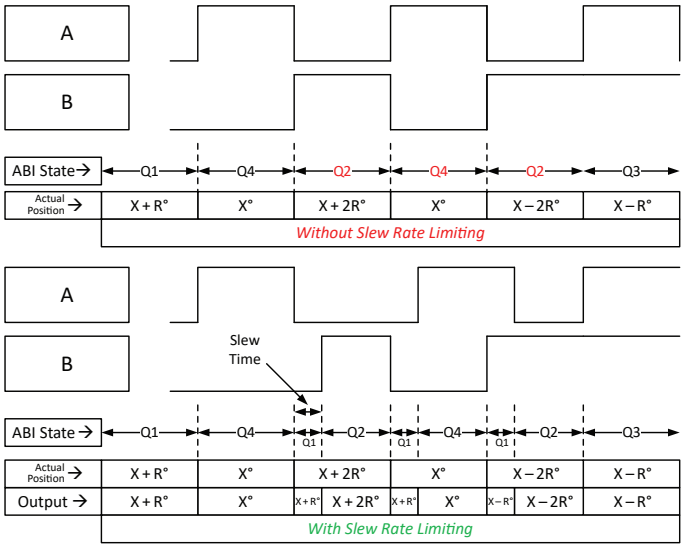

Figure 10: Slew Rate Limiting

EFFECTIVE SPEED OF SLEW TIME

When slew rate limiting occurs, the ABI update rate is no longer dependent on the observed rotation rate, but instead occurs at a period set by the following EEPROM parameters. This change in the edge rate is observed as a change in the target velocity, and this perceived velocity depends on the following parameters:

- ABI_SLEW_RATE (extended: 0x25 [11:6])
- ABI_UVW_RESOLUTION (extended: 0x25 [5:2])

Table 4 shows the equivalent RPMs for select combinations of slew time and ABI resolution.

When designing a system, it is important to note these RPMs will occur for any change in rotation direction (i.e., motor transitioning from CW to CCW rotation), when both hysteresis and ABI slew rate limiting are enabled, as the IC back fills the ABI edges for the programmed hysteresis window ANGLE_HYST (extended: 0x3E [25:23]).

Table 4

EEPROM Setting		Equivalent Velocity (RPM) based on AB Quadrature Resolution		
ABI_SLEW_RATE (Decimal)	Slew Time (µs)	12-bit Quadrature	11-bit Quadrature	10-bit Quadrature
1	0.25	58,593.8	117,187.5	234,375.0
2	0.375	39,062.5	78,125.0	156,250.0
3	0.5	29,296.9	58,593.8	117,187.5
4	0.625	23,437.5	46,875.0	93,750.0
5	0.75	19,531.3	39,062.5	78,125.0
6	0.875	16,741.1	33,482.1	66,964.3
7	1	14,648.4	29,296.9	58,593.8
8	1.125	13,020.8	26,041.7	52,083.3
…	…	…	…	…
62	7.875	1,860.1	3,720.2	7,440.5
63	8	1,831.1	3,662.1	7,324.2

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Brushless DC Motor Output (U,V,W)

The A33115 features U, V, and W output signals for stator commutation of brushless DC (BLDC) motors. The output is mode-selectable for 1 to 16 pole-pairs. The BLDC signals (U, V, and W) are generated based on the quantity of pole-pairs and on angle information from either the primary or secondary channel.

The U, V, and W outputs switch when the measured mechanical angle crosses the value where a change should occur. If hysteresis is used, then the UVW edges will update based off the rotation direction and hysteresis window. Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. Figure 11, Figure 12, and Figure 13 below show the U, V, and W example waveforms for three and five pole-pair BLDC motors.

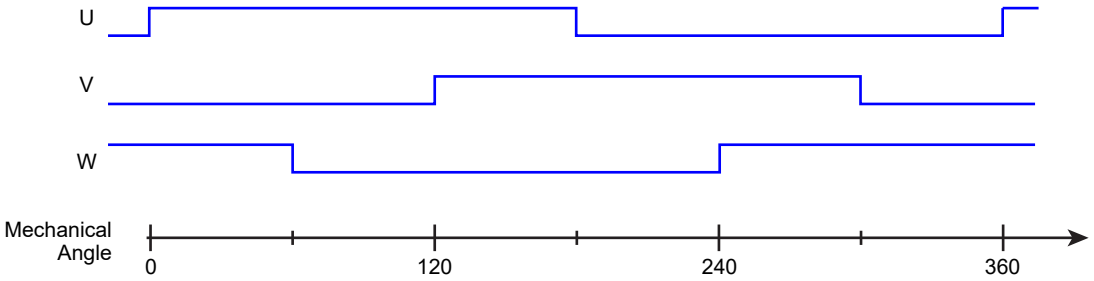

Figure 11: U, V, W Outputs for a 1 Pole-Pair BLDC Motor

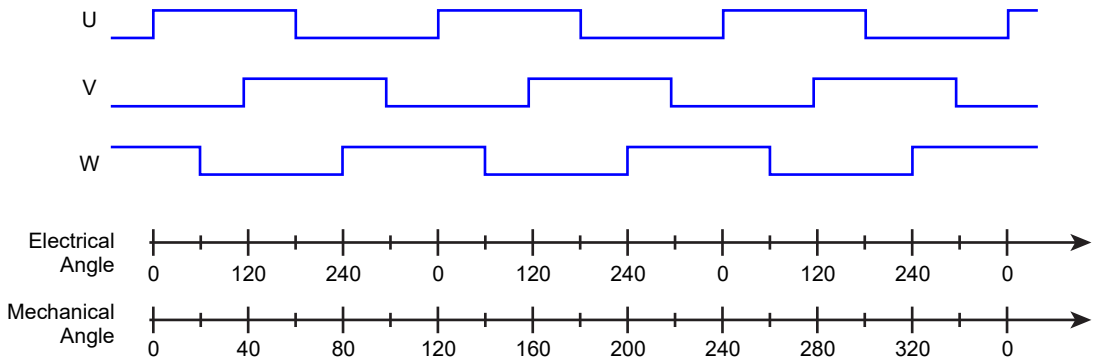

Figure 12: U, V, and W Outputs for Three Pole-Pair BLDC Motor

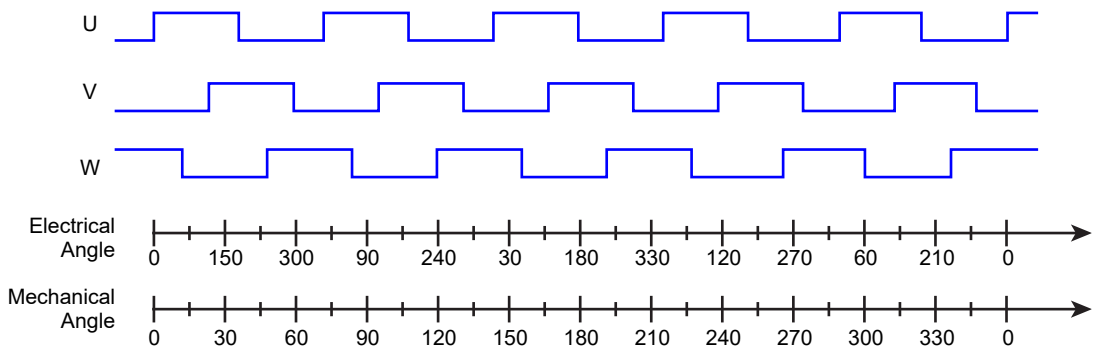

Figure 13: U, V, and W Outputs for Five Pole-Pair BLDC Motor

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Table 6: UVW Pole Pair Settings

ABI_UVW_RESOLUTION (hex)	Quantity of Pole-Pairs	Cycle Width (Mechanical Degrees)
0x0	1	360.00
0x1	2	180.00
0x2	3	120.00
0x3	4	90.00
0x4	5	72.00
0x5	6	60.00
0x6	7	51.43
0x7	8	45.00
0x8	9	40.00
0x9	10	36.00
0xA	11	32.73
0xB	12	30.00
0xC	13	27.69
0xD	14	25.71
0xE	15	24.00
0xF	16	22.50

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. The parameter ANGLE_HYS (extended: 0x3E [25:23]) defines the width of an angle window at 16-bits. Mathematically, the width of this window in degrees is:

$$Angle\ Hyseteresis = \frac{360}{2^{16}} \times 2^{(ANGLE\_HYS+1)}$$

The parameter ANGLE_HYS is a 3-bit EEPROM field, allowing a range of ≈0.01° to ≈1.41° of hysteresis to be applied. The hysteresis compensated angle is applied to the UVW/ABI output. This same angle populates the ABI_UVW_ANGLE field (primary: 0x16 [15:0]) within the primary serial register space and may be read via SPI.

The effect of the hysteresis is shown in Figure 14. The current angle position as measured by the sensor is at the “head” of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the hysteresis-compensated angle is equal to the channel angle output, minimizing latency. If the sensor angle reverses direction, the hysteresis-compensated angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the head was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or head for the purposes of hysteresis, is reported by the parameter ROT_H (primary: 0xE [1]).

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle will skip consecutive resolution steps.
   A. To prevent skipped ABI steps, a non-zero slew rate should be set whenever hysteresis is applied.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle will tend to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current head) rather than to the average position of the jitter.

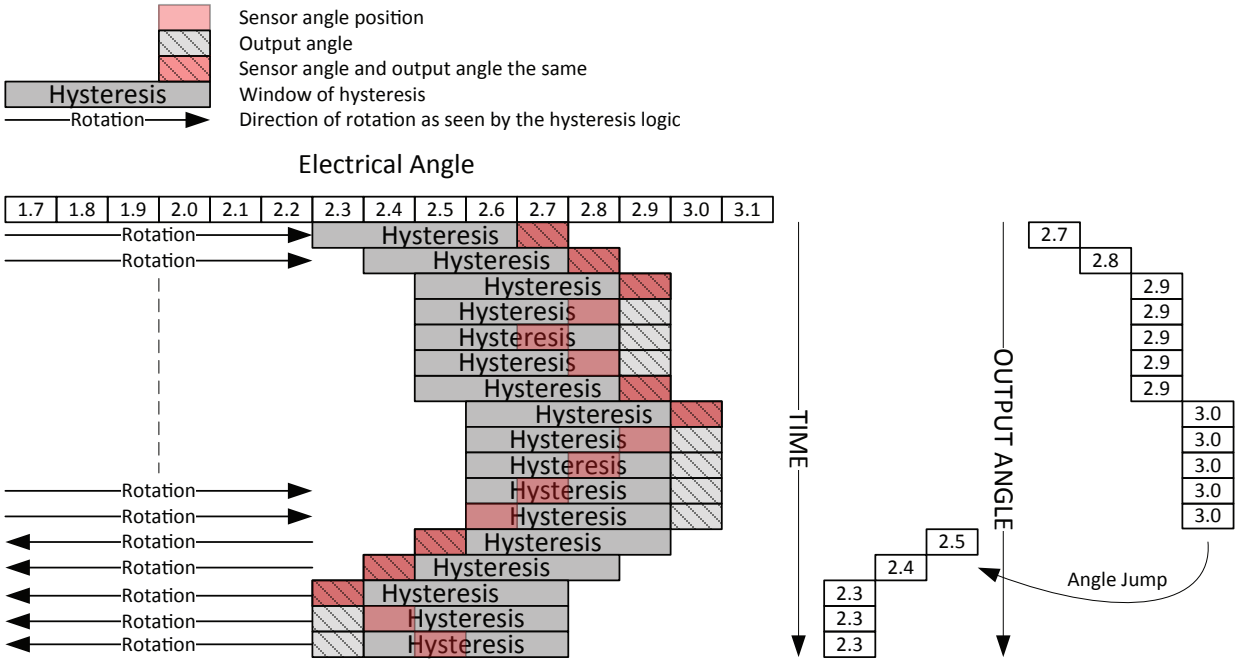

Figure 14

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Low Power Mode

The A33115 Low Power Mode (LPM) feature is a special operating mode to continue to monitor turns count information at reduced angle resolution and power. In LPM operating mode, the dedicated signal path cycles between the wake state, for angle sampling, and sleep state, for minimal power consumption. Low power mode is only entered if all of the following conditions are met:

• The SPI pins (SCLK, MOSI, CSN) at low logic level, AND

• Low Power Mode is enabled, LPM_DIS_C (extended: 0x24 [6]) = 0

In Low Power Mode (LPM), the IC does not provide angle readings over the available SPI, Manchester, ABI/UVW, or PWM interfaces, the majority of the analog and digital circuitry are powered down, and the sensor IC periodically cycles between LPM wake and sleep states. For most of the time, the sensor IC is held in a lower power quiescent current sleep state. In this state, the IC consumes minimal power to retain the turns count information.

Periodically, the IC enters the awake state. In this state, the turns count is updated via the low power VH signal paths.

STATE TRANSITIONS WITHIN LOW POWER MODE

The SPI input pins are used as the primary arbiter of low power-mode. When all three SPI pins inputs (MOSI, SCLK, CSN) are pulled low the sensor enters the LPM mode.

In the wake state, the magnetic position is sampled and compared to the previous angle reading. Once the angle sample is complete, the IC enters LPM sleep state. In the sleep state, the low-frequency oscillator remains active along with a digital counter to monitor the sleep period and logic to detect the state of the SPI pins. Expiration of the sleep counter transitions the sensor from sleep to wake state, and a new angle sample is taken.

If a logic high on any SPI input is observed, Low Power Mode is exited.

AVERAGE CURRENT CONSUMPTION IN LPM

Assuming the sensor is moving between the two LPM states in a periodic manner, the effective current draw observed from the system is the average of the two different current consumptions, weighted by the time of each state.

$$I_{CC(AVGlp)} = \frac{t_{LPsleep}}{t_{total}} \times I_{LPsleep} + \frac{t_{LPwake}}{t_{total}} \times I_{LPwake}$$

where: $t_{total} = t_{LPsleep} + t_{LPwake}$

The wake state time (t_{LPwake}) is fixed. This is the amount of time the internal circuitry requires to accurately acquire the sample the input angle.

The amount of time the sensor spends in sleep mode is programmable via EEPROM.

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Table 7: Low Power Mode Sleep Time Configuration

Typical Values at 25°C				
LPM_SLEEP_TIME	**Sleep Time (us)**	**Average I_{CC} (uA)**	**Input Angle Maximum Velocity (deg. / s)**	**Input Angle Maximum Velocity (RPM)**
0	1700	50	79,412	13,235
1	1900	48	71,053	11,842
2	2500	44	54,000	9,000
3	3500	40	38,571	6,429
4	5000	37	27,000	4,500
5	10000	33	13,500	2,250
6	50000	30	2,700	450
7	100000	30	1,350	225
8	500	100	270,000	45,000
9	600	88	225,000	37,500
10	700	80	192,857	32,143
11	800	74	168,750	28,125
12	900	69	150,000	25,000
13	1000	65	135,000	22,500
14	1200	59	112,500	18,750
15	1500	53	90,000	15,000

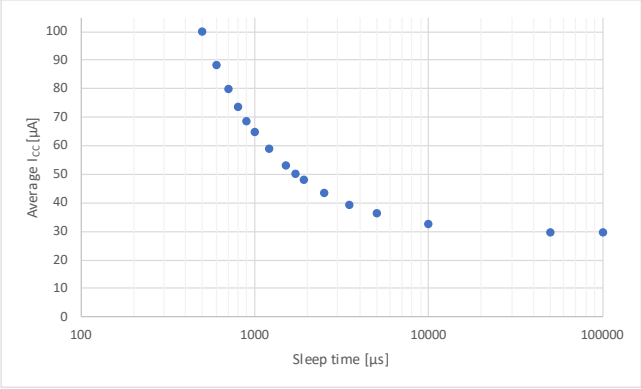

Figure 15: Low Power Mode Typical Average I_{CC} vs. Sleep Time

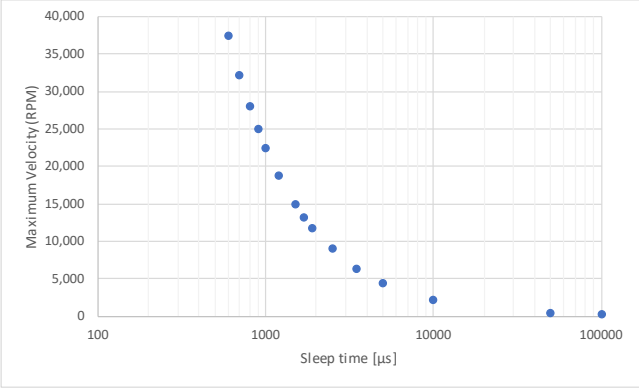

Figure 16: Low Power Mode Maximum Velocity vs. Sleep Time

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Turns Counting and Low Power Mode

Certain automotive angle sensing applications require the ability to track angular position, even in key-off conditions. In the key-off state, most voltage regulators in the vehicle are not operational. Therefore, sensors that must operate in the key-off state are often powered directly from the vehicle battery (12 V). Examples of such applications include:

- Seat-belt passive safety systems
- EPS motor position

Often, these motor and seat-belt systems are geared down so that multiple angle sensor rotations need to be counted by the angle sensor IC. For this reason, the A33115 includes a circuit that counts the rotational turns of a magnet. When sensor ICs are connected to the vehicle battery, it is often desirable to operate in low-power mode during a key-off conditions, to reduce the power draw on the battery. Also, the sensor IC is often required to track the turns-count of the magnet in the same key-off conditions. To support this need the A33115 features, a Low Power Mode during which the IC monitors and maintains a turns count. This allows the system to accurately and consistently track steering wheel position or seatbelt extension in a key-on or key-off condition. Traditionally, this key-off requirement is achieved by a combination of relatively complex mechanical and electronic components. The A33115 features help reduce system-level complexity and eliminate many system components by performing both the absolute angle measurement and the tracking of turns-count, while maintaining low battery power consumption at vehicle key-off.

During normal operation the turns counter logic tracks the magnet position and updates a counter to track angle in 90-degree increments. The primary turns-count updates based on the absolute angle measured by the primary channel and the secondary turns-count updates based on absolute angle measured by the secondary channel. A hysteresis of ±5.625° is applied at the incremental boundaries. For example, if the current angle is 45° the turns-count increments when the angle increases above approximately 96°, and decrements when the angle decreases below approximately –6°. The parameters TC_HYST_DIS_P (extended: 0x27 [12]) and TC_HYST_DISP_S (extended: 0x32 [12]) are available to disable the turns count hysteresis feature.

The turns-count value is reported in the parameters, TURNS_COUNT_P (primary: 0x15 [10:0]), TURNS_COUNT_S (primary: 0x1C [10:0]), TURNS_COUNT_LATCH_P (primary: 0x1B [10:0]), TURNS_COUNT_LATCH_S (primary: 0x1D [10:0]). The turns counter saturates at +1023 and –1024 in 90-degree increments. If a counter register saturates, the Turns Count error flags, TCO_ERROR_P (primary: 0x15 [12]), TCO_ERROR_S (primary: 0x1C [12]), TCO_ERROR_LATCH_P (primary: 0x1B [12]), and TCO_ERROR_LATCH_S (primary: 0x1D [12]), assert and stay asserted until the turns counter register is reset via the Control register.

During Low Power Mode, a dedicated low power signal path monitors the input angle to determine and keep track of the turns-count, to within the Turns Count resolution. The design minimizes the amount of logic that is drawing power, allowing for efficient turns count tracking during battery-operated low-power modes. The A33115 periodically measures the magnet position and updates the turns-count. If the angle changes by ≥ 180° within a sleep period, the direction change is ambiguous and may be interpreted as a rotation in the opposite direction. Therefore, if the velocity exceeds the maximum possible for the configured LPM sample rate, sample-to-sample delta can be greater than the maximum low power angle delta and may result in a loss of accurate turns count.

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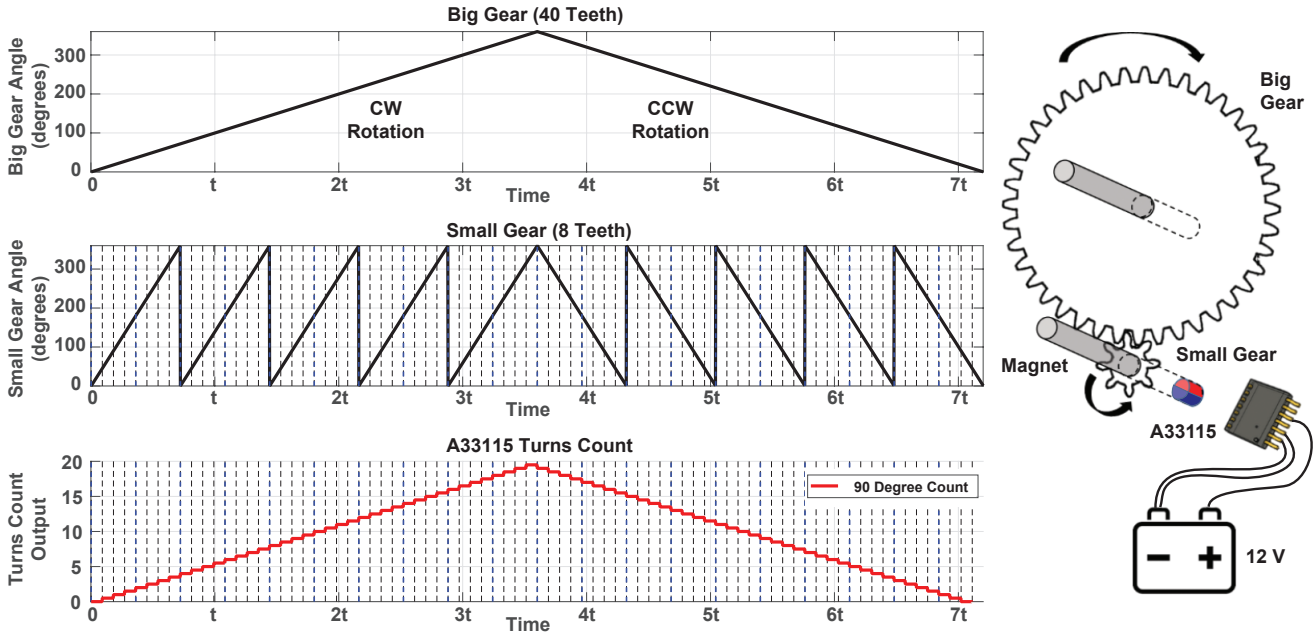

Figure 17: Turns Count Example Application

Turns Count Reset

The A33115 primary and secondary turns counter reset after a reset event. The external controller may invoke a reset using the CTRL register (primary: 0xF)). Following a reset, the primary and secondary turns count initialize according to the parameters TURNS_CNT_INT_P (extended: 0x3E [12]) and TURNS_CNT_INT_S (extended: 0x3F [12]). The parameters configure the turns count registers to initiate at zero or a value between zero and three, corresponding with the quadrant of the initial angle reading. All incremental counts are tracked relative to the initial point, as measured by the turns count logic. Note it is recommended that the parameters TURNS_CNT_INIT_P and TURNS_CNT_INIT_S are set to the same value.

Transport Mode

Transport mode is effectively an additional sleep mode feature of the A33115, but with the Low Power Mode Sleep State Oscillator disabled such that no turns counting occurs. To invoke transport mode, the parameter TRANSPORT_EN (extended: 0x24 [5]) is set. Then, when low power mode is enabled, (SPI inputs held low), transport mode is entered. As soon as one of the incoming SPI lines is high, the A33115 will wake up again. Transport mode is disabled by setting TRANSPORT_EN to a value of logic zero. When the TRANSPORT_EN bit is set in shadow memory to a logic value of one (extended: 0x64 [5]) and the corresponding EEPROM bit is set to a logic value of zero the bit will clear after exiting transport mode.

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Linearization Feature

The A33115 contains sixteen movable segment linearization for both the primary and secondary signal paths. Linearization allows for the conversion of the sensor measured magnetic field data into a customer desired output. This can be used to correct minor imperfections in the magnet or mounting tolerances.

Linearization converts the electrical angle (that sensed by the IC) into a corrected output angle. Typically, this is used to align the electrical angle to the mechanical angle (the actual magnet position).

The IC performs linearization by taking the measured electrical angle and adding / subtracting a correction factor. This correction factor will differ over electrical angle and is based on linearization coefficients stored in EEPROM. There are 16 coefficients, or Y entries (16 for each primary and secondary channels), corresponding to electrical angles chosen by 16 angle entries for the X entries (see Figure 18 below). For electrical angles not matching an entry in the EEPROM table, the correction factor is calculated by linearly interpolating between the two closest coefficients.

The Y Linearization EEPROM fields (LINT8- LINT23) are 11-bit signed values, each coefficient has a range of –1024 to 1023 LSB, corresponding to a correction of –22.50 to +22.49 degrees.

The 16 X linearization entry values are stored within 8 EEPROM fields (LINT00 through LINT07), each field containing two X values. The LINT0-7 EEPROM words are 12 bits, where the lower 6-bit word contains X_{2i} and upper 6-bit word contains $X_{(2i + 1)}$, with i ranging from 0 to 7. The set must satisfy $X_i < X_{(i + 1)}$. Each X location may range from 0° to 360° in 64 steps, or 5.625° resolution.

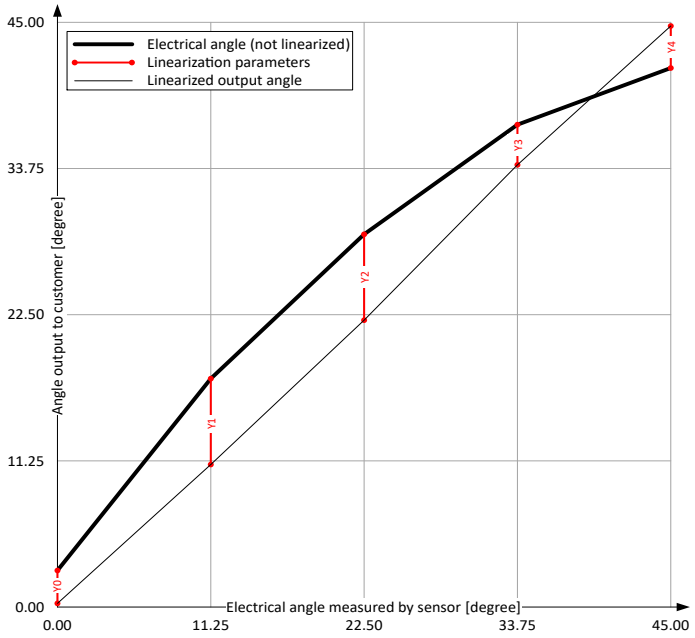

Figure 18

For example, the lower 6 bits in LINT0 correspond to X entry 0 and the upper 6 bits of LINT0 correspond to X entry 1. The angle value for X entry 0 must be less than the angle value for X entry 1.

Figure 18 is shown as an example of a nonlinear curve that is corrected by the sensor. In this example, the Y values contained within EEPROM fields LINT08, LINT09, LINT10, and LINT11 are positive numbers, while the Y value within lint12 is a negative number. The X entry 0 is equal to 0 degrees, X entry 1 is 11.25 degrees, X entry 2 is 22.5 degrees, X entry 3 is 33.75 degrees, and X entry 4 is 45 degrees.

Table 8

EEPROM Field [1]	Contents
(PRIM)_LINT00	[X1, X0]
(PRIM)_LINT01	[X3, X2]
(PRIM)_LINT02	[X5, X4]
(PRIM)_LINT03	[X7, X6]
(PRIM)_LINT04	[X9, X8]
(PRIM)_LINT05	[X11, X10]
(PRIM)_LINT06	[X13, X12]
(PRIM)_LINT07	[X15, X14]
(PRIM)_LINT08	[Y0]
(PRIM)_LINT09	[Y1]
(PRIM)_LINT10	[Y2]
(PRIM)_LINT11	[Y3]
(PRIM)_LINT12	[Y4]
(PRIM)_LINT13	[Y5]
(PRIM)_LINT14	[Y6]
(PRIM)_LINT15	[Y7]
(PRIM)_LINT16	[Y8]
(PRIM)_LINT17	[Y9]
(PRIM)_LINT18	[Y10]
(PRIM)_LINT19	[Y11]
(PRIM)_LINT20	[Y12]
(PRIM)_LINT21	[Y13]
(PRIM)_LINT22	[Y14]
(PRIM)_LINT23	[Y15]

[1] Linearization table entries are listed as (PRIM) for primary channel. EEPROM entries also exist for the secondary channel.

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DEVICE PROGRAMMING INTERFACES

The A33115 can be programmed in two ways:

- Using the *SPI interface* for input and output
- Using a *Manchester protocol* on the PWM pin to send and receive data

The A33115 does not require special supply voltages to write to the EEPROM.

All accessible fields of the IC may be read and written using both protocols. If EEPROM locking is used, write access using either protocol may be limited.

Interface Structure

The A33115 consists of two memory blocks: Primary serial registers (direct memory), and extended memory Shadow memory, EEPROM, and some miscellaneous volatile registers. The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information (for example, angle data, warning flags, field strength, and temperature). All forms of communication (including the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers provide data and address location for accessing extended memory locations. Accessing these extended locations is done in an indirect fashion: the controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed and the result is again presented in the primary interface.

This concept is shown in Figure 19 below.

For writing extended locations, the primary interface registers INDIRECT_WR_ADDRESS (primary: 0x1), INDIRECT_WR_DATA_MSB (primary: 0x2), and INDIRECT_WR_DATA_LSB (primary 0x3) are used for writing extended memory locations. INDIRECT_WR_ADDRESS holds the address of the target extended memory location to be written. INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_WR_STATUS (primary: 0x4) register is used for commands and status information. Refer to the section “Read Transaction from EEPROM” for further information and other register fields associated with indirect memory transactions.

For reading extended locations, the primary interface registers INDIRECT_RD_ADDRESS (primary: 0x5), INDIRECT_RD_DATA_MSB (primary: 0x7), and INDIRECT_RD_DATA_LSB (primary 0x8) are used for reading extended memory locations. INDIRECT_RD_ADDRESS holds the address of the target extended memory location to be read. INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_RD_STATUS (primary: 0x6) register is used for commands and status information. Refer to the section “Read Transaction from EEPROM” for further information and other register fields associated with indirect memory transactions.

For more information on EEPROM and shadow memory read and write access, see EEPROM and Shadow Memory section.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the following sections.

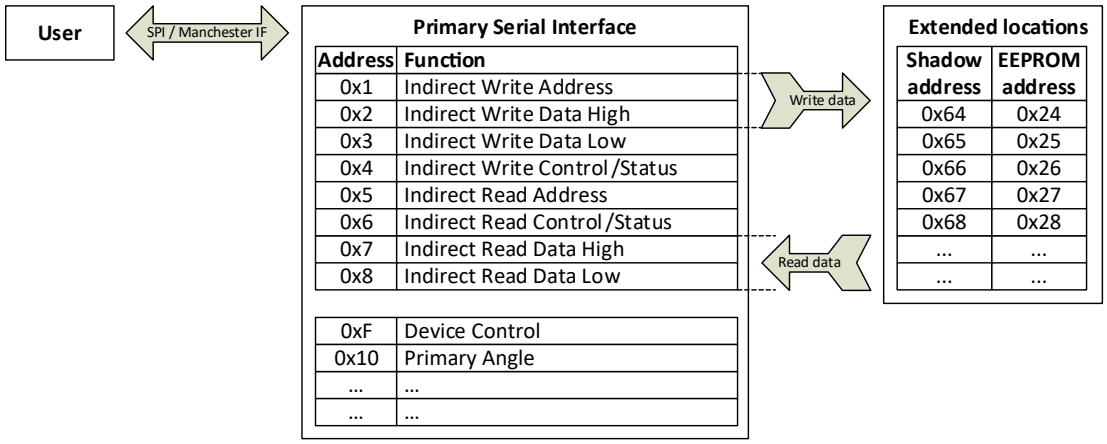

Figure 19: Serial Registers allow access to extended memory (EEPROM and Shadow)

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SPI

The A33115 provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1). For the A33115, the SPI interface is also used to control entering and leaving of the low power and transport modes.

The sensor responds to commands received on the MOSI (Controller-Out Peripheral-In), SCLK (Serial Clock), and $\overline{CS}$ (Chip Select) pins, and outputs data on the MISO (Controller-In Peripheral-Out) pin. All three input pins are 3.3 V SPI compatible. MISO output voltage level will conform to 3.3 V SPI levels.

TIMING

The interface timing parameters from Table 9 are displayed in the Figure 21 and Figure 22 below.

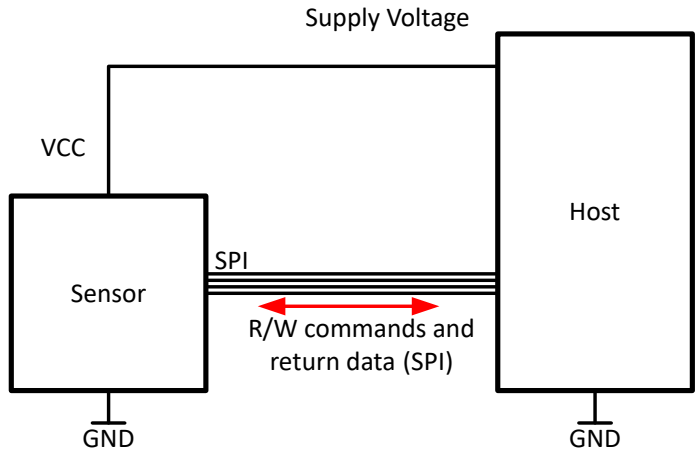

Figure 20: SPI Interface Programming Setup

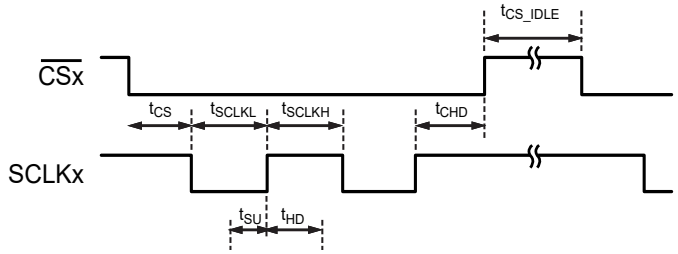

Figure 21: SPI Interface Timings Input

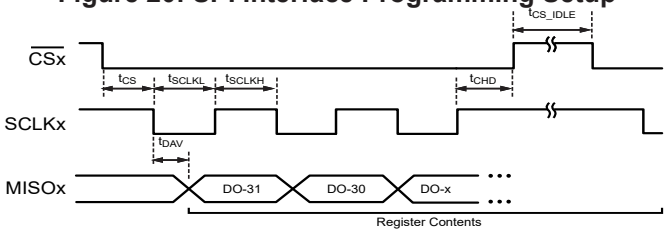

Figure 22: SPI Interface Timings Output

Table 9: SPI Interface

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC} (defines t_{SCLKL} t_{SCLKH})	40	–	60	%
SPI Frame Rate	t_{SPI}		3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge	–	30	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [1]	C_L	Load on Digital output pin MISO and ABI / UVW pins, with $f_{SCLCK} \leq 10$ MHz	–	–	20	pF
		Load on Digital output pin MISO and ABI / UVW pins, with $f_{SCLCK} \leq 1$ MHz	–	–	50	pF

[1] Parameter is not measured at final test. Limits based on design simulations.

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MESSAGE FRAME

The SPI interface uses a 32-bit packet and is designed to provide a high level of confidence for data for data integrity. There are three possible SPI transactions: Write Cycle, Read Request (from the controller) and Read Response (from the peripheral).

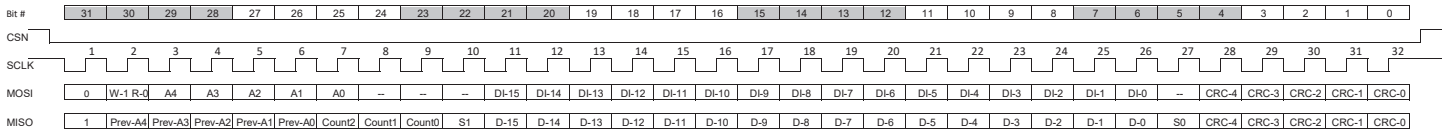

Figure 23: 32-Bit SPI Frame

Write Cycle or Read Request Cycle

The write cycle and read request frame structure is shown in Figure 24 and Figure 25. The frames consist of the following:

- Start Bit [31]: Static bit with a logic value of 0. This bit is not used in the CRC calculation.
- R/W[30]: Read/Write bit set to a logic value of 1 to signify a write cycle and 0 to signify a read request.
- Address [29:25]: Address bits for accessing primary registers
- Data[21:6]: Data bit for writing primary registers. Considered not applicable for a read request.
- CRC [4:0]: CRC bits calculated on the frame bits [30:5].
- Not applicable bits [24:22, 5]: Value can be 1 or 0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	Address [4:0]					—			Data [15:0]																—	CRC [4:0]				

Figure 24: Write Cycle SPI Frame

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	Address [4:0]					—			Data [15:0] (Not Applicable)																—	CRC [4:0]				

Figure 25: Read Request Cycle Frame

Read Response Cycle

The read response cycle frame, sent from the IC, as shown in Figure 26. The frame consists of the following:

- Start Bit [31]: Start bit is set to a value of 1. This bit is not used in the CRC calculation.
- Previous Address [30:26]: Register address corresponding to the read request data
- Frame Count [25:23]: Frame counter, increments with each SPI frame.
- S1 [22]: Status/Error Flag
  - Logical OR of all unmasked error flags. Set to 1 if any unmasked error flag is asserted. Will clear once presented on the SPI bus following a read, assuming error condition has cleared.
  - ABI and SLR reported via S1
- S0 [5]: Status/Error Flag
  - Logical OR of all unmasked error flags. Set to 1 if any unmasked error flag is asserted. Will clear once presented on the SPI bus following a read, assuming error condition has cleared.
- Data [21:6]: Data contents from primary register.
- CRC [4:0]: CRC bits calculated over the frame [30:5]

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Previous Address [4:0]						Frame Count [2:0]		S1	Data [15:0]																S0	CRC [4:0]				

Figure 26: Read Response Cycle Frame

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CRC

Each SPI frame includes a 5-bit CRC, calculated using the polynomial: $x^5 + x^2 + 1$ with a seed value of 11111_2.

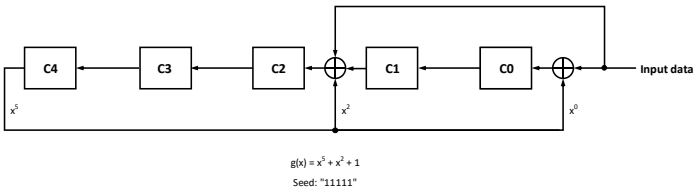

Figure 27: CRC Calculation with Left Shift Register

The outgoing CRC is calculated by the A33115 and transmitted on the MISO pin. The incoming CRC must be calculated by the Controller and included on the MOSI pin. The A33115 checks the CRC on every incoming frame, an invalid frame is ignored. The CRC achieves a hamming distance of 3 for secure data transmission.

The CRC may be calculated with the following Python code:

```
def spi_crc(data_frame):
    """
    SPI CRC: Takes 27 bit input and generates 5 bit CRC.
    Polynomial = x^5 + x^2 + 1
    Initial CRC value set to all 1s

    Input:
        data_frame: a string representing 27 bit binary data
    """
    crc = list('11111')  #CRC seed = 11111
    # MSB of SPI frame is not used during CRC calculation.
    for j in range(1, 27):
        old_crc = crc
        aux_crc_1 = crc[1]
        aux_crc_4 = crc[4]
        crc[4] = int(old_crc[3])
        crc[3] = int(old_crc[2])
        crc[2] = int(aux_crc_1) ^ int(aux_crc_4) ^ int(data_
frame[j])
        crc[1] = int(old_crc[0])
        crc[0] = int(aux_crc_4) ^ int(data_frame[j])
    #flips calculated CRC around to obtain value in proper
order
    crc = crc[::-1]
    return crc
```

A MATLAB implementation of the CRC is:

```
function [output_binary_word,CRC]=Allegro_CRC_x5_x2(input_
binary_word)
%% Initialization
CRC=ones(5,1);
%% CRC calculation
for i=1:length(input_binary_word)
    old_CRC=CRC;
    aux_CRC2=CRC(2);
    aux_CRC5=CRC(5);
    CRC(5)=old_CRC(4);
    CRC(4)=old_CRC(3);
    aux=xor(aux_CRC2,aux_CRC5);
    CRC(3)=xor(aux,str2num(input_binary_word(i)));
    CRC(2)=old_CRC(1);
    CRC(1)=xor(aux_CRC5,str2num(input_binary_word(i)));
end
%% Outputs
CRC=[num2str(CRC(5)) num2str(CRC(4)) num2str(CRC(3))
num2str(CRC(2)) num2str(CRC(1))];
output_binary_word=[input_binary_word CRC];
```


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MISO Response on Receipt of Bad CRC

Following receipt of a bad CRC the IC will return a special SPI packet to indicate to the Controller a problem has occurred. Changes to the MISO packet are:

- Previous Address [30:26]: Set to 0x11.
- Data[21:6]: Contains the contents of the ERROR_0 register (primary: 0x11).
  - Note: The IER flag, within the response packet, is not set on receipt of a single corrupted SPI frame; however, a read of the error register (primary: 0x11) will show the IER flag asserted.

This packet is shown in Figure 28.

MISO Response Following a Write

Following a write operation, the MISO packet will contain predetermined values within the Previous Address and Data Fields.

- Previous Address [30:26]: Set 0x10
- Data [21:6]: Primary Angle Value (ANGLE_OUT_P from primary 0x10)

This packet is shown in Figure 29.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	1	Frame Count [2:0]			0	IER	XEE	BSY	SME	EUE	ESE	POF	OVC	UVC	MSH	MSL	SMM	OFE	SAT	TSE	VCE	0	CRC [4:0]				

Figure 28: First MISO Response Following Bad CRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	0	Frame Count [2:0]			S1	ANGLE_OUT_P																S0	CRC [4:0]				

Figure 29: MISO Response Following a Write Operation

SPI Power On Response

After a reset event, the S1 and S0 bits are set to 1 until the ANGLE_RDY (primary: 0xE [0]) bit is set, and no other errors are locked in. This is an indication to the controller that the signal chain has stabilized, and angle is valid. In addition, transitioning S1 and S0 from a 1 to a 0 allows for the detection of a stuck diagnostic bit. The full contents of the first SPI return packet following a power-on will be 0x80400021.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1	Address					Frame Cnt			S1	Data																S0	CRC				
Binary	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Figure 30: Initial SPI Response Frame Following Power-On

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Manchester Interface

To facilitate addressable device programming when using the unidirectional PWM, ABI, or UVW protocols, without requiring four additional SPI connections, the A33115 incorporates an additional serial communication using the PWM line.

This interface allows an external controller to read and write registers in the A33115 EEPROM and volatile memory. The point-to-point communication protocol is based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first.

The setup for communication using the Manchester interface is given in Figure 31.

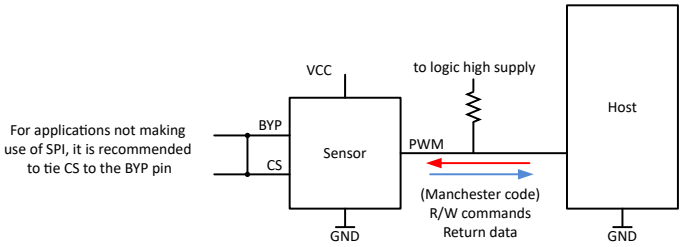

Figure 31: Manchester Programming Interface Setup

The Manchester interface allows programming and readout with a minimal number of pins involved. A valid auxiliary request command recognized by the sensor places the device into communications mode. In this mode, serial data is transmitted or received on the PWM pin. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate requested by the Controller. The high and low logic level for the Manchester serial data is determined by the Manchester High and Low Voltage parameters. The PWM output consists of an open drain type circuit. A sufficient pull-up resistor and external supply voltage are required.

Entering Manchester Communication Mode

The A33115 continuously monitors the PWM line for a valid Auxiliary command. The Auxiliary command, shown in Figure 32, is initiated by the main controller pulling the PWM Output line low for at least two PWM periods. When the controller releases the PWM line, there is a limited time window to start transmission of the Manchester Access Code (t_{msgRX}). Once the Access code is received, the A33115 devices enters programming mode, and customer EEPROM/Shadow memory may be read/written.

The communication enable, COMM_E, bit (extended: 0x9E [15]) controls the state of the PWM output. When set to a logic 1 the PWM output is disabled, allowing Manchester communication on the PWM line. Setting COMM_E to 0 re-enables the PWM output, disabling Manchester communication

If PWM is disabled in EEPROM, the Auxiliary Interrupt pulse is not required, simply send the Access Code to enable Manchester communication.

Table 10: Auxiliary Command Parameters

Parameter	Symbol	Description	Min	Max	Units
Hold Time	t_{hold}	PWM, Auxiliary Command	2 × PWM period	–	µs
Edge Detection Time	t_{gate}		0.7	–	µs
Access Code Window	t_{msgRX}		1.4	300	µs

Table 11: Programming Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Bit Rate		Communication rate	4	–	100	kbps
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on V_{OUT}	2.8	–	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on V_{OUT}	0	–	1.2	V

Table 12: Manchester Access Code

Parameter	Description	Value (Hex)
Manchester Access Code	Enables Manchester Communication. PWM output disabled. Enables Extended Reads/Writes.	C4 18 0E 81

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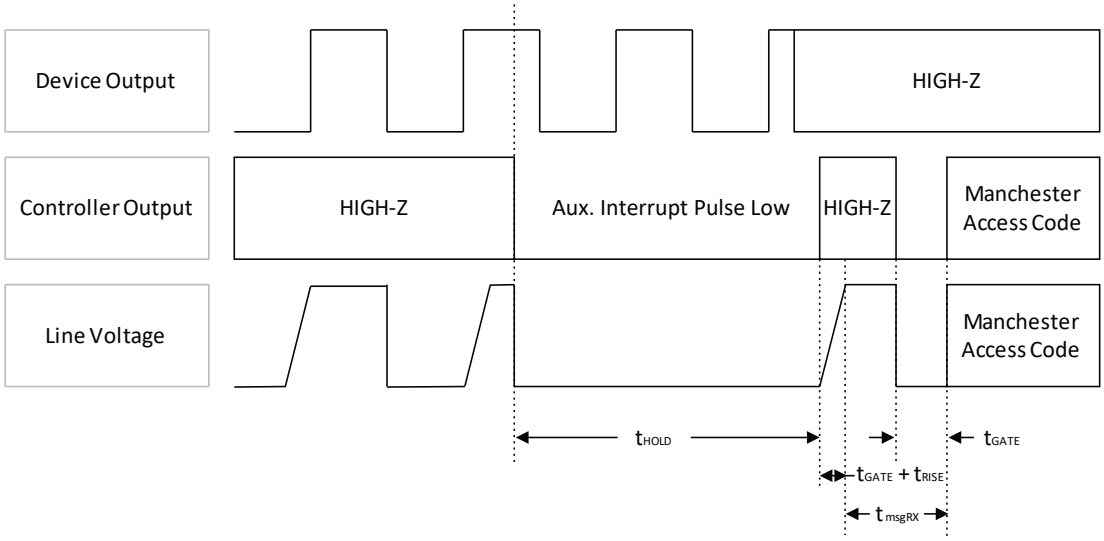

Figure 32: Auxiliary Interrupt Pulse Waveform

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TRANSACTION TYPES

The A33115 receives all Manchester communication commands and responds with data on the PWM pin. Each transaction is initiated by a command from the controller; the sensor does not initiate any transactions. Two commands are recognized: Write and Read.

Manchester Command Frame General Format

The general format of a Manchester command message frame is shown in Figure 33. Serial binary data is encoded using a Manchester encoding scheme, where a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A33115 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 13.

For a Read Request frame, the data bits are omitted. For a Read Acknowledge, the read / write bit and address bits are omitted. The bits are transmitted MSB as shown in Figure 33.

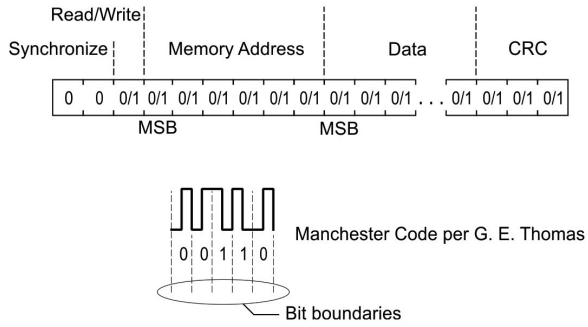

Figure 33: Manchester Message Format

Table 13

Quantity of Bits	Name	Values	Description
2	Synchronization	0	Used to identify the beginning of a serial interface command and communication bit time.
1	Read / $\overline{\text{Write}}$	0	[As required] Write operation
		1	[As required] Read operation
5	Address	0x-0x1F	[Read/Write] Register address (direct memory only)
16	Data	0/1	Write, 16 data bits (direct memory only)
3	CRC	0/1	Bits to check the validity of frame

Manchester Communication CRC

The Manchester serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored by the check). The CRC algorithm is based on the following polynomial and the calculation is represented graphically in Figure 34. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

$$g(x) = x^3 + x + 1.$$

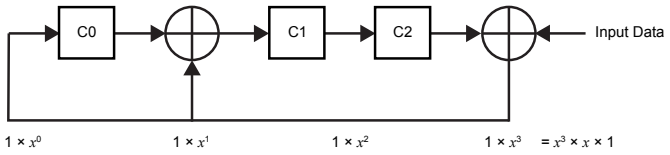

Figure 34: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the manchester command, right justified, does not
include the space for the CRC
// numberOfBits: number of bits in the command not including the 2
zero sync bits at the start of the command and the three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
	bool C0 = false;
	bool C1 = false;
	bool C2 = false;
	bool C0p = true;
	bool C1p = true;
	bool C2p = true;
	uint64_t bitMask = 1;

	bitMask <<= numberOfBits - 1;

	// Calculate the state machine
	for (; bitMask != 0; bitMask >>= 1)
	{
		C2 = C1p;
		C0 = C2p ^ ((data & bitMask) != 0);
		C1 = C0 ^ C0p;

		C0p = C0;
		C1p = C1;
		C2p = C2;
	}

	return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```


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EEPROM AND SHADOW MEMORY USAGE

The A33115 device features include integrated EEPROM to permanently store configuration parameters for operation. EEPROM is customer programmable and retains data, or parameter values, to configure the device for the application requirements. After a reset, or EEPROM write operation, parameter data is copied from EEPROM to shadow (volatile) memory. Parameter data in shadow memory, can be overwritten by performing an extended write to the shadow addresses. Access of device parameters through shadow memory is faster than access through EEPROM. In situations where it is desired to test many parameters quickly before permanently programming, use of shadow memory is recommended. The shadow memory registers have the same format as EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Some bits do not impact device operation and are not copied into shadow memory. Shadow registers do not contain the ECC bits and may have read or write protection restrictions similar to EEPROM.

Enabling EEPROM Access

Reads and writes to indirect memory, EEPROM, and shadow memory are restricted and require an unlock code. The unlock code is written to the primary serial register ACCESS (primary: 0x1E [15:0]). This involves two write commands, which should be executed after each other:

For SPI communication:
Write 0xC418 to register primary 0x1E [15:0]
Write 0x0E80 to register primary 0x1E [15:0]
For Manchester communication:
Write 0xC418 to register primary 0x1E [15:0]
Write 0x0E81 to register primary 0x1E [15:0]

Writing the communication enable bit, COMM_E (extended 0x9E [15]) to a value of 0 or a reset event disables the communications mode.

The access status is indicated by the direct serial register ACCESS. A read of primary 0x1E [1], bit 1, set to a value of 1 indicates the customer unlock code is set.

The customer unlock code is not required for write and read operations to all the direct serial registers.

Device must be unlocked when performing EEPROM margin checking.

EEPROM and Shadow Access Protections

The A33115 contains features to protect against unwanted EEPROM access.

- Setting the EEPROM parameter MEM-LOCK (extended: 0x24 [25:22]) to a value of 0xC (1100 binary) restricts write access to prevent changes the EEPROM registers. Temporary changes to device configuration settings are still possible by writing to the indirect volatile and shadow memory. Note, any changes to the indirect volatile memory are reset after a device reset event. Read access of the EEPROM is still possible.
- Setting the EEPROM parameter MEM-LOCK (extended: 0x24 [25:22]) to a value of 0x3 (0011 binary) restricts write access to prevent changes to EEPROM, indirect volatile, and shadow memory. Once set the parameter settings in indirect memory are read only. Read access is still possible.
- Writes to the MEM-LOCK parameter with the above values are one time access only and are not erasable through subsequent write commands.

Write Transactions to Extended Memory: EEPROM, Shadow, and Volatile

Invoking an extended write access is a three-step process:

1. Write the target extended address to the primary register INDIRECT_WR_ADDRESS (primary: 0x1 [7:0]).
2. Write the desired data, for the target extended register, to the primary registers INDIRECT_WR_DATA_MSB (primary: 0x2 [15:0]) and INDIRECT_WR_DATA_LSB (primary: 0x3 [15:0]). The register INDIRECT_WR_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_WR_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.
3. Execute the extended memory write by setting the extended memory execute write bit, EXW (primary: 0x4 [15]), to a value of 1.

When the bit EXW is set the 32 bits of data contained in INDIRECT_WR_DATA_LSB and INDIRECT_WR_DATA_LSB are written to the indirect memory address specified by INDIRECT_WR_ADDRESS. The status of the write may be interrogated by polling the primary register INDIRECT_WR_STATUS (primary: 0x4). The bit WIP (primary: 0x4 [8]), when set, indicates write transaction in progress. The bit WDN (primary: 0x4 [0]), when set, indicates write transaction done, or complete. The error status bit XEE (primary: 0x11 [15]), when set, indicates an error occurred when executing the write. For example, if a write is attempted without the proper access enabled the XEE bits indicates an error.

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Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the INDIRECT_RD_ADDRESS (primary: 0x5) register (using SPI or Manchester direct access). INDIRECT_RD_ADDRESS is the 8-bit extended address that determines which extended memory address will be accessed.
2. Invoke the extended access by writing the EXR bit (primary: 0x6 [15] with a value of 1. The address specified in INDIRECT_RD_ADDRESS is then read, and the data is loaded into the INDIRECT_RD_DATA_MSB (primary: 0x7) and INDIRECT_RD_DATA_LSB (primary: 0x8) registers.
3. Read the INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB registers (using SPI or Manchester direct access) to get the full data contents of the extended read address. The register INDIRECT_RD_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_RD_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.

EEPROM read accesses may take up to 2 µs to complete. The RDN (primary: 0x6 [0]) bit can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB) registers if the read access is in process (RIP primary: 0x6 [8] = 1), as it could change during the serial access and the data will be inconsistent. It is also possible that an SPI CRC error will be detected if the data changes during the serial read via the SPI interface.

Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, one must address to the Shadow Extended addresses, which are located at an offset of 0x40 above the EEPROM. Refer to the EEPROM Table 14, Table 15, and Table 16 for all addresses.

EEPROM Margin Check

The A33115 contains an EEPROM margin test mode to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with the customer access code. Margining is able to check all logic 1's, logic 0's, or both. The results of the test are reported back in extended memory addresses 0x82 and 0x84. Note that a failure of the margin test does not force the outputs to a diagnostic state or trigger a diagnostics error flag. The following is a step-by-step procedure to verify EEPROM programming.

1. Enable EEPROM access by sending the unlock code to primary address 0x1E.
2. Write a 1 to the MARGIN_START field (volatile 0x84 [0]).
   A. Once started the device will automatically check high/low thresholds of all EEPROM addresses.
3. Read MARGIN_STATUS (volatile 0x84 [4:3]):
   0 = No result.
   1 = Pass. Margin checking completed with no errors.
   2 = Failure detected during margin testing.
   3 = Running. Margin test is running.
4. If a margin failure is detected additional information may be retrieved.
   A. MARGIN_MIN_MAX_FAIL (volatile 0x84 [5]) indicated if a logic high or low failed.
      0 = Margin low threshold failure
      1 = Margin high threshold failure
   B. EE_TEST_ADDR (volatile 0x84 [12:7]) contains the failing address.
5. New EEPROM writes should not be considered valid unless margin testing passes. If a margin failure occurs on a previously modified address, EEPROM can be rewritten and margin checking repeated in an attempt to clear the issue.

See section Extended Memory (Table 15) for more information on EEPROM margining. Time required to verify margin levels across all EEPROM is ≈100 µs.

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PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 14: Direct Serial Interface Registers Bits Map

Address (0x00)	Register Symbol	Read/Write	Primary Addressed Byte (MSB)								Primary Addressed Byte (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	NULL_REG	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x01	INDIRECT_WR_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
0x02	INDIRECT_WR_DATA_MSB	RW	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
0x03	INDIRECT_WR_DATA_LSB	RW	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
0x04	INDIRECT_WR_STATUS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x05	INDIRECT_RD_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_READ_ADDR							
0x06	INDIRECT_RD_STATUS	RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x07	INDIRECT_RD_DATA_MSB	RO	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
0x08	INDIRECT_RD_DATA_LSB	RO	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
0x09	SIN_S_REG	RO	SIN_S															
0x0A	COS_S_REG	RO	COS_S															
0x0B	TEMP12B_S	RW	0	0	0	0	TEMP_OUT_S											
0x0C	SIN_P_REG	RO	SIN_P															
0x0D	COS_P_REG	RO	COS_P															
0x0E	STATUS_REG	ROC	0	0	0	0	0	0	0	0	0	BACK_FROM_LPM	R	SLR	ABI	ACD	ROT_H	ANG_RDY
0x0F	CTRL	RW	0	0	0	0	0	0	0	0	0	0	0	0	FULL_RST	SOFT_RST	TC_WR_EN	TCR
0x10	PRIM_ANGLE	RO	ANGLE_OUT_P															
0x11	ERROR_0	ROC	IER	XEE	BSY	SME	EUE	ESE	POR	OVCC	UVCC	MSH	MSL	SMM_P	OFE_P	SAT_P	TSE_P	VCF_P
0x12	ERROR_1	ROC	IER_R	XEE_R	BYS_R	SME_R	EUE_R	ESE_R	POR_R	OVCC_R	UVCC_R	MSH_R	MSL_R	SMM_S	OFE_S	SAT_S	TSE_S	VCF_S
0x13	TEMP12B_P	RW	0	0	0	0	TEMP_OUT_P											
0x14	FIELD_REG	RO	FIELD															
0x15	TURNS_COUNTER_P	RW	0	0	TCW_ERROR_P	TCO_ERROR_P	0	TURNS_COUNT_P										
0x16	ANGLE_WITH_HYST	RO	ABI_UVW_ANGLE															
0x17	VELOCITY_REG	RO	VELOCITY															
0x18	ACCELERATION_REG	RO	ACCELERATION															

RO: Read only
WO: Write only
RW: Read and write
ROC: Read only and clear on read

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Table 14: Direct Serial Interface Registers Bits Map (continued)

Address (0x00)	Register Symbol	Read/Write	Primary Addressed Byte (MSB)								Primary Addressed Byte (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x19	SEC_ANGLE	RO	ANGLE_OUT_S															
0x1A	SEC_ANGLE_LATCH	RO	ANGLE_OUT_LATCH_S															
0x1B	TURNS_COUNTER_LATCH_P	RO	0	0	TCW_ERROR_LATCH_P	TCO_ERROR_LATCH_P	0	TURNS_COUNT_LATCH_P										
0x1C	TURNS_COUNTER_S	RW	0	0	TCW_ERROR_S	TCO_ERROR_S	0	TURNS_COUNT_S										
0x1D	TURNS_COUNTER_LATCH_S	RO	0	0	TCW_ERROR_LATCH_S	TCO_ERROR_LATCH_S	0	TURNS_COUNT_LATCH_S										
0x1E	ACCESS	RO/WO	ACCESS_KEY		FREE_REG_LOCK_RD	FREE_REG_LOCK_WR	FACT	FACT	CUST_REG_LOCK_RD	CUST_REG_LOCK_WR	FACT	FACT	CUST_EE_LOCK_RD	CUST_EE_LOCK_WR	FACT	FACT	CUST_ACCESS	FACT
0x1F	LOOPBACK_REG	RW	LOOPBACK															

RO: Read only
WO: Write only
RW: Read and write
ROC: Read only and clear on read

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Address 0x00 (NOP) – Null Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RO	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address 0x01 – (INDIRECT_WR_ADDRESS) Extended Write Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
RW	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_ADDR [7:0]:

Target address to be used for an extended memory write. Address ranges:
0x00 - 0x3F: EEPROM (requires ≈ 6.5 ms following execution of a write)
0x40 - 0x7F: Shadow (Volatile)
0x80 - 0x9E: Miscellaneous (Volatile)

Address 0x02 – (INDIRECT_WR_DATA_MSB) Extended Write Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

INDIRECT_WR_DATA_3 [15:8]:
Upper fourth byte of data for an extended write operation, corresponds to bits [31:24] of the extended write address.

INDIRECT_WR_DATA_2 [7:0]:
Third byte of data for an extended write operation, corresponds to bits [23:16] of the extended write address.

Address 0x03 (INDIRECT_WR_DATA_LSB) – Extended Write Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

INDIRECT_WR_DATA_1 [15:8]:
Second byte of data for an extended write operation, corresponds to bits [15:8] of the extended write address.

INDIRECT_WR_DATA_0 [7:0]:
Lower first byte of data for an extended write operation, corresponds to bits [7:0] of the extended write address.

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Address 0x04: (INDIRECT_WR_STATUS) – Extended Write Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXW [15]:

Initiate extended write by writing with a value of 1. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP [8]:

Indicates write in progress when set to 1 .

WDN [0]:

Write operation complete when set to a value of 1, clears when EXW is set to 1.

Address 0x05: (INDIRECT_RD_ADDRESS) – Extended Read Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDRESS							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

INDIRECT_RD_ADDRESS [7:0]:

Address to be used for an extended read. Address ranges:
Extended 0x00 - 0x3F: EEPROM (requires ≈ 2µs)
Extended 0x40 - 0x7F: Shadow (Volatile)
Extended 0x80 - 0x9E: Miscellaneous (Volatile)

Address 0x06: (INDIRECT_RD_STATUS) – Extended Read Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXR [15]:

Initiate extended read by writing with a value of 1. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP [8]:

Read in progress when set to a value of 1.

RDN [0]:

Read operation complete when set to a value of 1, clears when EXR is set to 1.

Address 0x07: (INDIRECT_RD_DATA_MSB) – Extended Read Data High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

INDIRECT_RD_DATA_3 [15:8]:
Upper fourth byte of data for an extended read operation, corresponds to bits [31:24] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_2 [7:0]:
Third byte of data for an extended read operation, corresponds to bits [23:16] of the extended read address after execution of a read operation.

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Address 0x08: (INDIRECT_RD_DATA_LSB) – Extended Read Data Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

INDIRECT_RD_DATA_1 [15:8]:
Second byte of data for an extended read operation, corresponds to bits [15:8] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_0 [7:0]:
Lower first byte of data for an extended read operation, corresponds to bits [7:0] of the extended read address after execution of a read operation.

Address 0x09: (SIN_S_REG) – Secondary sin, y, Channel Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIN_S															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

SIN_S [15:0]:

Digitized value of the Secondary sin, y axis, channel. Value is a 16-bit signed integer.

Address 0x0A: (COS_S_REG) – Secondary cos, x, Channel Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COS_S															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

COS_S [15:0]:

Digitized value of the Secondary cos, x axis, channel. Value is a 16-bit signed integer.

Address 0x0B: (TEMP12B_S) – Secondary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	TEMP_OUT_S											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TEMP_OUT_S [11:0]:

Current ambient temperature from the secondary channel internal temperature sensor. Value is a 12-bit signed integer, where: Temperature (°C) ≈ (Value of TEMP_OUT_S / 8) + 25.0.

Address 0x0C: (SIN_P_REG) – Primary sin, y, Channel Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SIN_P															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

SIN_S [15:0]:

Digitized value of the Primary sin, y, channel. Value is a 16-bit signed integer.

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Address 0x0D: (COS_P_REG) – Primary cos, x, Channel Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COS_P															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

COS_P [15:0]:

Digitized value of the Primary cos, x, channel. Value is a 16-bit signed integer.

Address 0x0E (STATUS_REG) – Device Status Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	BACK_FROM_LPM	reserved	SLR	ABI	ACD	ROT_H	ANG_RDY
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

BACK_FROM_LPM [6]:
Indicates the device has returned from the low power operating mode to normal operation. The bit is set to a value of one after leaving low power mode and the first angle update in normal operating mode. The bit is cleared after a read of the register, STATUS_REG.

Reserved [5]:
Reserved bit. No function.

SLR [4]:

Slew rate warning. This warning is asserted if the ABI slew rate limiting is enabled and a condition that requires the limiting to be applied has occurred. The error flag clears on a read of the STATUS_REG register or reset.
Purpose of Slew Rate Limiting is to prevent an ABI integrity error.

Value	Description
0	Slew rate limiting is not active.
1	Slew rate limiting is enabled and active. ABI output is incrementing at the designated slew rate.

ABI [3]:

ABI integrity error. This bit is asserted if the SLR is equal to zero and the ABI output signals violate the ABI state flow. The error flag clears on a reset.

Value	Description
0	ABI signals are in a valid state
1	ABI signals violate ABI state flow and ABI_SLEW_RATE = 0.

ACD [2]:

ABI count-up feature done (complete). The bit is asserted when the ABI count-up feature is enabled, was active, and is now complete. The bit clears after a read of the register. The count-up feature is disabled when ABI_SLEW_RATE (extended: 0x25 [11:6]) is set to 0.

Value	Description
0	ABI count-up feature is not active
1	ABI count-up feature activated and is complete

ROT_H [1]:

Rotation Direction.

Value	Description
0	indicates rotation direction of increasing angle
1	indicates rotation direction of decreasing angle

ANGLE_RDY [0]:

Angle output is valid. The bit is asserted after the first angle update to the primary and secondary channels when returning from low power mode to normal operation or after a reset event. The bit remains asserted when in normal operation.

Value	Description
0	Angle is not valid
1	Angle is valid following a reset event or after returning to normal operation from low power mode.

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Address 0x0F: (CTRL) – Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	FULL_RST	SOFT_RST	TC_WR_EN	TCR
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

FULL_RST [3]:

Full Reset. Writing at value of one to this bit triggers a full reset of the device logic, including a full load of the EEPROM, reset of all the status and error registers, reset of the signal processing, reset of the outputs and communication protocols, and a reset of the main controller. This function includes all functions performed in a SOFT_RST. After the reset is complete the POR flags (primary: 0x11 [9] and 0x12 [9]) are asserted.

SOFT_RST [2]:

Soft Reset. Writing at value of one to this bit triggers a full reset of the device logic, reset of all the status and error registers, reset of the signal processing, and reset of the outputs and communication protocols. After the reset is complete the POR flag (primary: 0x11 [9] and 0x12 [9]) are asserted.

TC_WR_EN [1]

Turns Count Write Enable. If the loss of power feature is enabled, this bit allows for write access to the registers TURNS_COUNT_P (primary: 0x15 [10:0]) and TURNS_COUNT_S (primary: 0x1C [10:0]. This allows the external controller to overwrite the Turns Count value. Note, the TURNS_COUNT_P and TURN_COUNT_S must be set to the equivalent value to avoid a Turns Count warning error flag.

To modify the Turns Count registers first write the desired turns count to the registers TURNS_COUNT_P and TURNS_COUNT_S. Then write the bit TC_WR_EN. This will reset the internal turns counters, primary and secondary channel, to the value stored in TURNS_COUNT_P and TURNS_COUNT_S respectively. The bit, TC_WR_EN, clears when the sequence completes.

TCR [0]:

Turns Count Reset. Writing a value of one to this bit triggers a reset of the internal turns counters, primary and secondary channel. The counters reset to values dependent on the status of TURNS_CNT_INT_P (extended: 0x3E [12]) and TURNS_CNT_INIT_S (extended: 0x3F [12]).

Address 0x10: (PRIM_ANGLE) – Primary Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_P															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_OUT_P [15:0]:

Register indicates the calculated angle from the primary sin (y channel) and primary cos (x channel) inputs. The parameter is a 16-bit unsigned integer with value of ANGLE_OUT_P × $360/2^{16}$ in degrees. A read of this register latches the data in ANGLE_OUT_LATCH_S (primary: 0x0A [15:0]), TURNS_COUNT_LATCH_P (primary: 0xB [15:0]), TURNS_COUNT_LATCH_S (primary: 0x0D [15:0]).

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Address 0x11 (ERROR_0) – Primary Device Error Flags

This is one of two error registers. All errors in the register are latched, meaning they will remain in a high logic state after they occurred until they are cleared. Errors clear after a read of the register and the error conditions no longer persist. An example is after a power on event the POR error flag is asserted a read of this register will reset the POR error flag.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	XEE	BSY	SME	EUE	ESE	POR	OVCC	UVCC	MSH	MSL	SMM_P	OFE_P	SAT_P	TSE_P	VCF_P
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

IER [15]:

Interface error. Invalid SPI packet detected. Packet was discarded. Also indicates an error in the Manchester communication.

Value	Description
0	No Interface Error
1	Interface Error

XEE [14]:

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute Error

BSY [13]:

Extended access overflow. An Extended write or Extended read was initiated before previous operation is complete.

Value	Description
0	No extended access error
1	extended access error

SME [12]:

Shadow memory error. Indicates detection of a MISR (multiple input shift register) error in the shadow memory. This error requires a reset to clear.

Value	Description
0	No error Shadow memory error
1	Shadow memory error

EUE [11]:

EEPROM uncorrectable error. A multi-bit EEPROM read error occurred. EEPROM bit errors are only checked on EEPROM load (i.e., power-up or reset). This error requires a reset to clear and the condition no longer persists.

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

ESE [10]:

EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset). Single bit errors are detected and corrected in shadow memory by hamming ECC.

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error detected

POR [9]:

Reset condition. Indicates a reset event has occurred or an EEPROM load has occurred.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are re-initialized.

OVCC [8]:

VCC Overvoltage condition. Indicates an overvoltage condition on the supply pin, VCC. Will continue to assert until fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Overvoltage error
1	VCC Overvoltage error detected error

UVCC [7]:

VCC Undervoltage condition. Indicates an undervoltage condition on the supply pin, VCC. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Undervoltage error
1	VCC Undervoltage error detected

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MSH [6]:

Magnetic signal high fault. Indicates the magnitude of the magnetic input signal sensed by the secondary channel is above the high limit threshold. The high limit threshold is set via the EEPROM parameter MSH_THR (extended: 0x24 [9:7]). Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field high fault
1	Magnetic field above the high threshold, MSH_THR

MSL [5]:

Magnetic signal low fault. Indicates the magnitude of the magnetic input signal sensed by the secondary channel is below the low limit threshold. The Low limit threshold is set via the EEPROM parameter MSL_THR (extended: 0x24 [12:10]. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field low fault
1	Magnetic field lower below the low threshold, MSL_THR

SMM_P [4]:

Signal mismatch error. Indicates the primary angle and secondary angle deviate by more than the angle mismatch threshold (set by EEPROM field ANGLE_MISMATCH, address 0x24 bits 14:13). An error detected by this monitor will continue to assert until the fault condition is removed (and the register is cleared).
SMM_P also reports a BIST error on registers ERROR_0 (primary: 0x11) and ERROR_1 (primary: 0x12). During power on, every low power mode to normal operating mode transition, all ERROR_0 and ERROR_1 inputs are checked for a stuck at zero condition to confirm the error condition may assert the appropriate indicator bit. An error detected by this monitor requires a reset to clear.

Value	Description
0	No signal path mismatch or error register BIST failure detected
1	Signal path mismatch or error register BIST failure detected

OFE_P [3]:

Oscillator Frequency Error. One of the oscillator watchdogs circuits, monitoring the high frequency and low frequency oscillators has detected a fault. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No oscillator error
1	Oscillator watchdog error

SAT_P [2]:

Primary channel saturation flag. Indicates internal signals in the primary or secondary channel have saturated, including the input to the x and y ADCs and factory signal conditioning prior to the angle calculation. May indicate the magnetic input is outside of the specified range. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No saturation detected in the primary channel signal path
1	Saturation conditions detected within the primary channel signal path

TSE_P [1]:

Temperature sensor error. The primary or secondary temperature sensor calculated output is below –71°C or above 185°C. Also reports when the calculated temperature output of the primary and secondary temperature sensors differ by more than 20°C. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	Primary and secondary temperature sensors within range.
1	Primary or secondary temperature sensor calculated output below –71° or above 185°C or the primary temperature sensor calculate output differs more than 20 degrees when compared to the secondary temperature sensor calculated output.

VCF_P [8]:

Voltage Check Fault. Indicates a failure of an internal reference voltage. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No voltage check fault detected
1	Voltage check fault

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Address 0x12 (ERROR_1) – Secondary Device Error Flags

This is one of two error registers. All errors in the register are latched, meaning they will remain in a high logic state after they occurred until they are cleared. Errors clear after a read of the register and the error conditions no longer persist. An example is after a power on event the POR error flag is asserted a read of this register will reset the POR error flag.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER_R	XEE_R	BSY_R	SME_R	EUE_R	ESE_R	POR_R	OVCC_R	UVCC_R	MSH_R	MSL_R	SMM_S	OFE_S	SAT_S	TSE_S	VCF_S
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

IER_R [15]:

Redundant Interface error. Invalid SPI packet detected. Packet was discarded. Also indicates an error in the Manchester communication.

Value	Description
0	No Interface Error
1	Interface Error

XEE_R [14]:

Redundant Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute Error

BSY_R [13]:

Redundant Extended access overflow. An Extended write or Extended read was initiated before previous operation is complete.

Value	Description
0	No extended access error
1	extended access error

SME_R [12]:

Redundant Shadow memory error. Indicates detection of a MISR (multiple input shift register) error in the shadow memory. This error requires a reset to clear.

Value	Description
0	No error Shadow memory error
1	Shadow memory error

EUE_R [11]:

A multi-bit EEPROM read error occurred.
EEPROM bit errors are only checked on EEPROM load (i.e., power-up or reset). This error requires a reset to clear and the condition no longer persists.

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

ESE_R [10]:

Redundant EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset). Single-bit errors are correctable in shadow memory by hamming ECC.

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error detected

POR_R [9]:

Redundant Reset condition. Indicates a reset event has occurred or a EEPROM load has occurred.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are re-initialized.

OVCC_R [8]:

Redundant VCC Overvoltage condition. Indicates an overvoltage condition on the supply pin, VCC. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Overvoltage error
1	VCC Overvoltage error detected error

UVCC_R [7]:

Redundant VCC Undervoltage condition. Indicates an undervoltage condition on the supply pin, VCC. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No VCC Undervoltage error
1	VCC Undervoltage error detected

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MSH_R [6]:

Redundant Magnetic signal high fault. Indicates the magnitude of the magnetic input signal sensed by the secondary channel is above the high limit threshold. The high limit threshold is set via the EEPROM parameter MSH_THR (extended: 0x24 [9:7]). Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field high fault
1	Magnetic field above the high threshold, MSH_THR

MSL_R [5]:

Redundant Magnetic signal low fault. Indicates the magnitude of the magnetic input signal sensed by the secondary channel is below the low limit threshold. The Low limit threshold is set via the EEPROM parameter MSL_THR (extended: 0x24 [12:10]. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field low fault
1	Magnetic field lower below the low threshold, MSL_THR

SMM_S [4]:

Redundant Signal mismatch error. Indicates the primary angle and secondary angle deviate by more than the angle mismatch threshold (set by EEPROM field ANGLE_MISMATCH, address 0x24 bits 14:13). An error detected by this monitor will continue to assert until the fault condition is removed (and the register is cleared).
SMM_S also reports a BIST error on registers ERROR_0 (primary: 0x11) and ERROR_1 (primary: 0x12). During power on, every low power mode to normal operating mode transition, all ERROR_0 and ERROR_1 inputs are checked for a stuck at zero condition to confirm the error condition may assert the appropriate indicator bit. An error detected by this monitor requires a reset to clear.

Value	Description
0	No signal path mismatch or error register BIST failure detected
1	Signal path mismatch or error register BIST failure detected

OFE_S [3]:

Redundant Oscillator Frequency Error. One of the oscillator watchdogs circuits, monitoring the high frequency and low frequency oscillators has detected a fault. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No oscillator error
1	Oscillator watchdog error

SAT_S [2]:

Secondary channel saturation flag. Indicates internal signals in the primary or secondary channel have saturated, including the input to the x and y ADCs and factory signal conditioning prior to the angle calculation. May indicate the magnetic input is outside of the specified range. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No saturation detected in the secondary channel signal path
1	Saturation conditions detected within the secondary channel signal path

TSE_S [1]:

Temperature sensor error. The primary or secondary temperature sensor calculated output is below –71°C or above 185°C. Also reports when the calculated temperature output of the primary and secondary temperature sensors differ by more than 20°C. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	Primary and secondary temperature sensors within range.
1	Primary or secondary temperature sensor calculated output below –71° or above 185°C or the primary temperature sensor calculate output differs more than 20 degrees when compared to the secondary temperature sensor calculated output.

VCF_S [8]:

Redundant Voltage Check Fault. Indicates a failure of an internal reference voltage. Will continue to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No voltage check fault detected
1	Voltage check fault

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Address 0x13: (TEMP12B_P) – Primary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	TEMP_OUT_P											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TEMP_OUT_P [11:0]:

Current ambient temperature from the primary channel internal temperature sensor. Value is a 12-bit signed integer, where: Temperature (°C) ≈ (Value of TEMP_OUT_S / 8) + 25.0.

Address 0x14: (FIELD_REG) – Field Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIELD															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

FIELD [15:0]:

Register indicates the calculated amplitude of the secondary sin (y channel) and secondary cos (x channel). This value may be used to give a relative measure of the peak magnetic flux density applied to the sensing plane of the device. Value is a 16-bit unsigned integer.

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Address 0x15: (TURNS_COUNTER_P) – Primary Turns Counter

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ERROR_P	TCO_ERROR_P	0	TURNS_COUNT_P										
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TCW_ERROR_P [13]:

Primary channel Turns counter warning. The bit is set on a condition that may compromise the accuracy of the primary turns count value. The bit is redundant with TCW_ERROR_S and TCW_ERROR_LATCH_S. If any of the error bits, VCF_P, OFE, and UVCC are set, but not limited to TCW_ERROR_P is set. The bit is also set on a condition that may compromise the accuracy of the turns count value during low power operation.

TCW_ERROR_P also reports a BIST error on registers TURNS_COUNTER_P (primary: 0x15) and TURNS_COUNTER_S (primary 0x1C). During power on, every low power mode to normal operating mode transition, all TURNS_COUNTER_P and TURNS_COUNTER_S inputs are checked for a stuck at zero condition to confirm the error condition may assert the appropriate indicator bit. An error detected by this monitor requires a reset to clear.

Value	Description
0	No turns count warning
1	Warning primary turns count value may be incorrect

TCO_ERROR_P [12]:

Primary Turns Counter Overflow Error. Indicates the turns counter surpassed its allowable range of –1024 to 1023 (approximately ±256 rotations). Must be cleared with a turns-count reset (See special commands in the CTRL register description, primary: 0xF).

Value	Description
0	No turns count overflow error
1	Primary Turns count overflow error

TURNS_COUNT_P [10:0]:

Primary turns count. Value represents the primary channel turns count Indicates total number of turns relative to initial value at power-on. The parameter has a resolution of 90° and represented as an 11-bit signed integer.

Decimal Value	Binary Bit Value	Turns Count 90° resolution (Actual mechanical full rotations)
0	000 0000 0000	0 (0)
1	000 0000 0001	+1 (+0.25)
511	0001 1111 1111	+511 (127.75)
512	010 0000 0000	+512 (128)
1023	011 1111 1111	+1023(+255.75)
–1	111 1111 1111	–1 (–0.25)
–512	110 0000 0000	–512 (–128)
–1024	1000 0000 0000	–1024 (–256)

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Address 0x16 (ANGLE_WITH_HYST) – Hysteresis Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ABI_UVW_ANGLE															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ABI_UVW_ANGLE [15:0]:

Angle output from channel selected for ABI / UVW after hysteresis processing. The hysteresis configuration is set using the parameter ANGLE_HYST (extended: 0x3E [25:23]). The parameter is a 16-bit unsigned integer with a value of ABI_UVW_ANGLE × $(360/2^{16})$ in degrees.

Address 0x17 (VELOCITY_REG) – Primary Channel Velocity Reading (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VELOCITY															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

VELOCITY [15:0]:

Angular velocity of the primary channel calculated as the 1st derivative of the primary channel angle position data. The parameter is a 16-bit unsigned integer with a value of VELOCITY × (0.8941) in revolutions per minute. Accuracy of the velocity measurement is not quantified at final test and not guaranteed by Allegro.

Address 0x18 (ACCELERATION_REG) – Primary Channel Acceleration Reading (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCELERATION															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ACCELERATION [15:0]:

Angular acceleration of the primary channel calculated as the 1st derivative of the velocity data. The parameter is a 16-bit signed integer with a value of ACCELERATION × (0.4547) in revolutions per second squared. Accuracy of the acceleration measurement is not quantified at final test and not guaranteed by Allegro.

Address 0x19: (SEC_ANGLE) – Secondary Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_S															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_OUT_S [15:0]:

Register indicates the calculated angle from the secondary sin (y channel) and secondary cos (x channel) inputs. The parameter is a 16-bit unsigned integer with value of ANGLE_OUT_S × $360/2^{16}$ in degrees.

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Address 0x1A: (SEC_ANGLE_LATCH) – Latched Secondary Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_LATCH_S															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_OUT_LATCH_S [15:0]:

Register indicates the calculated angle from the secondary sin (y channel) and secondary cos (x channel) inputs. The parameter is latched on the read of ANGLE_OUT_P (Primary: 0x10 [15:0]) and is represented as a 16-bit unsigned integer with a value of ANGLE_OUT_LATCH_S × $360/2^{16}$ in degrees.

Address 0x1B: (TURNS_COUNTER_LATCH_P) – Latched Primary Turns Counter

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ERROR_LATCH_P	TCO_ERROR_LATCH_P	0	TURNS_COUNT_LATCH_P										
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TCW_ERROR_LATCH_P [13]:

Latched Primary channel Turns Counter Warning. The bit has the same definition as TCW_ERROR_P (primary 0x15 [13]) and is latched on the read of ANGLE_OUT_P (primary: 0x10 [15:0])

TCO_ERROR_LATCH_P [12]:

Latched Primary Turns Counter Overflow Error. The bit has the same definition as TCO_ERROR_P (primary 0x15 [12]) and is latched on the read of ANGLE_OUT_P (Primary: 0x10 [15:0])

TURNS_COUNT_P [10:0]:

Latched Primary Turns Count. The parameter has the same definition as TURNS_COUNT_P (primary 0x15 [10:0]) and is latched on the read of ANGLE_OUT_P (primary: 0x10 [15:0])

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Address 0x1C: (TURNS_COUNTER_S) – Secondary Turns Counter

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ERROR_S	TCO_ERROR_S	0	TURNS_COUNT_S										
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TCW_ERROR_S [13]:

Secondary channel Turns Counter Warning. The bit is set on a condition that may compromise the accuracy of the secondary turns count value. This bit is asserted if any of the error bits, VCF_S, OFE, MSH, MSL, and UVCC are set. The bit is also set on a condition that may compromise the accuracy of the secondary turns count value during low power operation.

TCW_ERROR_S also reports a BIST error on registers TURNS_COUNTER_P (primary: 0x15) and TURNS_COUNTER_S (primary 0x1C). During power on, every low power mode to normal operating mode transition, all TURNS_COUNTER_P and TURNS_COUNTER_S inputs are checked for a stuck at zero condition to confirm the error condition may assert the appropriate indicator bit. An error detected by this monitor requires a reset to clear.

Value	Description
0	No turns count warning
1	Warning primary turns count value may be incorrect

TCO_ERROR_S [12]:

Secondary Turns Counter Overflow Error. Indicates the turns counter surpassed its allowable range of –1023 to 1024 (approximately ±256 rotations). Must be cleared with a turns-count reset (See special commands in the CTRL register description, primary: 0xF).

Value	Description
0	No turns count overflow error
1	Primary Turns count overflow error

TURNS_COUNT_S [10:0]:

Secondary turns count. Value represents the secondary channel turns count Indicates total number of turns relative to initial value at power-on. The parameter has a resolution of 90° and represented as an 11-bit signed integer.

Decimal Value	Binary Bit Value	Turns Count 90° resolution (Actual mechanical full rotations)
0	000 0000 0000	0 (0)
1	000 0000 0001	+1 (+0.25)
511	0001 1111 1111	+511 (127.75)
512	010 0000 0000	+512 (128)
1023	011 1111 1111	+1023(+255.75)
–1	111 1111 1111	–1 (–0.25)
–512	110 0000 0000	–512 (–128)
–1024	1000 0000 0000	–1024 (–256)

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Address 0x1D: (TURNS_COUNTER_LATCH_S) – Latched Secondary Turns Counter

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	TCW_ERROR_LATCH_S	TCO_ERROR_LATCH_S	0	TURNS_COUNT_LATCH_S										
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TCW_ERROR_LATCH_S [13]:

Latched Secondary channel Turns Counter Warning. The bit has the same definition as TCW_ERROR_S (primary: 0x1C [13]) and is latched on the read of ANGLE_OUT_P (primary: 0x10 [15:0])

TCO_ERROR_LATCH_S [12]:

Latched Secondary Turns Counter Overflow Error. The bit has the same definition as TCO_ERROR_S (primary: 0x1C [12]) and is latched on the read of ANGLE_OUT_P (primary: 0x10 [15:0])

TURNS_COUNT_S [10:0]:

Latched Primary Turns Count. The parameter has the same definition as TURNS_COUNT_S (primary: 0x1C [10:0]) and is latched on the read of ANGLE_OUT_P (primary: 0x10 [15:0])

Address 0x1E: (ACCESS) – Access Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCESS_KEY						CUSTOMER_REGISTER_LOCK		factory		CUSTOMER_EEPROM_LOCK		FACTORY_EEPROM_LOCK		CUSTOMER_ACCESS	FACTORY_ACCESS
R/W	W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ACCESS_KEY [15:0]:

Writing to register 0x1E is a special command to enable access to the extended memory space, EEPROM and Volatile. See section Enabling EEPROM Access for more information.

CUSTOMER_ACCESS [1]:

Bit indicates access to customer registers within the extended memory space. A logic value of one indicates access to customer registers within the extended memory space is enabled.

FACTORY_ACCESS [0]:

Bit indicates access to factory registers within the extended memory space. A logic value of one indicates access to factory registers within the extended memory space is enabled.

Address 0x1F: (LOOPBACK_REG) – Loopback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOOPBACK															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LOOPBACK [15:0]:

Customer loopback register. The registers allow the external controller to perform a loopback test of the SPI communication between the controller and the peripheral A33115.

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EXTENDED MEMORY TABLE:

EEPROM (NONVOLATILE), SHADOW (VOLATILE), AND MISCELANEOUS (VOLATILE)

The EEPROM/Shadow register bitmap is shown below. All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires device unlock. The shadow memory is a copy of the EEPROM in the address range 0x40-0x7F.

Table 15: EEPROM / Shadow Memory Map

EEPROM Address	Bits																											
	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ECC	reserved				FACTORY_DIE_ID																reserved					
0x01	ECC	reserved				FACTORY_LOT																FACTORY_WAFER					
0x02	ECC	CUSTOM_ID																reserved									
0x03	ECC	CUSTOMER_ID																									
0x04... 0x23	Factory Reserved																										
0x24	ECC	MEM_LOCK				* _VOL_OUT	* _HIGH_Z	MASK_0	MASK_1	MASK_2	MASK_3	MASK_4	ANGLE_MISMATCH		MSL_THR			MSH_THR			LPM_DIS_C	TRNS_EN	reserved			reserved	
0x25	ECC	–	PWM _EN	PWM_CH	PWM_PERIOD				PWM_SLW_SEL			ABI_UVW_EN	ABI_UVW_CH	ABI_INDEX_MODE		ABI_SLEW_RATE						ABI_UVW_RESOLUTION			ABI_UVW_INV*	ABI_0_UVW_1	
0x26	ECC	INTREP_RATE	PRIM_LINT01												INTERP_BYP	PRIM_LINT00											
0x27	ECC	–	PRIM_LINT03												TC_HYST*	PRIM_LINT02											
0x28	ECC	–	PRIM_LINT05												–	PRIM_LINT04											
0x29	ECC	–	PRIM_LINT07												–	PRIM_LINT06											
0x2A	ECC	PWM_PORCH_SEL			–	PRIM_LINT09												PRIM_LINT08									
0x2B	ECC	–	–	–	–	PRIM_LINT11												PRIM_LINT10									
0x2C	ECC	–	–	–	–	PRIM_LINT13												PRIM_LINT12									
0x2D	ECC	–	–	–	–	PRIM_LINT15												PRIM_LINT14									
0x2E	ECC	–	–	–	–	PRIM_LINT17												PRIM_LINT16									
0x2F	ECC	–	–	–	–	PRIM_LINT19												PRIM_LINT18									
0x30	ECC	–	–	–	–	PRIM_LINT21												PRIM_LINT20									
0x31	ECC	–	–	–	–	PRIM_LINT23												PRIM_LINT22									
0x32	ECC	–	SEC_LINT01												TC_HYST*	SEC_LINT00											
0x33	ECC	–	SEC_LINT03												–	SEC_LINT02											
0x34	ECC	–	SEC_LINT05												–	SEC_LINT04											
0x35	ECC	–	SEC_LINT07												–	SEC_LINT06											

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Table 15: EEPROM / Shadow Memory Map

EEPROM Address	Bits																											
	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x36	ECC	–	–	–	–	SEC_LINT09											SEC_LINT08										
0x37	ECC	–	–	–	–	SEC_LINT11											SEC_LINT10										
0x38	ECC	–	–	–	–	SEC_LINT13											SEC_LINT12										
0x39	ECC	–	–	–	–	SEC_LINT15											SEC_LINT14										
0x3A	ECC	–	–	–	–	SEC_LINT17											SEC_LINT16										
0x3B	ECC					SEC_LINT19											SEC_LINT18										
0x3C	ECC	–	–	–	–	SEC_LINT21											SEC_LINT20										
0x3D	ECC	ABI_CNT*	ABI_SR_DLY_EN	ABI_ERR_RPT_M*		SEC_LINT23											SEC_LINT22										
0x3E	ECC	ANGLE_HYST			SPI_FREQ_SHIFT			VEL_ACC_*	AUTO_CAL_DIS	LPM_SLEEP_TIME				PRIM_LIN_EN	TURNS_COUNT_INT_P	ROT_DIR_P	CUST_ANGLE_OFFSET_P										
0x3F	ECC	SPARE_CUST						ACCEL_UPDT_RATE		unused				SEC_LIN_EN	TURNS_COUNT_INT_S	ROT_DIR_S	CUST_ANGLE_OFFSET_S										

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Table 16: Volatile Memory Map

EEPROM Address	Bits																										
	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x80	Read Only, Factory Reserved																										
0x81	Read Only, Factory Reserved																										
0x82	–	–	–	–	–	–	EE_DBE_*	EE_SBE_*	EE_ECC						EE_ADDR						EE_ERR_STATUS					CP_ERR	EE_ERR
0x83		EE_DATA																									
0x84	–	–	–	–	–	–	–	–	–	–	–	–	–	EE_LOOP	EE_TEST_ADDR						USE*_TEST_ADDR	MARG*_*FAIL	MARGIN_STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
0x85	Read Only, Factory Reserved																										
0x86	Read Only, Factory Reserved																										
0x87	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	IBIST_PASS1_FAIL0	BIST_DONE	BIST_START
0x88-0x9D	Read Only, Factory Reserved																										
0x9E	–	–	–	–	–	–	–	–	–	–	–	MANCH_COMM_EN	Reserved														
0x9F-0xFF	Unused																										

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Address 0x0

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				FACTORY_ID																reserved					
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

FACTORY_ID [21:6]:

Identification number. When used in combination with FACTORY_LOT and FACTORY_WAFER create a unique identification for device traceability. The register access is customer read only.

Address 0x1

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				FACTORY_LOT																FACTORY_WAFER					
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

FACTORY_LOT [21:6]:

Identification number. When used in combination with FACTORY_ID and FACTORY_WAFER create a unique identification for device traceability. The register access is customer read only.

FACTORY_WAFER [5:0]:

Identification number. When used in combination with FACTORY_ID and FACTORY_LOT create a unique identification for device traceability. The register access is customer read only.

Address 0x2

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOM_ID																reserved									
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

CUSTOM_ID [25:10]:

Type identification number. May contain an identification number to distinguish a specific device configuration. For example, the CUSTOM_ID may be used to distinguish between various device types. The register access is customer read only.

Address 0x3

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOMER_ID																									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CUSTOMER_ID [23:7]:

Customer identification number. The register space is open for customer write access. The contents of the register have no effect on the device operating modes. A common use for the register is to store a unique identification number written by the customer. The register access is customer read and write.

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Address 0x24

Address range contains error mask bits, primary/secondary mismatch threshold settings, and magnetic threshold settings.

Bit	25	34	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEM_LOCK				*_VOL_OUT	*_HIGH_Z	MASK_0	MASK_1	MASK_2	MASK_3	MASK_4	ANGLE_ MISMATCH		MSL_THR			MSH_THR			LPM_DIS_C	TRNS_EN	reserved			reserved	
Default	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

MEM_LOCK [25:22]:
Extended memory access lock, EEPROM, Shadow, and Miscellaneous Volatile memory lock. Setting this parameter is permanent and may not be undone.

Value	Description
1100	Writing to EEPROM is locked
0011	Writing to EEPROM and Shadow memory is locked

BLOCK_VOLATILE_OUTPUT [21]:
Prevents bits within the volatile memory space, 0x80 through 0x9E, that may impact the output from operating.

Value	Description
0	Volatile bits allowed to function normally
1	Prevents operation of volatile bits, 0x80 through 0x9E, that may impact the output.

MAKE_ERRORS_HIGH_Z [20]:
Option for the PWM to stay in a high impedance state when an errors flag is set.

Value	Description
0	PWM outputs at 1/2 frequency and a fixed duty cycle in response to an error flag.
1	PWM output goes to a high impedance state in response to an error flag.

MASK_0 [19]:
Masks voltage related errors from reporting via S1/S0 of the SPI frame or PWM/ABI. Impacts VCF_P, VCF_S, UVCC, UVCC_R, OVCC, and OVCC_R. When set, masks OFE_P and OFE_S from asserting S1/S0 within the SPI frame. Oscillator frequency errors cannot be masked from PWM/ABI error reporting.

Value	Description
0	Voltage check, undervoltage, and overvoltage flags are reported by S1/S0 in SPI and ABI/PWM as configured by EEPROM fields: MAKE_ ERRORS_HIGH_Z and ABI_ERR_RPT_MODE. Oscillator frequency errors (OFE_P and OFE_S) are reported via S1/S0, PWM/ABI.
1	Voltage check, undervoltage, and overvoltage flags are not reported via S1/S0 of the SPI frame or via ABI/PWM. Oscillator frequency errors (OFE_P and OFE_S) are not reported via S1/ S0 in SPI, but are still reported in PWM/ABI OFE_PR, OFE_S, VCF_P, VCF_S, UVCC, UVCC_R, OVCC, OVCC_R will still assert within direct memory address 0x11 and 0x12.

MASK_1 [18]:
Masks the Temperature Sensor Error (TSE_P and TSE_S) flag from asserting via S1/0 in SPI or by way of ABI/PWM.

Value	Description
0	TSE_P and TSE_S are reported via S1/S0 in SPI and ABI/ PWM as configured by EEPROM fields: MAKE_ERRORS_ HIGH_Z and ABI_ERR_RPT_MODE.
1	Temperature Sensor Error conditions are not reported via S1/S0 of the SPI frame or via ABI/PWM. TSE_P and TSE_S will still assert within direct memory address 0x11 and 0x12.

MASK_2 [17]:
Masks magnetic field related error conditions from being reported via S1/ S0 of SPI or through ABI/PWM.
Impacts SAT_P, SAT_S, MSL, MSL_R, MSH, and MSH_R.

Value	Description
0	Saturation and magnetic sense flags are reported via S1/ S0 in SPI and ABI/PWM as configured by EEPROM fields: MAKE_ERRORS_HIGH_Z and ABI_ERR_RPT_MODE.
1	Saturation and magnetic sense error flags are not reported via S1/S0 of the SPI frame or via ABI/PWM. SAT_P, SAT_S, MSL, MSL_R, MSH, and MSH_R will still assert within direct memory address 0x11 and 0x12.

MASK_3 [16]:
Bit to mask the SMM_P and SMM_S flags from being reported via S0/S1 SPI bits, PWM or ABI.
SMM_P and SMM_S will still be present within ERROR_0 and ERROR_1 serial registers.

Value	Description
0	Signal mismatch error reported by S1/S0 in SPI, and by ABI/PWM as configured by EEPROM fields: MAKE_ ERRORS_HIGH_Z and ABI_ERR_RPT_MODE.
1	Signal mismatch error is not reported via S1/S0 of the SPI frame or via ABI/PWM. SMM_P and SMM_S will still be asserted within direct memory address 0x11 and 0x12.

MASK_4 [15]:
Bit to mask error flags reporting on the output. Setting this bit to a logic value of one masks the ABI or SLR error flags.

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ANGLE_MISMATCH [14:13]:
Angle mismatch. Sets the threshold for the allowable mismatch between the Primary and Secondary angle outputs. If the Primary and Secondary angle outputs differ more than the threshold the SMM and SMM_S flags are set.

Value	Description: Signal Path Mismatch Threshold in degrees
0	3
1	5
2	8
3	12

MSL_THR [12:10]:
Magnetic Threshold low value. Sets the low threshold of the input magnetic flux density magnitude. If the magnetic field value reported in the field register (direct 0x14) is below the msl threshold, the MSL and MSL_R flag will be set. When MSL_THR is set to a value of 0 the low threshold is disabled.

Value	Description: Digital Value of the Input Magnetic Flux Density
0	0
1	9830
2	13107
3	19661
4	22938
5	26214
6	29491
7	32768

MSH_THR [9:7]:
Magnetic Threshold high value. Sets the high threshold of the input magnetic flux density magnitude. If the magnetic field value reported in the field register (direct 0x14) is above the MSH threshold, the MSH and MSH_R flag will be set. When MSH_THR is set to a value of 0 the high threshold is disabled.

Value	Description: Digital Value of the Input Magnetic Flux Density
0	No threshold
1	52429
2	45875
3	39322
4	36045
5	32768
6	29491
7	26214

LPM_DIS_C [6]:
Setting this bit to a logic value of one disables the Low Power Mode feature.

TRANSPORT_EN [5]:
Enables the transport mode feature. When TRANSPORT_E is set to a logic value of one the A33115 operates in transport mode after entering low power mode.

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Address 0x25

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PWM_EN	PWM_CH*	PWM_PERIOD				PWM_SLW_SEL			ABI_UVW_EN	ABI_UVW_CH*	ABI_INDEX_MODE		ABI_SLEW_RATE						ABI_UVW_RESOLUTION				ABI_UVW_INV*	ABI_0_UVW_1
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PWM_EN [24]:

PWM output enable. Setting this bit to a logic value of one enables the PWM output.

PWM_CHANNEL [23]:

PWM channel select. Controls the angle output channel reported on the PWM output.

Value	Description
0	Primary channel angle reported on the PWM output
1	Secondary channel angle reported on the PWM output

PWM_PERIOD [22:19]

PWM output period. Controls the period, or frequency, of the PWM output.

Value	Frequency (Hz)
0	125
1	167
2	250
3	333
4	500
5	667
6	800
7	1000

Value	Frequency (Hz)
8	1333
9	1600
10	2000
11	2667
12	4000
13	5333
14	8000
15	16000

PWM_SLW_SEL [18:16]

PWM fall time control. Controls the fall time of the PWM output. A value of zero sets the PWM output fall time to the fastest rate, a value of seven sets the PWM output fall time to the slowest rate.

ABI_UVW_EN [15]:

ABI or UVW output enable. Setting this bit to a logic value of one enables the ABI or UVW outputs.

ABI_UVW_CHANNEL [14]:

ABI or UVW channel select. Controls what angle output channel is reported on the ABI or UVW outputs.

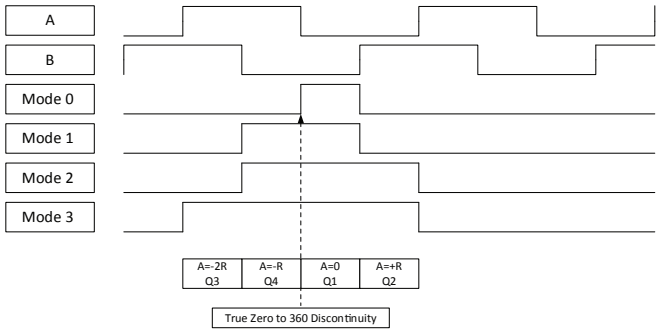
Value	Description
0	Primary channel angle reported on the AB or UVW outputs
1	Secondary channel angle reported on the ABI or UVW outputs

ABI_INDEX_MODE [13:12]:

Defines the width and placement of the “I” pulse in ABI.

Value	Description
0	I pulse is set only at 0° to +R
1	I pulse set between –R to +R
2	I pulse set between –R to +2R
3	I pulse set between –2R and +2R

“R” indicates the ABI quadrature resolution.



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ABI_SLEW_RATE [11:6]:

ABI slew time rate. “0” disables slew limiting.
Minimum edged-to-edge time for ABI output is defined by:

$$(N + 1) \times 125\ ns$$

where “N” is the value of ABI_SLEW_RATE.
This limits the maximum ABI velocity. Reducing the ABI resolution can be used to counteract this. Setting to a non-zero value disables the ABI count-up feature.

Value	Description
0	Slew limiting disable
1	250 ns of slew control
…	…
63	8 µs of slew control

ABI_UVW_RESOLUTION [5:2]:

Defines resolution of ABI/UVW outputs.
In ABI mode, cycle resolution = $2^{(14-n)}$ where “n” is the ABI_UVW_RESOLUTION value.
In UVW mode, the number of pole pairs is n + 1.

Value	AB Pulses per Rev.	UVW Pole Pairs
0	N/A	1
1	N/A	2
2*	2^{12} = 4096	3
3*	2^{11} = 2048	4
4*	2^{10} = 1024	5
…	…	…
14	2^{0} = 1	15
15	N/A	16

* Values recommend for use only with TMR primary channel

ABI_UVW_INVERT_OUT_EN [1]:

Invert ABI/UVW signals.

Value	Description
0	ABI/UVW signals behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Value	Description
1	ABI/UVW signals are inverted and behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	1	1
Q2	1	0
Q3	0	0
Q4	0	1

ABI_0_UVW_1 [0]:

Defines behavior of the ABI/UVW pins. When ABI_0_UVW_1 is set to a logic value of one the parameters selects the output mode of the ABI / UVW output.

Value	Description
0	ABI output mode is selected
1	UVW output mode is selected

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Address 0x26

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INTREP_RATE	PRIM_LINT01												INTERP_BYP	PRIM_LINT00											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INTERPOLATOR_RATE [25]:

Interpolator rate. Angle output of Linearization blocks (both from Primary and Secondary paths) are driven to the interpolator block. This block takes the angle selected to be output through ABI/UVW protocol and applies a 2nd order interpolator to get an upsampled angle signal with configurable rate. The interpolator rate applies when INTERPOLATOR_BYPASS is set to a logic value of zero.

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^2$$

Transfer function: Where R = 2 or 4.

INTERPOLATOR_RATE Value	INTERPOLATOR_BYPASS Value	Angle Output Rate (µs)
X	1	2
0	0	0.5
1	0	1

PRIM_LINT01 [24:13]:
Primary channel Linearization table entry 01.

INTERPOLATOR_BYPASS [12]:
Interpolator bypass. See INTERPOLATOR_RATE for more information.

PRIM_LINT00 [11:0]:
Primary channel Linearization table entry 00.

Address 0x27

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	PRIM_LINT03												TC_HYST*	PRIM_LINT02											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PRIM_LINT03 [24:13]:
Primary channel Linearization table entry 03.

TC_HYST_DIS_P [12]:
Disables primary channel turns count hysteresis. A hysteresis of approximately 11.25 degrees, applies to the angle for the turns count calculation. A value of approximately ±5.625 degree area is applied on the turns count angle boundaries (90, 180, 270, 360 degrees) where the turns count is not updated.

Value	Description
0	Hysteresis applied to primary channel turns count
1	No hysteresis applied to primary channel turns count

PRIM_LINT02 [11:0]:
Primary channel Linearization table entry 02.

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Address 0x2A

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWM_PORCH_SEL			–	PRIM_LINT09											PRIM_LINT08										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PWM_PORCH_SEL [25:23]:
PWM output fixed low and high time selection. This parameter configures the fixed low and high time of the PWM output.

Value	PWM Low Clamp (% Duty Cycle)	PWM High Clamp (% Duty Cycle)
0	2	98
1	3	97
2	4	96
3	5	95
4	6	94
5	7	93
6	8	92
7	2	98

PRIM_LINT09 [21:11]:
Secondary channel Linearization table entry 9.

PRIM_LINT08 [10:0]:
Primary channel Linearization table entry 8.

Address 0x32

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	SEC_LINT01												TC_HYST*	SEC_LINT00											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

SEC_LINT01 [24:13]:
Secondary channel Linearization table entry 1.

TC_HYST_DIS_S [12]:
Disables secondary channel turns count hysteresis. A hysteresis of approximately 11.25 degrees, applies to the angle for the turns count calculation. A value of approximately ±5.625 degree area is applied on the turns count angle boundaries (90, 180, 270, 360 degrees) where the turns count is not updated.

Value	Description
0	Hysteresis applied to secondary channel turns count
1	No hysteresis applied to secondary channel turns count

SEC_LINT00 [11:0]:
Secondary channel Linearization table entry 0.

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Address 0x3D

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ABI_CNT*	ABI_SR_DLY_EN	ABI_ERR_RPT_M*		SEC_LINT23											SEC_LINT22										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ABI_COUNT_UP_RPT_EN [25]:
ABI count up report enable.

When set to a logic 1, PWM indicates the completion of ABI count-up by outputting the ACD flag. See Table 20 for details on ACD reporting. If set to 0, the ACD flag is not communicated via PWM.
It is recommended to set this field to a logic 0, disabling PWM reporting of the ACD flag.

Note: The count-up is disabled when ABI_SLEW_RATE (extended 0x25 [11:6]) is set to a value of zero.

Note: ABI conducts the count-up procedure when returning from an error state, unless ABI diagnostics are disabled (ABI_ERR_RPT_MODE = 2).

ABI_SR_DLY_EN [24]:
ABI Slew Rate Delay Enable.

Disables ABI count-up following power-on or reset (if ABI error reporting is enabled). If set to a logic 1, ABI pins will jump to the magnetic angle following initial power-on (or reset) sequence. The ABI integrity error will not assert during this transition.

Disabling of count-up only applies if ABI error reporting is enabled. If ABI error reporting is disabled (ABI_ERR_RPT_MODE = 2), ABI count-up will still occur following power-on or reset.

Value	Description
0	ABI count-up occurs following power-on or reset (if ABI_SLEW_RATE is non-zero).
1	ABI count-up will not occur following power-on or reset, if ABI error reporting is enabled.

ABI_ERR_RPT_MODE [23:22]:
ABI error report mode.

ABI fault reporting strongly depends on PWM logic.

Errors are reported through ABI in two different ways: In-phase error reporting or high-z error reporting. ABI_ERR_RPT_MODE controls which of these two methods is used.

With in-phase reporting, when an error occurs, the A and B outputs are in-phase with PWM (A and B pins mirror the PWM signal). The I pin is set to high impedance. See MAKE_ERRORS_HIGH_Z (extended: 0x24 [20]) for PWM error reporting configurations. In-phase error reporting is not recommended if PWM is disabled.

With high-Z reporting the A, B, and I pins are set to high impedance if an error occurs.

Value	Description
0	ABI high-z report mode
1	AB in-phase report mode
2	Error reporting disabled
3	ABI in-phase report mode (same as 1)

SEC_LINT23 [21:11]:
Secondary channel Linearization table entry 23.

SEC_LINT22 [10:0]:
Secondary channel Linearization table entry 22.

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Address 0x3E

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_HYST			SPI_FREQ_SHIFT			VEL_ACC_*	AUTO_CAL_DIS	LPM_SLEEP_TIME				PRIM_LIN_EN	TURNS_COUNT_INT_P	ROT_DIR_P	CUST_ANGLE_OFFSET_P										
Default	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ANGLE_HYST [25:23]:

Angle ABI hysteresis. Angle Hysteresis threshold applied to the angle for ABI calculation. Value is 16-bit resolution. Provides ≈0.01 to 1.41° of hysteresis.

$$\text{Angle Hysteresis} = \frac{360}{2^{16}} \times 2^{(\text{ANGLE\_HYS}+1)}$$

Value	Description
0	0.01° of Hysteresis
1	0.02° of Hysteresis
…	…
7	1.41° of Hysteresis

SPI_FREQ_SHIFT [22:20]:

Velocity and Acceleration SPI Frequency. The parameter selects the SPI SCLK frequency used. The setting is only used for scaling the Velocity and Acceleration values.

The SPI SCLK frequency is selectable as:

$$7.75\ \text{MHz} \times 2^{(\text{SPI\_FREQ\_SHIFT} - 7)}$$

Example: SPI_FREQ_SHIFT = 5 represents an SCLK of 1.9375 MHz.

In the case a different SPI FREQ is used, Velocity and Acceleration values will need to be scaled by the host controller using the following calculation.

$$\text{scale} = \frac{\text{REAL\_SPI\_FREQ}}{\text{SELECTED\_SPI\_FREQ}}$$

Where: Velocity = velocity × scale and Acceleration = acceleration × scale.

VEL_ACC_P0_S1 [9]:

Velocity and Acceleration angle channel selection. Setting the parameter to a logic value of zero selects the primary angle channel for use in the velocity and acceleration calculation. Setting the parameter to a logic value of one selects the secondary angle channel for use in the velocity and acceleration calculation.

AUTOCAL_DIS [18]:

Autocalibration disable. The angle processing signal paths uses an autocalibration algorithm, on the Primary path only, to remove residual Offset and Sensitivity mismatch between the sin and cos. Setting this parameter to a logic value of one disables the autocalibration feature. Note, if the autocalibration is enabled there must be an input magnetic field applied during power on.

LPM_SLEEP_TIME [17:14]:

Low Power Mode sleep time selection. Sets the sleep time during Low Power Mode for the turns count tracking. See section Low Power Mode for more information.

PRIM_LIN_EN [13]:

Primary angle channel Linearization correction enable. When set to a logic value of one the primary angle channel linearization correction is enabled.

TURNS_CNT_INT_P [12]:

Turns count initialization selection. Defines the initial value of the Turns count after a power reset event. Must be equal to the value set for TURNS_CNT_INT_S (extended: 0x3F [12])

Value	Description
0	Turns count initializes to a value of 0.
1	Turns count initialize to a value based on the initial angle reading. 0 ≤ primary angle < 90 degrees = 0 90 ≤ primary angle < 180 degrees = 1 180 ≤ primary angle < 270 degrees = 2 270 ≤ primary angle < 360 degrees = 3

ROT_DIR_P [11]:

Primary angle channel rotation direction. Must be set to the same value as ROT_DIR_S (extend: 0x3F [11]).

Value	Description
0	Primary channel rotation direction is counterclockwise
1	Primary channel rotation direction is clockwise

CUSTOMER_ANGLE_OFFSET_P [10:0]:

Primary channel angle offset adjustment. The parameter determines an angle offset value applied the primary angle channel.

Primary angle output = primary angle + CUSTOMER_ANGLE_OFFSET_P × 360 × 2^{-12}.

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Address 0x3F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE_CUST						ACCEL_UPDT_RATE		unused				SEC_LIN_EN	TURNS_COUNT_INT_S	ROT_DIR_S	CUST_ANGLE_OFFSET_S										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

SPARE_CUST [25:20]:

Spare customer bits. Spare EEPROM bits for miscellaneous customer purpose. The value of these bits have no effect on the outputs.

ACCEL_UPDT_RATE [19:18]:

Acceleration update rate.

Value	Acceleration Update Rate (ms)	Acceleration Bandwidth (Hz)
0	8.192	40
1	1.024	320
2	2.048	160
3	4.096	80

TURNS_CNT_INT_S [12]:

Turns count initialization selection. Defines the initial value of the Turns count after a power reset event. Must be equal to the value set for TURNS_CNT_INT_P (extended: 0x3E [12])

Value	Description
0	Turns count initializes to a value of 0.
1	Turns count initialize to a value based on the initial angle reading. 0 ≤ primary angle < 90 degrees = 0 90 ≤ primary angle < 180 degrees = 1 180 ≤ primary angle < 270 degrees = 2 270 ≤ primary angle < 360 degrees = 3

ROT_DIR_S [11]:

Secondary angle channel rotation direction. Must be set to the same value as ROT_DIR_P (extend: 0x3E [11]).

Value	Description
0	Secondary channel rotation direction is counterclockwise
1	Secondary channel rotation direction is clockwise

CUSTOMER_ANGLE_OFFSET_S [10:0]:

Secondary channel angle offset adjustment. The parameter determines an angle offset value applied the secondary angle channel.

Secondary angle output = secondary angle + CUSTOMER_ANGLE_OFFSET_S × 360 × 2^{-12}.

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Volatile Memory

Address 0x82

Bit	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	EE_DBE_*	EE_SBE_*	EE_ECC						EE_ADDR						EE_ERR_STATUS					CP_ERR	EE_ERR
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EE_DBE_FLAG [20]:

Error flag indicates detection of an EEPROM dual bit error. The EEPROM ECC logic detects an address with a dual bit error. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM dual bit error detected
1	EEPROM dual bit error detected

EE_SBE_FLAG [19]:

Error flag indicates detection of an EEPROM single bit error. The EEPROM ECC logic detects an address with a single bit error. The ECC logic automatically corrects the faulty bit in the volatile region of memory. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM single bit error detected
1	EEPROM single bit error detected

EE_ECC [18:13]:

EEPROM ECC data. After the internal margin test is complete this parameter contains the ECC data bits of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x84 [4:3]) for margin results information.

EE_ADDR [12:7]:

EEPROM address data. After the internal margin test is complete this parameter contains the address of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x84 [4:3]) for margin results information.

EE_ERR_STATUS [6:2]:

Indicates the error status of the last EEPROM write. Any value greater than zero indicates an error detected during the last EEPROM write.

CP_ERR [1]:

Indicates the error status of the EEPROM write charge pump during the last EEPROM write. A logic value of one indicates an error is detected and sets EE_ERR_STATUS (extended: 0x82 [6:2]).

EE_ERR [0]:

Indicates detection of an EEPROM write error. The bit is set to a logic value of one when an EEPROM write error is detected. The bit clears after read.

Address 0x83

Bit	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	EE_DATA																									
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EE_DATA [25:0]:

EEPROM field data. After the internal margin test is complete this parameter contains information from the data fields of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x84 [4:3]) for margin results information.

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Address 0x84

Bit	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–	–	–	–	–	–	EE_LOOP	EE_TEST_ADDR						USE*_TEST_ADDR	MARG*_*FAIL	MARGIN_STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW	RW	RW

EE_LOOP [13]:

Continuously loop the margin test. When this bit is set to logic value of one the margin test will loop continuously when started and will stop if an error is detected or the MARGIN_START (extended: 0x84 [0]) is cleared.

Value	Description
0	Margin test runs once.
1	Margin test loops continuously until an error is detected.

EE_TEST_ADDR [12:7]:

Optional start address for margin test. Defines the starting address for the margin test when EE_USE_TEST_ADDR (extended: 0x84 [6]) is set to one. If the margin test reports a failure, this will contain the address of the first failing EEPROM row, similar to EE_ADDR.

EE_USE_TEST_ADDR [6]:
When set to a logic value of one the margin test will start at the address defined by EE_TEST_ADDR (extended: 0x84 [12:7])

Value	Description
0	Margin test starts at address 0x0
1	Margin test starts at address defined by EE_TEST_ADDR

MARGIN_MIN_MAX_FAIL [5]:

If a margin failure is detected this bit indicates if the failure was detected at the minimum or maximum reference level.

Value	Description
0	Margin test failure detected at minimum threshold
1	Margin test failure detected at maximum threshold

MARGIN_STATUS [4:3]:

Indicates the status of the margin test. The bits clear after read or reset event.

Value	Description
0	Reset condition, no result from margin test
1	Pass. No errors detected during margin test.
2	Fail. Error detected during margin test.
3	In progress. Margin test is in still running.

MARGIN_NO_MIN [2]:

Disable the minimum reference level during margin test. When the bit is set to a logic value of one the margin test does not check for errors at the low reference level.

Value	Description
0	Margin test includes check at the low reference level.
1	Margin test does not include check at the low reference level.

MARGIN_NO_MAX [1]:

Disable the maximum reference level during margin test. When the bit is set to a logic value of one, the margin test does not check for errors at the high reference level.

Value	Description
0	Margin test includes check at the high reference level.
1	Margin test does not include check at the high reference level.

MARGIN_START [0]:
Triggers start of margin test. When the bit is set to a logic value of one the margin test begins. The bit clears when the margin test completes and EE_LOOP (extended: 0x84 [13]) equals zero. If EE_LOOP equals one the margin test runs until MARGIN_START is set to a value of zero. If margin test detects an error the MARGIN_START bit clears.

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Address 0x87

Bit	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	IBIST_PASS1_FAIL0	BIST_DONE	BIST_START
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LBIST_PASS1_FAIL0 [2]:

Indicates pass or fail result of LBIST (logic built-in self test).

Value	Description
0	Indicates a fail result from the LBIST
1	Indicates a pass result from the LBIST

BIST_DONE [1]:

Indicates BIST (built-in self test) is complete.

Value	Description
0	Indicates BIST is in progress, BIST did not execute, or BIST was aborted.
1	Indicates BIST is complete

BIST_START [1]:

Initiates start of BIST. Bit is set to a logic value of one to initiate the start of LBIST. The bit self clears when LBIST is started. LBIST requires ≈105 ms to run. Angle is not available during LBIST. Running of LBIST is not typically required to meet safety metrics. See specific safety manual for a detailed listing of safety requirements.

Value	Description
0	Indicates LBIST is in progress or result not available.
1	Indicates LBIST is complete

Address 0x9E

Bit	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MANCH_COMM_EN	Reserved														
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

MANCH_COMM_E [15]:

Enables Manchester communications mode on the PWM output pin. When this bit is set to a logic value of one the PWM output stops and the pin becomes an input / output pin for Manchester communication. This bit is set directly with a write operation or indirectly using the access code. To exit Manchester communications mode the bit is set to a logic value of zero.

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SAFETY AND DIAGNOSTICS

The A33115 was developed in accordance with the ASIL design flow (ISO 26262) and incorporates several internal diagnostics as well as error/warning/status flags enabling the host microcontroller to assess the operational status of the die.

A short summary of the diagnostics is provided below. A complete listing and discussion of the A33115 safety features may be found in the Safety Manual.

Built-In Self-Tests

The A33115 features built-in-self-tests (BISTs) which may be initiated by the system microcontroller using the serial device communication, SPI, or Manchester.

BUILT-IN SELF-TEST (BIST)

BIST is implemented to verify the integrity of the logic (LBIST). LBIST is effectively a form of auto-driven scan. The tested logic is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudo-random data. The output of the scan chains are fed back into a multiple input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST requires approximately 105 ms to complete. During this time the logic circuits are under test and therefore communication and normal device operation are suspended. After completion of LBIST a reset, FULL_RST, is triggered and normal operation resumes. The results are reported in LBIST_PASS1_FAIL0 (extended: 0x87 [2]).

Status, Error, and Warning Flags

The A33115 features include several status, error, and warning flags. These flags allow the external controller to act in response of detected fault condition. Table 18 provides a summary list of the flags. More information is also found in the Primary Serial Interface Register Reference.

All flags may be read through the primary serial registers via SPI or Manchester communication. The error register, ERROR_1 (0x12) is a redundant copy of error flags contained in error register, ERROR_0 (0x11). These error flags remain set until the register is read or reset, and the condition is removed.

Error Reporting Through SPI

There are two error reporting bits, S0 and S1, within the A33115 SPI frame. The value of S0 and S1 represent the logical “or” of the bits within the error registers, ERROR_0 and ERROR_1. ABI related flags are only reported by S1. The S0 and S1 bits clear after a SPI read transaction and the condition for the flag no longer exists. Note, S0 and S1 are set to a value of one after a reset event and after returning to normal operating mode from Low Power Mode. If an error flag is masked the result of this flag is not reported by S0 and S1.

Information Flags

The A33115 features a dedicated status register (Primary 0xE), providing informational flags to the external controller. These flags may be useful for the external controller to monitor operation. Table 17 provides a summary list of the information status flags. More information is also found in the Primary Serial Interface Register Reference.

Table 17: Status Register Contents (Address 0xE)

Bit Value	Status Flag	Description
0	ANG_RDY	Angle Ready
1	ROT_H	Rotation Direction
2	ACD	ABI count-up procedure complete
3	ABI	ABI integrity error detected
4	SLR	Slew rate warning
5	Reserved	Reserved bit, no function.
6	BACK_FROM_LPM	Back from Low Power Mode

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Table 18: Status and Error Flags

Status and Error Flag	Description	Flag Response
VCF	Voltage Check Failure	VCF_P = 1 (primary: 0x11 [0] VCF_S = 1 (primary: 0x12 [0]
TSE	Temperature Sensor Error	TSE_P = 1 (primary: 0x11 [1] TSE_S = 1 (primary: 0x12 [1]
SAT	Saturation Error	SAT_P = 1 (primary: 0x11 [2] SAT_S = 1 (primary: 0x12 [2]
OFE	Oscillator Frequency Discrepancy Error	OFE_P = 1 (primary: 0x11 [3] OFE_S = 1 (primary: 0x12 [3]
SMM	Signal Path (primary channel versus secondary channel) Mismatch Error	SMM_P = 1 (primary: 0x11 [4] SMM_S = 1 (primary: 0x12 [4]
MSL	Magnet Sense Low (input condition below low threshold) Error	MSL = 1 (primary: 0x11 [5] MSL_R = 1 (primary: 0x12 [5]
MSH	Magnet Sense High (input condition above high threshold) Error	MSL = 1 (primary: 0x11 [6] MSL_R = 1 (primary: 0x11 [6]
UVCC	Undervoltage Error	UVCC = 1 (primary: 0x11 [7] UVCC_R = 1 (primary: 0x12 [7]
OVCC	Overvoltage Error	OVCC = 1 (primary: 0x11 [8] OVCC_R = 1 (primary: 0x12 [8]
POR	Power On Reset Event	POR = 1 (primary: 0x11 [9] POR_R = 1 (primary: 0x12 [9]
ESE	Single Bit EEPROM Error (correctable)	ESE = 1 (primary: 0x11 [10] ESE_R = 1 (primary: 0x12 [10]
EUE	Multi-Bit EEPROM Error (uncorrectable)	EUE = 1 (primary: 0x11 [11] EUE_R = 1 (primary: 0x12 [11]
SME	Shadow Memory Error. (Multiple Input Shift Register signature error)	SME = 1 (primary: 0x11 [12] SME_R = 1 (primary: 0x12 [12]
BSY	Extended Access Busy Condition	BSY = 1 (primary: 0x11 [13] BSY_R = 1 (primary: 0x12 [13]
XEE	Extended Execute Error Condition	EXE = 1 (primary: 0x11 [14] EXE_R = 1 (primary: 0x12 [14]
IER	Interface Error Condition	IER = 1 (primary: 0x11 [15] IER_R = 1 (primary: 0x12 [15]
ABI	ABI Integrity Fault	ABI = 1 (primary: 0x0E [3]
SLR	ABI Slew Rate Warning	SLR = 1 (primary: 0x0E [4]
TCW_ERROR	Turns Count Warning and Error	TCW_ERROR_P = 1 (primary: 0x15 [13] TCW_ERROR_LATCH_P = 1 (primary: 0x1B [13] TCW_ERROR_S = 1 (primary: 0x1C [13] TCW_ERROR_LATCH_S = 1 (primary: 0x1D [13]
TCO_ERROR	Turns Count Overflow Error	TCO_ERROR_P = 1 (primary: 0x15 [12] TCO_ERROR_LATCH_P = 1 (primary: 0x1B [12] TCO_ERROR_S = 1 (primary: 0x1C [12] TCO_ERROR_LATCH_S = 1 (primary: 0x1D [12]

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Error Reporting Through PWM

The PWM output is configurable to report flags using a special frequency and duty cycle or by going to a high impedance state. The parameter MAKE_ERRORS_HIGH_Z (extended: 0x24 [20]) configures the PWM error reporting function. When set to a value one the error flags result in a PWM at high impedance state for a minimum of two periods. When MAKE_ERRORS_HIGH_Z is set to a value of zero the PWM reports the error flags at a defined duty cycle, shown in Table 20, and at 1/2 the frequency defined by PWM_PERIOD (extended: 0x25 [22:19]).

In the event of multiple error flags, when MAKE_ERRORS_HIGH_Z equals zero, the PWM output reports the error condition according to priority. Table 20 list the error flags in the order of priority from highest to lowest. The highest priority error dictates the PWM duty cycle. Error flags OFE, SME, EUE, and ESE are the highest priority flags and report through the PWM output by a high-impedance state (100% duty cycle).

The parameter PWM_PORCH_SEL (extended: 0x2A [25:23]) configures the PWM minimum and maximum duty cycle, and also sets the duty cycle used for error reporting.

The duty cycle for a specific error and PWM_PORCH_SEL setting are shown in Table 20.

Table 19: MAKE_ERRORS_HIGH_Z

Code	Description
0	PWM carrier frequency is halved, and highest priority error is output on PWM at selected duty cycle.
1	PWM tristates on an error

Table 20: PWM Error Flag Duty Cycle

PMW_PORCH_SEL →		0	1	2	3	4	5	6	7
Error	Priority	Duty Cycle (%)							
OFE [1]	Highest	100	100	100	100	100	100	100	100
SME [1]	Highest	100	100	100	100	100	100	100	100
EUE [1]	Highest	100	100	100	100	100	100	100	100
ESE [1]	Highest	100	100	100	100	100	100	100	100
POR	1	16.31	16.27	16.27	16.29	16.35	16.44	16.24	16.31
UVCC	2	38.89	38.76	38.64	38.88	38.78	38.70	38.64	38.89
VCF	3	33.25	33.23	33.22	33.24	33.26	32.97	33.04	33.25
OVCC	4	72.40	72.67	72.55	72.41	72.60	72.43	72.56	72.40
TSE	5	66.75	66.77	66.78	66.76	66.74	67.03	66.96	66.75
MSH	6	61.11	61.24	61.36	61.12	61.22	61.30	61.36	61.11
SAT	7	56.59	56.45	56.67	56.53	56.73	56.58	56.75	56.59
MSL	8	44.54	44.29	44.41	44.53	44.31	44.44	44.24	44.54
SMM	9	21.95	21.80	22.04	21.94	21.87	21.84	21.84	21.95
ABI or SLR	10	27.60	27.33	27.45	27.59	27.40	27.57	27.44	27.60
ACD	11	84.07	84.10	84.09	84.06	83.99	83.89	84.09	84.07

[1] IC must be reset to clear flag.

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Error Reporting in ABI/UVW

Error reporting when using ABI/UVW requires the transmission of angle information to be interrupted. When using ABI/UVW, it is recommended to use an additional output (PWM or SPI).

For more information on ABI / UVW error reporting please contact Allegro MicroSystems.

Turns Count and Low Power Mode Error Checking

The A33115 monitors and keeps track of Turns Counts during normal operation and Low Power Mode (LPM). The turns count value, as reported in normal power model, is also included in the A33115 Safety Analysis for ASIL D operation.

The A33115 features diagnostic on the turns count during normal operating and LPM. Status and error conditions of the turns count report using two bits, turns count warning (TCW_ERROR) and turns count overflow (TCO_ERROR). The flags are reported in the registers that include the turns count value. A list is shown in Table 21 below.

Table 21

Turns Count Flag	Description	Primary Memory Location
TCW_ERROR_P	Turns Count Warning Primary Channel	0x15 [13]
TCO_ERROR_P	Turns Count Overflow Primary Channel	0x15 [12]
TCW_ERROR_S	Turns Count Warning Primary Channel	0x1C [13]
TCO_ERROR_S	Turns Count Overflow Primary Channel	0x1C [12]
TCW_ERROR_LATCH_P	Turns Count Warning Primary Channel	0x1B [13]
TCO_ERROR_LATCH_P	Turns Count Overflow Primary Channel	0x1B [12]
TCW_ERROR_LATCH_S	Turns Count Warning Primary Channel	0x1D [13]
TCO_ERROR_LATCH_S	Turns Count Overflow Primary Channel	0x1D [12]

The TCW_ERROR or TCO_ERROR flags set in normal operation are latched and saved in LPM until cleared. The error flags set in LPM remain, after returning to normal operation, until cleared. The TCW_ERROR and TCO_ERROR flags only clear after a reset. The external controller may execute a reset of the Turns Count using the CTRL register (primary: 0x0F). More information is available in the Primary Serial Interface Register Reference.

On the transition from LPM to normal operating mode, indicated by BACK_FROM_LPM (primary: 0x0E [6]), the turns count value is compared to the initial angle. During this transition the TCW_ERROR flags are set if the calculated angle from the turns count values compared to the initial angle differ by more than 135 degrees.

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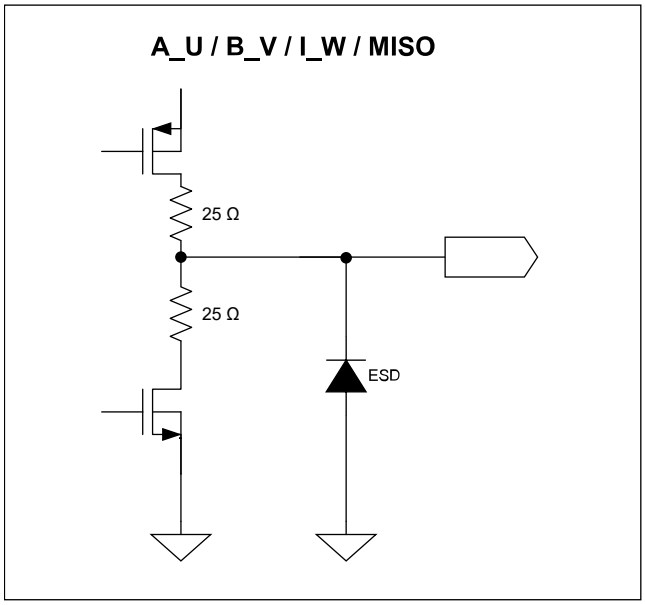
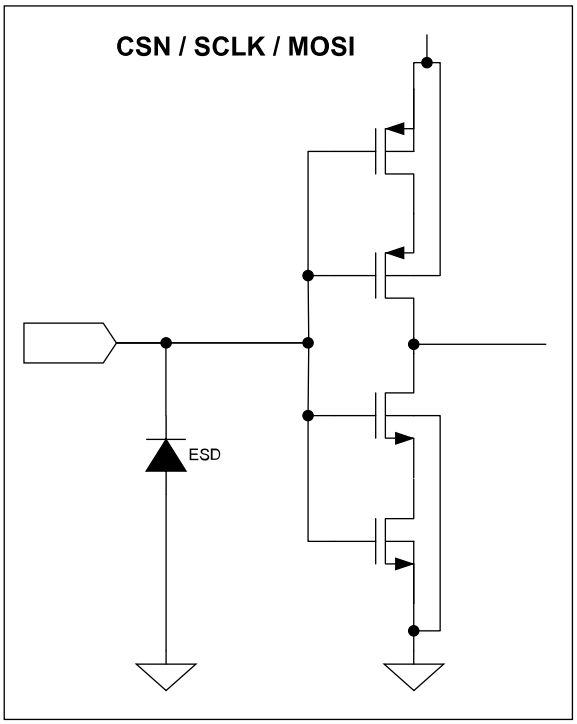
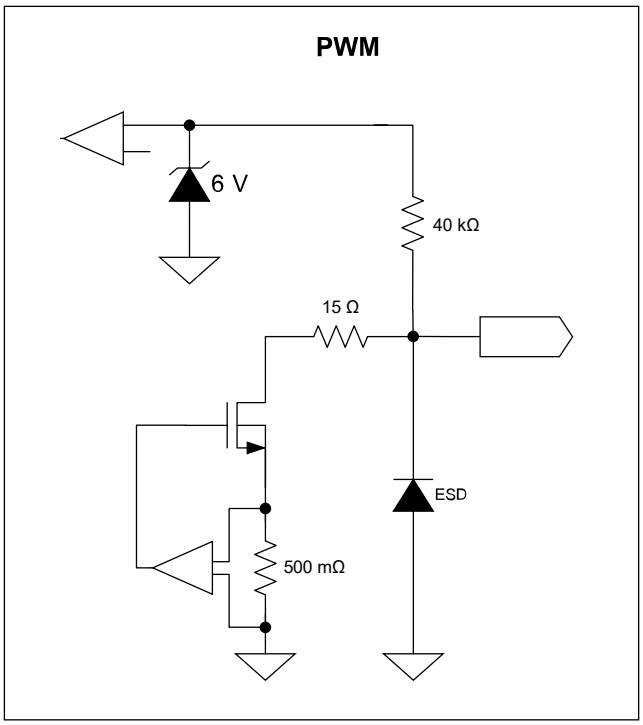
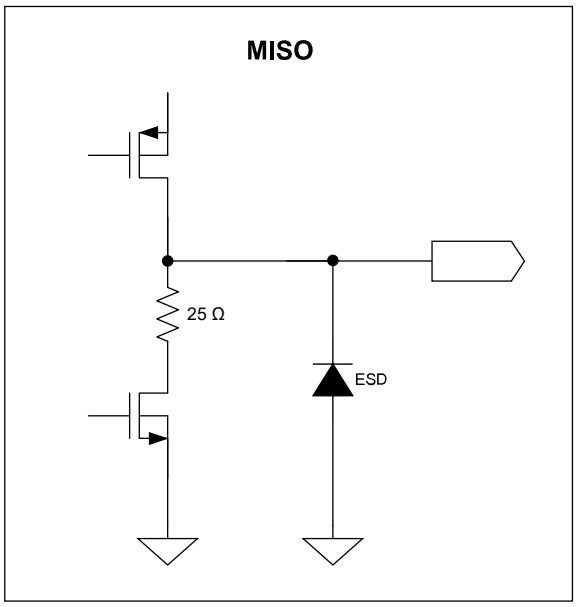
I/O STRUCTURES









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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

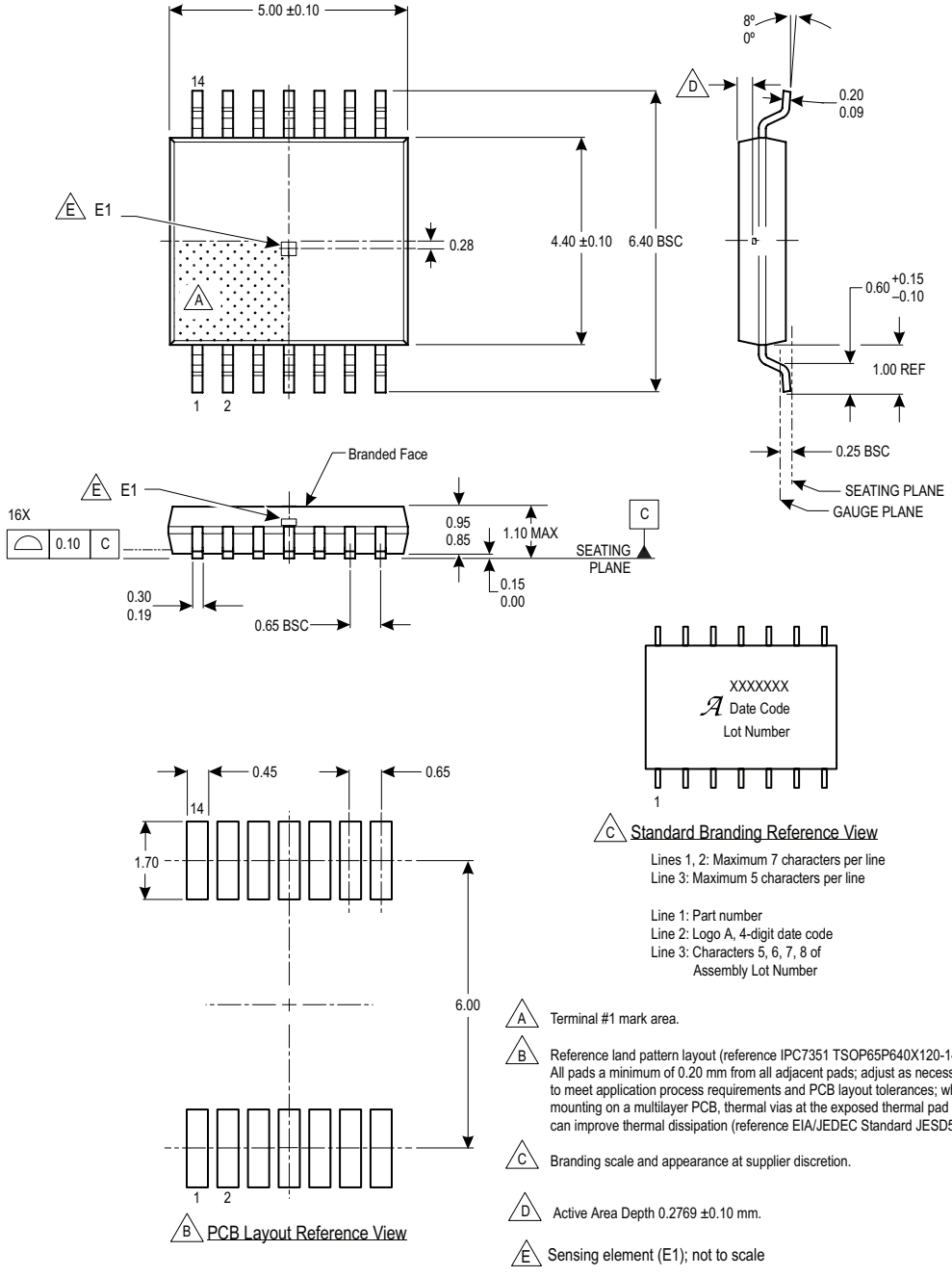

Figure 35: Package LE, 14-Pin TSSOP

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Revision History

Number	Date	Description
–	May 22, 2023	Initial release
1	September 28, 2023	Updated ASIL D status (page 1).
2	February 5, 2024	Added I/O Structures section (page 74).
3	July 8, 2024	Updated SPI and ABI tables (page 6); added Maximum Sourcing Current and Maximum Sinking Current characteristics (page 7); updated Input Magnetic Flux Density minimum values and footnotes (page 8); updated ABI Count-Up Following Power-Up section (page 16); updated CRC section (page 30); updated MISO Response on Receipt of Bad CRC section (page 31); updated EEPROM Margin Check section (page 36); updated INDIRECT_WR_ADDR section (page 39); added default values to Addresses 0x3 through 0x3F (pages 57 to 66); updated ABI_SLEW_RATE section (page 61); updated ABI_COUNT_UP_RPT_EN, ABI_SR_DLY_EN, and ABI_ERR_RPT_MODE sections (page 64); updated EE_TEST_ADDR section (page 68); updated BIST_START section (page 69).
4	August 19, 2024	Input Magnetic Flux Density minimum values and footnote (page 8).

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