Adjustable Frequency Buck or Buck-Boost Pre-Regulator with Synchronous Buck, 3 LDOs, Pulse-Width Window Watchdog, NPOR, and POK5V

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- 3.5 to 36 V_{IN} operating range, 40 V_{IN} maximum
- Buck or buck-boost pre-regulator (VREG)
- Adjustable PWM switching frequency: 250 kHz to 2.4 MHz
- PWM frequency can be synchronized to external clock
- Synchronous buck regulator (ADJ) delivers 0.8 to 3.3 V
- Two 5 V LDOs for "local" sensors ($V5_{SNR}$) and communications ($V5_{CAN}$) with foldback short-circuit protections
- 5 V internal tracking LDO for remote sensors with foldback short-circuit and short-to-battery protections (V5P)
- TRACK sets FB_{ADJ} or $V5_{SNR}$ as the reference for V5P
- Programmable pulse-width window watchdog (PWWD) with scalable activation delay and selectable tolerance
- Internal Watchdog (WD) CLK with ±5% accuracy
- Accepts external WD CLK for improving accuracy
- Active-low Watchdog Enable pin (WD_{ENn})
- Dual bandgaps for increased reliability: BG_{VREF}, BG_{FAULT}
- Power-on reset (NPOR) with fixed delay of 2 ms
- Power OK output for 5 V LDOs UV/OV (POK5V)
- Logic enable input for microprocessor control (ENB)

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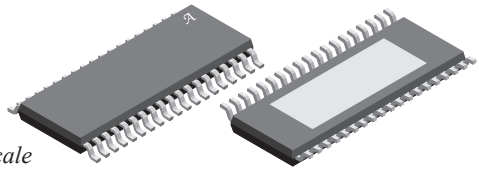
APPLICATIONS

- □ Electronic power steering (EPS) modules
- □ Automotive power trains
- □ CAN power supplies
- □ High-temperature applications

PACKAGE: 38-Pin eTSSOP (suffix LV)



Not to scale

DESCRIPTION

The A4411 is a power management IC that can be configured as a buck or buck-boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections. The output of the pre-regulator supplies a 5 V / 150 mA_{MAX} LDO for "local" sensors ($V5_{SNR}$), a 5 V / 200 mA_{MAX} LDO for communications ($V5_{CAN}$), a 5 V / 120 mA_{MAX} tracking/protected LDO for remote sensors (V5P), and a 0.8 to 3.3 V / 800 mA_{MAX} adjustable synchronous buck regulator (ADJ). Designed to supply CAN or microprocessor power supplies in high-temperature environments, the A4411 is ideal for underhood applications.

The A4411 can be enabled by its logic level (ENB) or high-voltage (ENBAT) input. The A4411 includes a TRACK pin to set the reference of the V5P tracking regulator to either $V5_{SNR}$ or the buck FB_{ADJ} pin, so the A4411 can be adapted across multiple platforms with different sensors and supply rails.

Diagnostic outputs from the A4411 include a power-on-reset output (NPOR) with a fixed delay, an ENBAT status output, and a Power OK output for the 5 V LDOs (POK5V). Dual bandgaps, one for regulation and one for fault checking, improve long-term reliability of the A4411.

The A4411 contains a Pulse-Width Window Watchdog (PWWD) that can be programmed to detect pulse widths from 1 to 2 ms (WD_{ADJ}). The watchdog has an activation delay that scales with the pulse-width setting to accommodate processor startup. The tolerance of the Watchdog's Window can be set to ±8%, ±13%, or ±18% using the WD_{TOL} pin. The watchdog has an active-low enable pin (WD_{ENn}) to facilitate initial factory programming or field reflash programming.

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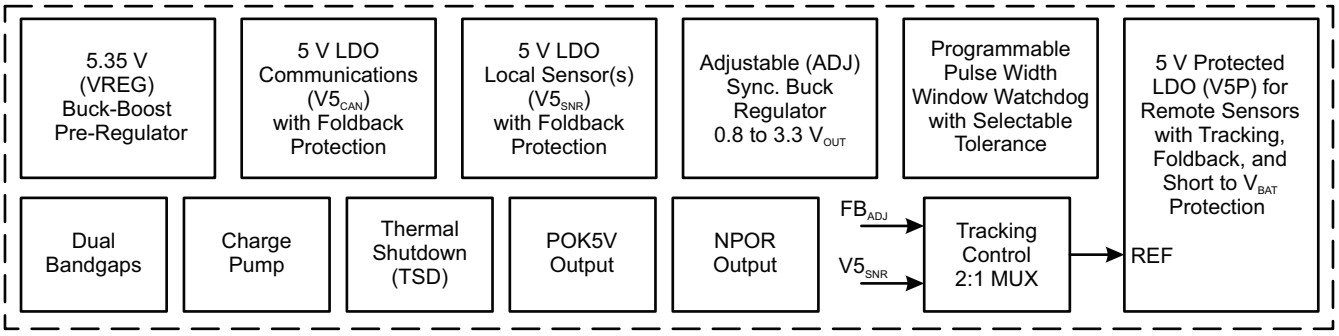

A4411 Simplified Block Diagram

FEATURES AND BENEFITS (continued)

- High-voltage ignition enable input (ENBAT)
- ENBAT status indicator output (ENBATS)
- SLEW rate control pin helps reduce EMI/EMC
- Frequency dithering helps reduce EMI/EMC
- OV and UV protection for all four CPU supply rails
- Pin-to-pin and pin-to-ground tolerant at every pin
- Thermal shutdown protection
- −40°C to 150°C junction temperature range

DESCRIPTION (continued)

Protection features include under- and overvoltage lockout on all four CPU supply rails. In case of a shorted output, all linear regulators feature foldback overcurrent protection. In addition, the V5P output is protected from a short-to-battery event. Both switching regulators include pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, missing asynchronous diode protection (VREG only), and thermal shutdown.

The A4411 is supplied in a low-profile 38-lead eTSSOP package (suffix “LV”) with exposed power pad.

SELECTION GUIDE

Part Number	Temperature Range	Package	Packing [1]	Lead Frame
A4411KLVTR-T	–40 to 135°C	38-pin eTSSOP with thermal pad	4000 pieces per 7-inch reel	100% matte tin

[1] Contact Allegro for additional packing options.

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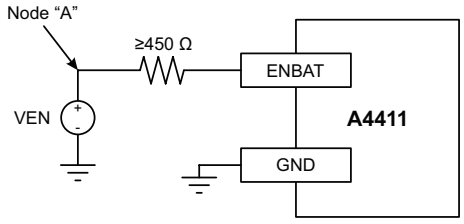
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBATx}	With current limiting resistor [2]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBATx}		±75	mA
LX1, SLEW			−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{VIN} + 3 V	V
VCP, CP1, CP2			−0.3 to 50	V
V5P	V_{V5P}	Independent of V_{VIN}	−1 to 40	V
All other pins			−0.3 to 7	V
Ambient Temperature	T_A	Range K for automotive	−40 to 135	°C
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

[2] The higher ENBAT ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	eTSSOP-38 (LV) Package	30	°C/W

[1] Additional thermal information available on the Allegro website.

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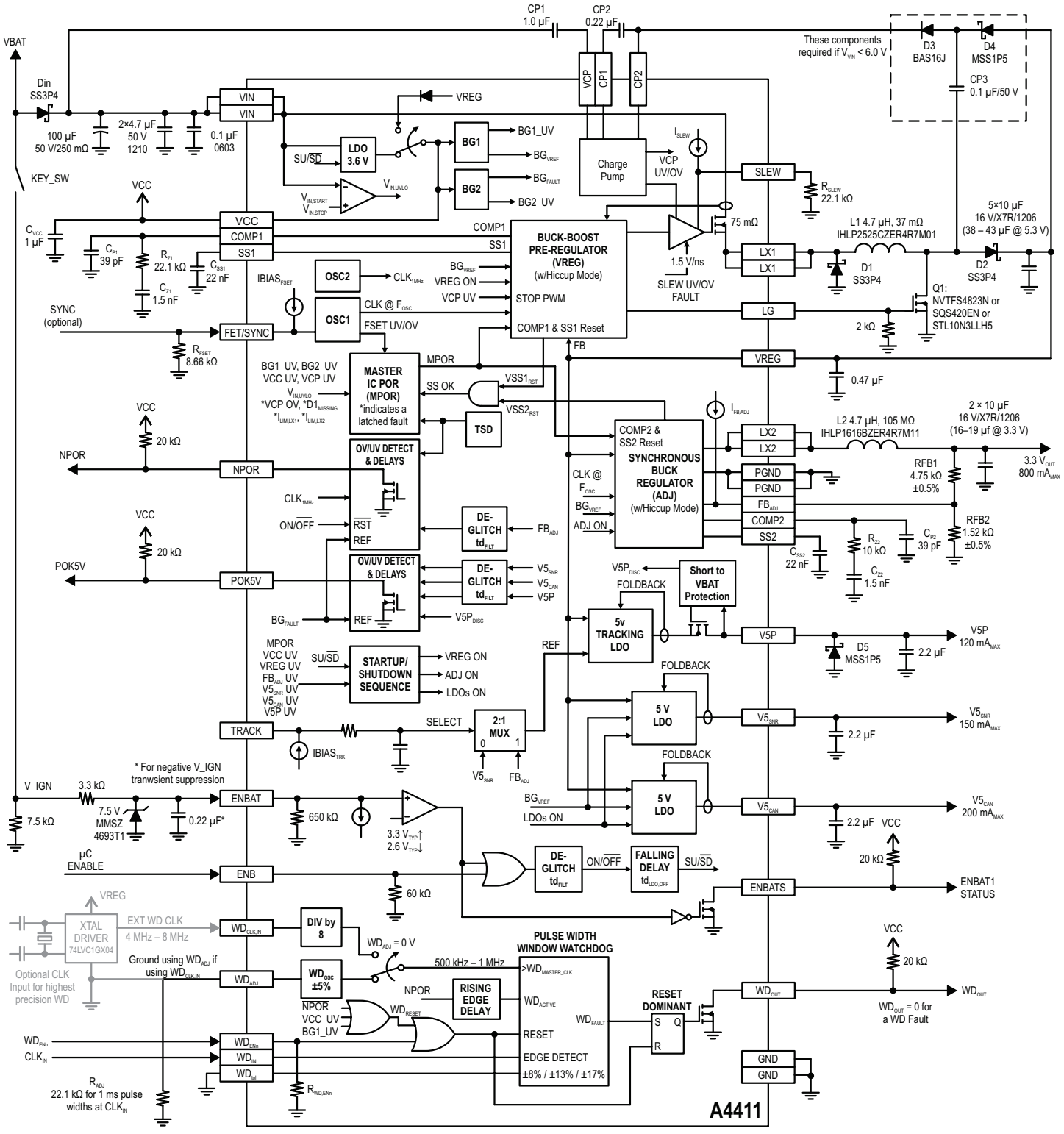

Functional Block Diagram/Typical Schematic

Buck-Boost Mode (f_{OSC} = 2 MHz)

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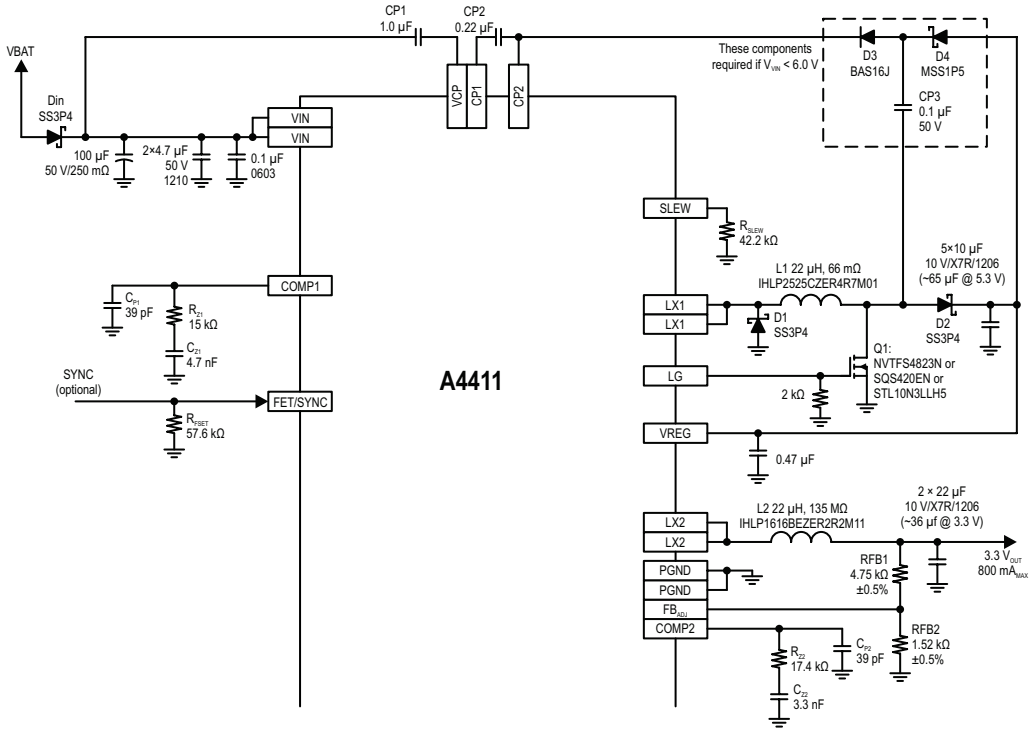
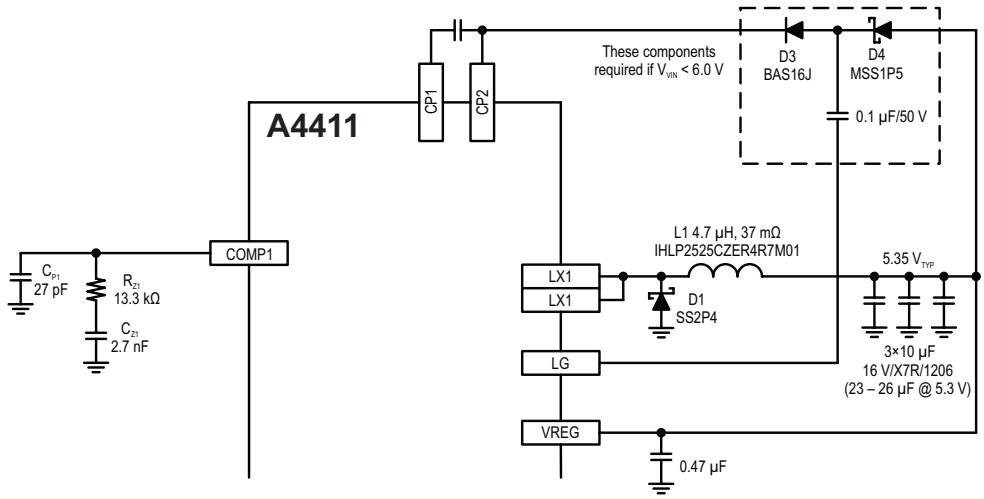


Functional Block Diagram Modifications for Buck-Boost Mode (f_{OSC} = 400 kHz)



Functional Block Diagram Modifications for Buck Only Mode, f_{OSC} = 2 MHz

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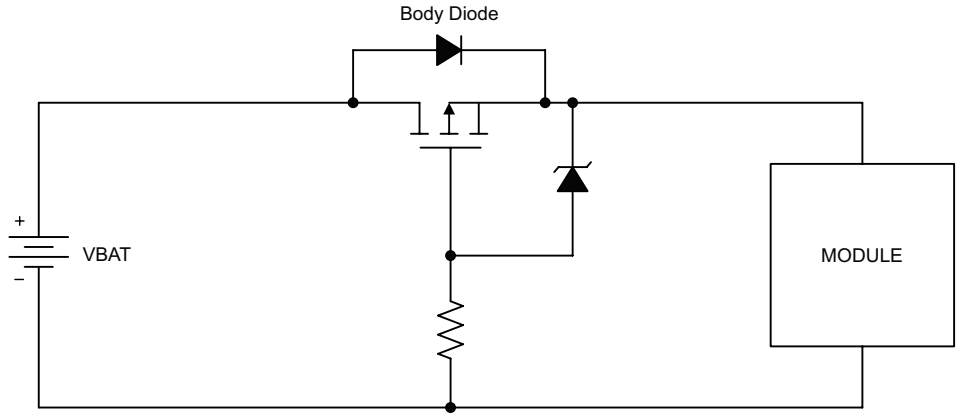
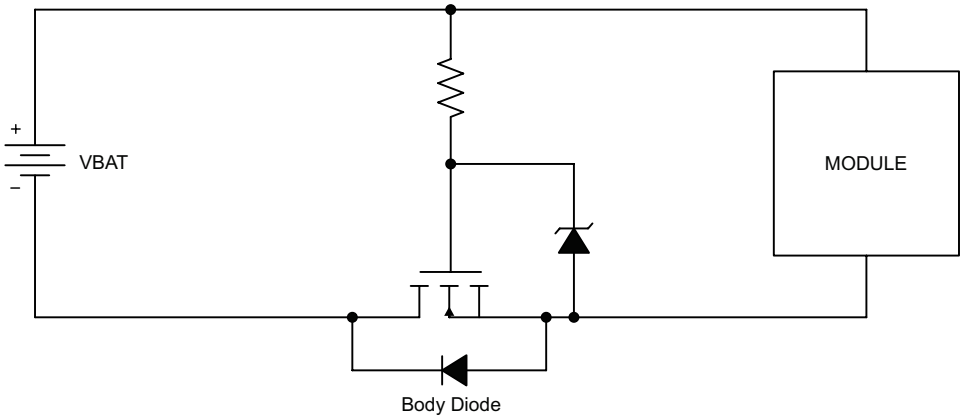


Functional Block Diagram Using a PMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D_{IN})



Functional Block Diagram Using an NMOS FET for Reverse-Battery Protection Instead of a Series Schottky Diode (D_{IN})

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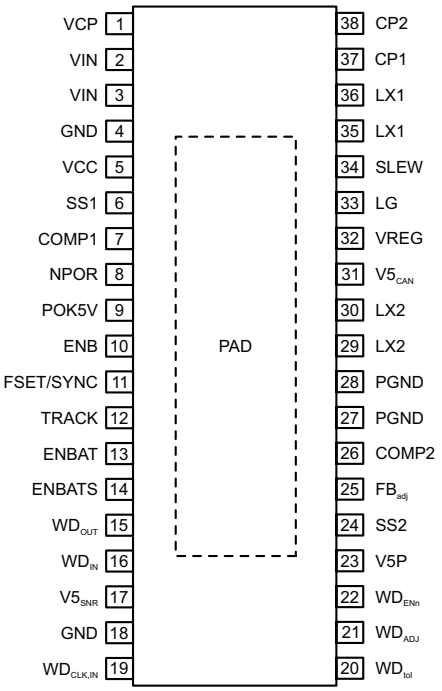

Package LV, 38-Pin eTSSOP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2, 3	VIN	Input voltage pins
4, 18	GND	Ground pin
5	VCC	Internal voltage regulator bypass capacitor pin
6	SS1	Soft-start programming pin for the buck-boost pre-regulator
7	COMP1	Error amplifier compensation network pin for the buck-boost pre-regulator
8	NPOR	Active-low, open-drain regulator fault detection output
9	POK5V	Power OK output indicating when either the $V5_{SNR}$, $V5_{CAN}$, or V5P rail is undervoltage (UV)
10	ENB	Logic-enable input from a microcontroller or DSP
11	FSET/ SYNC	Frequency setting and synchronization input
12	TRACK	Tracking control: Open/High – V5P tracks the FB_{ADJ} pin, GND/Low – V5P tracks $V5_{SNR}$
13	ENBAT	Ignition enable input from the key/switch via a series resistor
14	ENBATS	Open-drain ignition status output of ENBAT
15	WD_{OUT}	Watchdog output, latched low if a watchdog fault is detected
16	WD_{IN}	Watchdog pulse train input from a microcontroller or DSP
17	$V5_{SNR}$	5 V regulator output for local sensor(s)
19	$WD_{CLK,IN}$	WD clock input for highest WD accuracy. If this pin is used the WD_{ADJ} pin must be grounded.
20	WD_{TOL}	Selectable watchdog tolerance: low = ±8%, float = ±13%, high (to VCC) = ±18%
21	WD_{ADJ}	The watchdog window time is set from 1 to 2 ms by connecting R_{ADJ} from this pin to ground
22	WD_{ENn}	Active-low watchdog enable input from a microcontroller or DSP. Open/ Low = WD is enabled, High = WD is disabled
23	V5P	5 V tracking/protected regulator output
24	SS2	Soft-start programming pin for the adjustable synchronous buck regulator
25	FB_{ADJ}	Feedback pin for the adjustable synchronous buck regulator
26	COMP2	Error amplifier compensation network pin for the adjustable synchronous buck regulator
27, 28	PGND	Power ground for the adjustable synchronous regulator / gate driver
29, 30	LX2	Switching node for the adjustable synchronous buck regulator
31	$5V_{CAN}$	5 V regulator output for communications
32	VREG	Output of the pre-regulator and input to the LDOs and adjustable synchronous buck
33	LG	Boost gate drive output for the buck-boost pre-regulator
34	SLEW	Slew rate adjustment for the rise time of LX1
35, 36	LX1	Switching node for the buck-boost pre-regulator
37	CP1	Charge pump capacitor connection
38	CP2	Charge pump capacitor connection
–	PAD	

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ELECTRICAL CHARACTERISTICS [1]: Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage [3]	V_{VIN}	Buck-Boost Mode, after V_{VIN} > VIN_{START}, and V_{ENB} > 2 V or V_{ENBAT} > 3.5 V, NPOR = 1, POK5V = 1	3.5	13.5	36	V
		Buck Only Mode, after V_{VIN} > VIN_{START}, and V_{ENB} > 2 V or V_{ENBAT} > 3.5 V, NPOR = 1 and POK5V = 1	5.8	13.5	36	V
VIN UVLO Start Voltage	VIN_{START}	V_{VIN} rising, Buck or Boost Mode	5.10	5.40	5.80	V
VIN UVLO Stop Voltage	VIN_{STOP}	V_{VIN} falling, Buck or Boost Mode	2.88	3.04	3.30	V
VIN UVLO Hysteresis	VIN_{HYS}	VIN_{START} – VIN_{STOP}	–	2.7	–	V
VIN Dropout Voltages Buck Mode, V_{VIN} Falling [2]	$VIN_{STOP1,BUCK}$	NPOR = 1, POK5V ↓	–	5.1	–	V
	$VIN_{STOP2,BUCK}$	V_{VCP} < $V_{CPUV,L}$ and NPOR ↓, POK5V = 0	–	3.8	–	V
Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{ENBAT} ≥ 3.6 V or V_{ENB} ≥ 2 V, V_{VREG} = 5.6 V (no PWM)	–	13	–	mA
	$I_{Q,SLEEP}$	V_{VIN} = 13.5 V, V_{ENBAT} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	–	–	25	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	R_{FSET} = 8.66 kΩ	1.8	2	2.2	MHz
		R_{FSET} = 20.5 kΩ [2]	–	1	–	MHz
		R_{FSET} = 57.6 kΩ [2]	343	400	457	kHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±12	–	%
Dither/Slew START Threshold	$VIN_{DS,ON}$		8.5	9	9.6	V
Dither/Slew STOP Threshold	$VIN_{DS,OFF}$		7.8	8.3	8.9	V
VIN Dithering/Slew Hysteresis			–	700	–	mV
CHARGE PUMP (VCP)						
Output Voltage	V_{VCP}	V_{VCP} – V_{VIN}, V_{VIN} = 13.5 V, V_{VREG} = 5.5 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	4.1	6.6	–	V
		V_{VCP} – V_{VIN}, V_{VIN} = 6.5 V, V_{VREG} = 5.5 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	3.1	3.8	–	V
Switching Frequency	$f_{SW,CP}$		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.65	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	155	170	185	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Buck Output Voltage – Regulating	V_{VREG}	V_{VIN} = 13.5 V, ENB = 1, 0.1 A < I_{VREG} < 1.25 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$PWM1_{OFFS}$	V_{COMP1} for 0% duty cycle	–	400	–	mV
LX1 Rising Slew Rate Control [2]	$LX1_{RISE}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 22.1 kΩ	–	0.9	–	V/ns
		V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 249 kΩ	–	0.3	–	V/ns
LX1 Falling Slew Rate [2]	$LX1_{FALL}$	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time	$t_{ON,MIN,BUCK}$		–	100	150	ns
Buck Maximum Duty Cycle	$D_{MAX,BUCK}$	$t_{OFF,BUCK}$ < 50 ns	–	100	–	%
Boost Minimum Off-Time	$t_{ON,MIN,BST}$		100	130	230	ns
Boost Duty Cycle	$D_{MIN,BST}$	After V_{VIN} > VIN_{START}, V_{VIN} = 6.5 V	–	20	–	%
	$D_{MAX,BST}$	After V_{VIN} > VIN_{START}, V_{VIN} = 3.5 V	–	58	68	%
COMP1 to LX1 Current Gain	gm_{POWER1}		–	4.5	–	A/V
Slope Compensation [2]	S_{E1}	f_{OSC} = 2 MHz	1.04	1.48	1.92	A/µs
		f_{OSC} = 400 kHz	0.22	0.33	0.44	A/µs
INTERNAL MOSFET						
MOSFET On-Resistance	R_{DSon}	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	–	50	65	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.1 A	–	75	90	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	150	180	mΩ
MOSFET Leakage	$I_{FET,LKG}$	IC disabled, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [3]	–	–	10	µA
		IC disabled, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open-Loop Voltage Gain	A_{VOL1}		–	60	–	dB
Transconductance	gm_{EA1}	V_{SS1} = 750 mV	550	750	950	µA/V
		V_{SS1} = 500 mV	275	375	475	µA/V
Output Current	I_{EA1}		–	±75	–	µA
Maximum Output Voltage	$EA1_{VO(max)}$		1.3	1.7	2.1	V
Minimum Output Voltage	$EA1_{VO(min)}$		–	–	300	mV
COMP1 Pull-Down Resistance	R_{COMP1}	HICCUP1 = 1 or FAULT1 = 1 or IC disabled, latched until V_{SS1} < $VSS1_{RST}$	–	1	–	kΩ

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG,ON}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.5	V
LG Low Output Voltage	$V_{LG,OFF}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG,ON}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG,OFF}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS1 Offset Voltage	$VSS1_{OFFS}$	V_{SS1} rising due to $ISS1_{SU}$	–	400	–	mV
SS1 Fault/Hiccup Reset Voltage	$VSS1_{RST}$	V_{SS1} falling due to HICCUP1 = 1 or FAULT1 = 1 or IC disabled	140	200	275	mV
SS1 Startup (Source) Current	$ISS1_{SU}$	V_{SS1} = 100 mV, HICCUP1 = FAULT1 = 0	−10	−20	−30	µA
SS1 Hiccup (Sink) Current	$ISS1_{HIC}$	V_{SS1} = 0.5 V, HICCUP1 = 1	5	10	15	µA
SS1 Delay Time	$t_{SS1,DLY}$	C_{SS1} = 22 nF	–	440	–	µs
SS1 Ramp Time	t_{SS1}	C_{SS1} = 22 nF	–	880	–	µs
SS1 Pull-Down Resistance	RPD_{SS1}	FAULT1 = 1 or IC disabled, latched until V_{SS1} < $VSS1_{RST}$	–	3	–	kΩ
SS1 PWM Frequency Foldback	$f_{SW1,SS}$	0 V < V_{VREG} < 1.3 V_{TYP}	–	f_{OSC}/4	–	–
		1.3 V < V_{VREG} < 2.7 V_{TYP}	–	f_{OSC}/2	–	–
		V_{VREG} > 2.7 V_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup1 OCP PWM Counts	$t_{HIC1,OCP}$	V_{SS1} > $V_{HIC1,EN}$, V_{VREG} < 1.3 V_{TYP}, V_{COMP} = $EA1_{VO(max)}$	–	30	–	PWM cycles
		V_{SS1} > $V_{HIC1,EN}$, V_{VREG} > 1.3 V_{TYP}, V_{COMP} = $EA1_{VO(max)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM1,ton(min)}$	t_{ON} = $t_{ON(MIN)}$	3.8	4.3	4.8	A
LX1 Short-Circuit Current Limit	$I_{LIM,LX1}$	Latched off after 1 detection	7.5	10	–	A
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D,OPEN}$		−1.4	−1.1	−0.8	V
Time Filtering [2]	$t_{D,OPEN}$		50	–	250	ns

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR [1]:

Valid at 3.6 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FEEDBACK REFERENCE VOLTAGE						
Reference Voltage	$V_{FB,ADJ}$		787	800	813	mV
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$PWM2_{OFFS}$	V_{COMP2} for 0% duty cycle	–	350	–	mV
High-Side MOSFET Minimum On-Time	$t_{ON(MIN)}$		–	65	105	ns
High-Side MOSFET Minimum Off-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, t_{NO}	–	80	110	ns
Gate Driver Non-Overlap Time [2]	t_{NO}		–	15	–	ns
COMP2 to LX2 Current Gain	gm_{POWER2}		–	2.5	–	A/V
Slope Compensation [2]	S_{E2}	f_{OSC} = 2 MHz	0.45	0.63	0.81	A/µs
		f_{OSC} = 400 kHz	0.12	0.14	0.19	A/µs
INTERNAL MOSFETS						
High-Side MOSFET On-Resistance	$R_{DSon(HS)}$	T_A = 25°C [3], I_{DS} = 100 mA	–	150	180	mΩ
		I_{DS} = 100 mA	–	–	300	mΩ
LX2 Node Rise/Fall Time [2]	$t_{R/F,LX2}$	V_{VREG} = 5.5 V	–	12	–	ns
High-Side MOSFET Leakage [1]	$I_{DSS\ (HS)}$	IC disabled, V_{LX2} = 0 V, V_{VREG} = 5.5 V, –40°C < T_J < 85°C [3]	–	–	2	µA
		IC disabled, V_{LX2} = 0 V, V_{VREG} = 5.5 V, −40°C < T_J < 150°C	–	3	15	µA
Low-Side MOSFET On-Resistance	$R_{DSon(LS)}$	T_A = 25°C [3], I_{DS} = 100 mA	–	55	65	mΩ
		I_{DS} = 100 mA	–	–	110	mΩ
Low-Side MOSFET Leakage [1]	$I_{DSS\ (LS)}$	IC disabled, V_{LX2} = 5.5 V, –40°C < T_J < 85°C [3]	–	–	1	µA
		IC disabled, V_{LX2} = 5.5 V, −40°C < T_J < 150°C	–	4	10	µA
ERROR AMPLIFIER						
Feedback Input Bias Current [1]	$I_{FB,\ ADJ}$	V_{COMP2} = 0.8 V, $V_{FB,ADJ}$ regulated so that I_{COMP2} = 0 A	–	–150	−350	nA
Open-Loop Voltage Gain [2]	A_{VOL2}		–	60	–	dB
Transconductance	gm_{EA2}	I_{COMP2} = 0 µA, V_{SS2} > 500 mV	550	750	950	µA/V
		0 V < V_{SS2} < 500 mV	–	250	–	µA/V
Source and Sink Current	I_{EA2}	V_{COMP2} = 1.5 V	–	±50	–	µA
Maximum Output Voltage	$EA2_{VO(max)}$		1.00	1.25	1.50	V
Minimum Output Voltage	$EA2_{VO(min)}$		–	–	150	mV
COMP2 Pull-Down Resistance	R_{COMP2}	HICCUP2 = 1 or FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS2} < $VSS2_{RST}$	–	1.5	–	kΩ

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

Continued on next page...

ELECTRICAL CHARACTERISTICS – ADJUSTABLE SYNCHRONOUS BUCK REGULATOR (continued) [1]:

Valid at 3.6 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SOFT-START						
SS2 Offset Voltage	$V_{SS2,OFFS}$	V_{SS2} rising due to $I_{SS2,SU}$	120	200	270	mV
SS2 Fault/Hiccup Reset Voltage	$V_{SS2,RST}$	V_{SS2} falling due to HICCUP2 = 1 or FAULT2 = 1 or IC disabled	–	100	120	mV
SS2 Startup (Source) Current	$I_{SS2,SU}$	V_{SS2} = 1 V, HICCUP2 = FAULT2 = 0	−10	–20	−30	µA
SS2 Hiccup (Sink) Current	$I_{SS2,HIC}$	V_{SS2} = 0.5 V, HICCUP2 = 1	5	10	20	µA
SS2 to V_{ADJ} Delay Time	$t_{SS2,DLY}$	C_{SS2} = 10 nF	–	100	–	µs
$V_{FB,ADJ}$ Soft Start Ramp Time	t_{SS2}	C_{SS2} = 10 nF	–	400	–	µs
SS2 Pull Down Resistance	RPD_{SS2}	FAULT2 = 1 or IC disabled, latched until V_{SS2} < $VSS2_{RST}$	–	2	–	kΩ
SS2 PWM Frequency Foldback	$f_{SW2,SS}$	$V_{FB,ADJ}$ < 300 mV_{TYP}	–	f_{OSC}/4	–	–
		300 mV_{TYP} < $V_{FB,ADJ}$ < 500 mV_{TYP}	–	f_{OSC}/2	–	–
		$V_{FB,ADJ}$ > 500 mV_{TYP}	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup2 OCP Enable Threshold	$V_{HIC2,EN}$	V_{SS2} rising	–	1.2	–	V
Hiccup2 OCP Counts	$t_{HIC2,OCP}$	V_{SS2} > $V_{HIC2,EN}$, $V_{FB,ADJ}$ < 300 mV_{TYP}	–	30	–	PWM cycles
		V_{SS2} > $V_{HIC2,EN}$, $V_{FB,ADJ}$ > 300 mV_{TYP}	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM2,5\%}$	Duty cycle = 5%	1.8	2.1	2.4	A
	$I_{LIM2,90\%}$	Duty cycle = 90%	1.2	1.6	2.0	A
LX2 Short-Circuit Protection	$V_{LIM,LX2}$	V_{LX2} stuck low for more than 60 ns, Hiccup mode after 1 detection	–	V_{VREG} –1.2 V	–	V

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS – LINEAR REGULATOR (LDO) SPECIFICATIONS [1]:

Valid at 3.5 V < V_{IN} < 36 V, −40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
$V5_{SNR}$, $V5_{CAN}$, AND V5P LINEAR REGULATORS						
$V5_{SNR}$ Accuracy and Load Regulation	$V_{V5,SNR}$	10 mA < $I_{V5,SNR}$ < 150 mA, V_{VREG} = 5.25 V	4.9	5	5.1	V
$V5_{SNR}$ Output Capacitance [2]	$C_{OUT,V5,SNR}$		1	–	22	µF
$V5_{CAN}$ Accuracy and Load Regulation	$V_{V5,CAN}$	10 mA < $I_{V5,CAN}$ < 200 mA, V_{VREG} = 5.25 V	4.9	5	5.1	V
$V5_{CAN}$ Output Capacitance [2]	$C_{OUT,V5,CAN}$		1	–	22	µF
V5P Accuracy and Load Regulation	V_{V5P}	10 mA < I_{V5P} < 120 mA, V_{VREG} = 5.25 V	4.875	5	5.125	V
V5P Output Capacitance [2]	$C_{OUT,V5P}$		1.6	2.2	4.1	µF
V5 and V5P Minimum Output Voltage [2]	$V_{V5x,MIN1}$	V_{VIN} = 5.35 V, V_{VREG} = 5.19 V, V_{VCP} = 9.4 V, $I_{V5,SNR}$ = 50 mA, $I_{V5,CAN}$ = 200 mA, I_{V5P} = 75 mA, I_{3V3} = 700 mA (510 mA to VREG)	4.86	4.95	–	V
	$V_{V5x,MIN2}$	V_{VIN} = 4.50 V, V_{VREG} = 4.34 V, V_{VCP} = 8.5 V, $I_{V5,SNR}$ = 50 mA, $I_{V5,CAN}$ = 200 mA, I_{V5P} = 75 mA, I_{3V3} = 700 mA (610 mA to VREG)	4.06	4.29	–	V
V5P TRACKING						
V5P/ADJ Tracking Ratio		V_{V5P} ÷ $V_{FB,ADJ}$	6.218	6.250	6.282	–
V5P/ADJ Tracking Accuracy	$TRACK_{ADJ}$	735 mV < $V_{FB,ADJ}$ < 800 mV, TRACK = 1, I_{V5P} = 10 mA	−0.5	–	+0.5	%
V5P/$V5_{SNR}$ Tracking Accuracy	$TRACK_{V5,SNR}$	4.5 V < $V_{V5,SNR}$ < 5 V, TRACK = 0, I_{V5P} = $I_{V5,SNR}$ = 75 mA	−25	–	+25	mV
V5P OVERCURRENT PROTECTION						
V5P Current Limit [1]	$V5P_{ILIM}$	V_{V5P} = 5 V	−140	−200	–	mA
V5P Foldback Current [1]	$V5P_{IFBK}$	V_{V5P} = 0 V	−10	–	−90	mA
$V5_{SNR}$ OVERCURRENT PROTECTION						
$V5_{SNR}$ Current Limit [1]	$V5_{SNR,ILIM}$	$V_{V5,SNR}$ = 5 V	−175	−245	–	mA
$V5_{SNR}$ Foldback Current [1]	$V5_{SNR,IFBK}$	$V_{V5,SNR}$ = 0 V	−35	−70	−105	mA
$V5_{CAN}$ OVERCURRENT PROTECTION						
$V5_{CAN}$ Current Limit [1]	$V5_{CAN,ILIM}$	$V_{V5,CAN}$ = 5 V	−230	−325	–	mA
$V5_{CAN}$ Foldback Current [1]	$V5_{CAN,IFBK}$	$V_{V5,CAN}$ = 0 V	−50	−95	−140	mA
V5P & $V5_{SNR}$, AND $V4_{CAN}$ STARTUP TIMING						
V5P Startup Time [2]		C_{V5P} ≤ 2.9 µF, Load = 42 Ω ±5% (120 mA)	–	0.26	1.1	ms
$V5_{SNR}$ Startup Time [2]		$C_{V5,SNR}$ ≤ 2.9 µF, Load = 33 Ω ±5% (150 mA)	–	0.24	1	ms
$V5_{CAN}$ Startup Time [2]		$C_{V5,CAN}$ ≤ 2.9 µF, Load = 25 Ω ±5% (200 mA)	–	0.22	1	ms

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ELECTRICAL CHARACTERISTICS – CONTROL INPUTS [2]: Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGNITION ENABLE (ENBAT) INPUTS						
ENBAT Thresholds	$V_{ENBAT,H}$	V_{ENBAT} rising	2.9	3.1	3.5	V
	$V_{ENBAT,L}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT,HYS}$	$V_{ENBAT,H}$ – $V_{ENBAT,L}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT,BIAS}$	T_J = 25°C [3], V_{ENBAT} = 3.51 V	–	40	65	µA
		T_J = 150°C, V_{ENBAT} = 3.51 V	–	50	80	µA
ENBAT Pull-Down Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	650	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB,H}$	V_{ENB} rising	–	–	2	V
	$V_{ENB,L}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB,IN}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBAT FILTER/DEGLITCH						
Enable Filter/Deglitch Time	$EN_{td,FILT}$		10	15	20	µs
ENB/ENBAT SHUTDOWN DELAY						
LDO Shutdown Delay	$td_{LDO,OFF}$	Measure $td_{LDO,OFF}$ from the falling edge of ENB and ENBAT to the time when all LDOs begin to decay	15	50	100	µs
TRACK INPUTS						
TRACK Thresholds	V_{TH}	V_{TRACK} rising	–	–	2	V
	V_{TL}	V_{TRACK} falling	0.8	–	–	V
TRACK Bias Current [1]	$IBIAS_{TRK}$		–	−100	–	µA
FSET/SYNC INPUTS						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	800	–	mV
FSET/SYNC Bias Current	$IBIAS_{FSET}$		–	−100	–	nA
FSET/SYNC Open Circuit (Undercurrent) Detection Time	$V_{FSET/SYNC,UC}$	1 MHz PWM operation if open	–	3	–	µs
FSET/SYNC Short Circuit (Overcurrent) Detection Time	$V_{FSET/SYNC,OC}$	1 MHz PWM operation if shorted	–	3	–	µs
Sync. High Threshold	$SYNC_{VIH}$	V_{SYNC} rising	–	–	2	V
Sync. Low Threshold	$SYNC_{VIL}$	V_{SYNC} falling	0.5	–	–	V
Sync. Input Duty Cycle	DC_{SYNC}		–	–	80	%
Sync. Input Pulse Width	tw_{SYNC}		200	–	–	ns
Sync. Input Transition Times [2]	tt_{SYNC}		–	10	15	ns
SLEW INPUTS						
SLEW Pin Operating Voltage	V_{SLEW}		–	800	–	mV
SLEW Pin Open Circuit (Undercurrent) Detection Time	$V_{SLEW,UC}$	LX1 defaults to 1.5 V/ns if fault	–	3	–	µs
SLEW Pin Short Circuit (Overcurrent) Detection Time	$V_{SLEW,OC}$	LX1 defaults to 1.5 V/ns if fault	–	3	–	µs
SLEW Bias Current [1]	I_{SLEW}		–	−100	–	nA

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]:

Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR OV/UV PROTECTION THRESHOLDS						
FB_{ADJ} OV Thresholds	$V_{FB,ADJ,OV,H}$	$V_{FB,ADJ}$ rising	825	845	865	mV
	$V_{FB,ADJ,OV,L}$	$V_{FB,ADJ}$ falling	–	838	–	mV
FB_{ADJ} OV Hysteresis	$V_{FB,ADJ,OV,HYS}$	$V_{FB,ADJ,OV,H}$ – $V_{FB,ADJ,OV,L}$	3	7	14	mV
FB_{ADJ} UV Thresholds	$V_{FB,ADJ,UV,H}$	$V_{FB,ADJ}$ rising	–	762	–	mV
	$V_{FB,ADJ,UV,L}$	$V_{FB,ADJ}$ falling	735	755	775	mV
FB_{ADJ} UV Hysteresis	$V_{FB,ADJ,UV,HYS}$	$V_{FB,ADJ,UV,H}$ – $V_{FB,ADJ,UV,L}$	3	7	14	mV
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$td_{NPOR,ON}$	$V_{VFB,ADJ}$ > $V_{FB,ADJ,UV,H}$, see Figure 11 for timing details	1.6	2	2.4	ms
NPOR Turn-Off Delay	$td_{NPOR,OFF}$	ENB and ENBAT low for t > td_{FILT}, see Figure 11 for timing details	–	–	3	µs
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR,L}$	ENB or ENBAT high, V_{VIN} ≥ 2.5 V, I_{NPOR} = 4 mA	–	150	400	mV
		ENB or ENBAT high, V_{VIN} = 1.5 V, I_{NPOR} = 2 mA	–	–	800	mV
NPOR Leakage Current [1]	$I_{NPOR,LKG}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR AND POK5V OV DELAY TIME						
Overvoltage Detection Delay	td_{OV}	V5P, $V5_{SNR}$, $V5_{CAN}$, or FB_{ADJ} overvoltage detection delay time (two independent timers, NPOR and POK5V)	3.2	4	4.8	ms
NPOR AND POK5V UV FILTERING/DEGLITCH						
UV Filter/Deglitch Times	td_{FILT}	Applies to undervoltage of the FB_{ADJ}, $V5_{SNR}$, $V5_{CAN}$, and V5P voltages	10	15	20	µs
POK5V OV/UV PROTECTION THRESHOLDS						
$V5_{SNR}$ and $V5_{CAN}$ OV Thresholds	$V_{V5x,OV,H}$	V_{V5x} rising	5.15	5.33	5.50	V
	$V_{V5x,OV,L}$	V_{V5x} falling	–	5.30	–	V
$V5_{SNR}$ and $V5_{CAN}$ OV Hysteresis	$V_{V5x,OV,HYS}$	$V_{V5x,OV,H}$ – $V_{V5x,OV,L}$	15	30	50	mV
$V5_{SNR}$ and $V5_{CAN}$ UV Thresholds	$V_{V5x,UV,H}$	V_{V5x} rising	–	4.71	–	V
	$V_{V5x,UV,L}$	V_{V5x} falling	4.50	4.68	4.85	V
$V5_{SNR}$ and $V5_{CAN}$ UV Hysteresis	$V_{V5x,UV,HYS}$	$V_{V5x,UV,H}$ – $V_{V5x,UV,L}$	15	30	50	mV
V5P Output Disconnect Threshold	$V_{V5P,DISC}$	V_{V5P} rising	–	7.2	–	V
V5P OV Thresholds	$V_{V5P,OV,H}$	V_{V5P} rising	5.15	5.33	5.50	V
	$V_{V5P,OV,L}$	V_{V5P} falling	–	5.30	–	V
V5P OV Hysteresis	$V_{V5P,OV,HYS}$	$V_{V5P,OV,H}$ – $V_{V5P,OV,L}$	15	30	50	mV
V5P UV Thresholds	$V_{V5P,UV,H}$	V_{V5P} rising	–	4.71	–	V
	$V_{VP5,UV,L}$	V_{V5P} falling	4.50	4.68	4.85	V
V5P UV Hysteresis	$V_{V5P,UV,HYS}$	$V_{V5P,UV,H}$ – $V_{V5P,UV,L}$	15	30	50	mV

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]:

Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POK5V OUTPUT VOLTAGES						
POK5V Output Voltage	$V_{POK5V,L}$	ENB = 1 or ENBAT = 1, V_{VIN} ≥ 2.5 V, I_{POK5V} = 4 mA	–	150	400	mV
		ENB = 1 or ENBAT= 1, V_{VIN} = 1.5 V, I_{POK5V} = 2 mA	–	–	800	mV
POK5V Leakage Current	$I_{POK5V,LKG}$	V_{POK5V} = 3.3 V	–	–	2	µA
VREG, VCP, AND BG THRESHOLDS						
VREG OV Thresholds	$VREG_{OV,H}$	V_{VREG} rising, LX1 PWM disabled	5.70	5.95	6.20	V
	$VREG_{OV,L}$	V_{VREG} falling, LX1 PWM enabled	–	5.85	–	V
VREG OV Hysteresis	$VREG_{OV, HYS}$	$V_{REGOV,H}$ – $V_{REGOV,L}$	–	100	–	mV
VREG UV Thresholds	$VREG_{UV,H}$	V_{VREG} rising, triggers rise of SS2	4.14	4.38	4.62	V
	$VREG_{UV,L}$	V_{VREG} falling	–	4.28	–	V
VREG UV Hysteresis	$VREG_{UV, HYS}$	$V_{REGUV,H}$ – $V_{REGUV,L}$	–	100	–	mV
VCP OV Thresholds	$VCP_{OV,H}$	V_{VCP} rising, latches all regulators off	11	12.5	14	V
VCP UV Thresholds	$VCP_{UV,H}$	V_{VCP} rising, PWM enabled	2.95	3.15	3.35	V
	$VCP_{UV,L}$	V_{VCP} falling, PWM disabled	–	2.8	–	V
VCP UV Hysteresis	$VCP_{UV,HYS}$	$V_{CPUV,H}$ – $V_{CPUV,L}$	–	350	–	mV
BG_{REF} and BG_{FAULT} UV Thresholds [2]	BGx_{UV}	BG_{VREF} or BG_{FAULT} rising	1.00	1.05	1.10	V
IGNITION STATUS (ENBATS) SPECIFICATIONS						
ENBATS Thresholds	$V_{ENBATS,H}$	V_{ENBATx} rising	2.9	3.3	3.5	V
	$V_{ENBATS,L}$	V_{ENBATx} falling	2.2	2.6	2.9	V
ENBATS Output Voltage	$VO_{ENBATS, LO}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATS Leakage Current [1]	I_{ENBATS}	V_{ENBATS} = 3.3 V	–	–	2	µA

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ELECTRICAL CHARACTERISTICS – PULSE WIDTH WINDOW WATCHDOG TIMER (PWWD) [1]:

Valid at 3.5 V < V_{IN} < 36 V, –40°C < T_A = T_J < 150°C, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD ENABLE\INPUT (WD_{ENn})						
WD_{ENn} Voltage Thresholds	$WD_{ENn,LO}$	V_{WDENn} falling, WDT enabled	0.8	–	–	V
	$WD_{ENn,HI}$	V_{WDENn} rising, WDT disabled	–	–	2	V
WD_{ENn} Input Resistance	$R_{WD,ENn}$		–	60	–	kΩ
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$WD_{IN,LO}$	$V_{WD,IN}$ falling, WD_{ADJ} pulled low by R_{ADJ}	0.8	–	–	V
	$WD_{IN,HI}$	$V_{WD,IN}$ rising, WD_{ADJ} charging	–	–	2	V
WD_{IN} Input Current [1]	$WD_{I,IN}$	$V_{WD,IN}$ = 5 V	−10	±1	10	µA
WD_{OUT} SPECIFICATIONS						
WD_{OUT} Output Voltage	$V_{WD,OUT,LO}$	$I_{WD,OUT}$ = 4 mA	–	–	400	mV
WD_{OUT} Leakage Current [1]	$I_{WD,OUT}$	$V_{WD,OUT}$ = 3.3 V	–	–	2	µA
WATCHDOG (WD) OSCILLATOR, PULSE WIDTH SELECTION, AND START DELAY						
WD Oscillator Tolerance	$WD_{OSC,TOL}$	Typical value is at 25°C [2]	−5	±2.5	+5	%
WD Startup Delay	$WD_{START,DLY}$	Gated by WD_{ENn} = 0 × NPOR↥	1.6	2	2.4	ms
WD_{IN} Pulse-Width Programming	$WD_{IN,PW}$	R_{ADJ} = 22.1 kΩ (WD_{OSC} = 1 MHz)	0.95	1	1.05	ms
		R_{ADJ} = 44.2 kΩ (WD_{OSC} = 500 kHz)	1.9	2	2.1	ms
WD First Edge Timeout Delay	$WD_{EDGE,TO}$	R_{ADJ} = 22.1 kΩ (WD_{OSC} = 1 MHz)	4.7	5	5.3	ms
		R_{ADJ} = 44.2 kΩ (WD_{OSC} = 500 kHz)	9.4	10	10.6	ms
WD CLK_{IN} Non-Activity Timeout	$WD_{ACT,TO}$	R_{ADJ} = 22.1 kΩ (WD_{OSC} = 1 MHz)	15.2	16	16.8	ms
		R_{ADJ} = 44.2 kΩ (WD_{OSC} = 500 kHz)	30.4	32	33.6	ms
WATCHDOG CLOCK INPUT ($WD_{CLK,IN}$)						
Input Clock Divider	$WD_{CLK,DIV}$		–	8	–	–
$WD_{CLK,IN}$ Voltage Thresholds	$WD_{CLK,IN,LO}$	$V_{WD,CLK,IN}$ falling	0.8	–	–	V
	$WD_{CLK,IN,HI}$	$V_{WD,CLK,IN}$ rising	–	–	2	V
WATCHDOG WINDOW TOLERANCE SELECTION ($WD_{WIN,TOL}$)						
WD Window Tolerance Settings	$WD_{WIN,TOL}$	WD_{TOL} pin connected to GND	−8	–	+8	%
		WD_{TOL} pin floating	−13	–	+13	%
		WD_{TOL} pin connected to VCC	−18	–	+18	%
WATCHDOG PULSE WIDTH (PW) ERROR COUNTING						
Counter Increment if PW Fault	WD_{INC}		–	+10	–	counts
Counter Decrement if PW is OK	WD_{DEC}		–	–2	–	counts
Counts to Latch WD_{FAULT} Low	WD_{COUNT}		–	160	–	counts

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FUNCTIONAL DESCRIPTION

Overview

The A4411 is a power management IC designed for automotive applications. It contains a pre-regulator plus four DC post-regulators to create the voltages necessary for typical automotive applications, such as electrical power steering and automatic transmission control.

The pre-regulator can be configured as a buck or buck-boost regulator. Buck-boost is required for applications that need to work at extremely low battery voltages. This pre-regulator generates a fixed 5.35 V and can deliver up to 1 A to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

The A4411 includes four internal post-regulators: three linear regulators and one adjustable output synchronous buck regulator.

Buck-Boost Pre-Regulator (VREG)

The pre-regulator incorporates an internal high-side buck switch and a boost switch gate driver. An external freewheeling Schottky diode and an LC filter are required to complete the buck converter. By adding a MOSFET and a Schottky diode, the boost configuration can maintain all outputs with input voltages as low as 3.5 V. Typical boost performance is shown in Figure 1. The A4411 includes a compensation pin (COMP1) and a soft-start pin (SS1) for the pre-regulator.

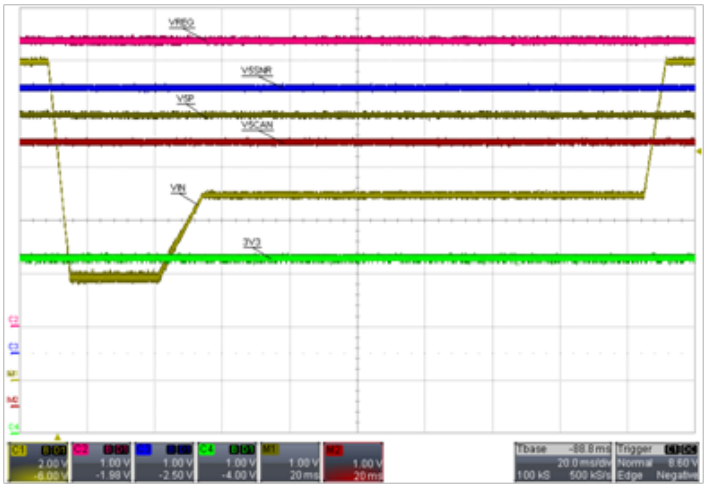

Figure 1: Buck-Boost Performance with Relatively Fast V_{VIN} Transition Times for a Representative Start/Stop Waveform

$V_{VIN(TYP)}$ = 12 V, $V_{VIN(MIN)}$ = 4 V, 20 ms/DIV

The pre-regulator provides protection and diagnostic functions.

1. Overvoltage protection
2. High voltage rating for load dump
3. Switch-node-to-ground short-circuit protection
4. Open freewheeling diode protection
5. Pulse-by-pulse current limit
6. Hiccup mode short-circuit protection (refer to Figure 2)

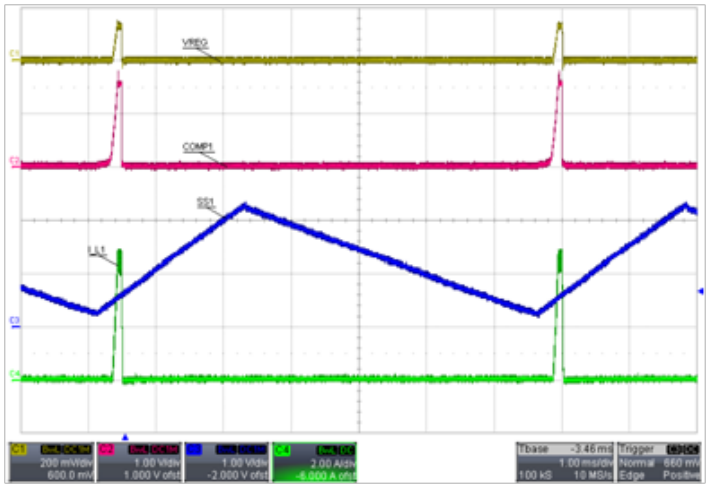

Figure 2: Pre-Regulator Hiccup Mode Operation when VREG is Shorted to GND and C_{SS1} = 22nF

CH1 = VREG, CH2 = COMP1, CH3 = SS1, CH4 = I_{L1}, 1 ms/DIV

For the pre-regulator, hiccup mode is enabled when PWM switching begins. If V_{VREG} is less than 1.3 V, the number of overcurrent pulses (OCP) is limited to only 30. If V_{VREG} is greater than 1.3 V, the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance.

Adjustable Synchronous Buck Regulator (ADJ)

The A4411 integrates the high-side and low-side MOSFETs necessary for implementing an adjustable output 750 mA_{DC} / 1 A_{PEAK} synchronous buck regulator. The synchronous buck is powered by the 5.35 V pre-regulators output. An external LC filter is required to complete the synchronous buck regulator. The synchronous buck output voltage is adjusted by a connecting a resistor divider from the buck output to the feedback pin (FB_{ADJ}). The A4411 includes a compensation pin (COMP2) and a soft-start pin (SS2) for the synchronous buck.

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Protection and safety functions provided by the synchronous buck are:

1. Undervoltage detection
2. Overvoltage detection
3. Switch-node-to-ground short-circuit protection
4. Pulse-by-pulse current limit
5. Hiccup mode short-circuit protection (shown in Figure 3)

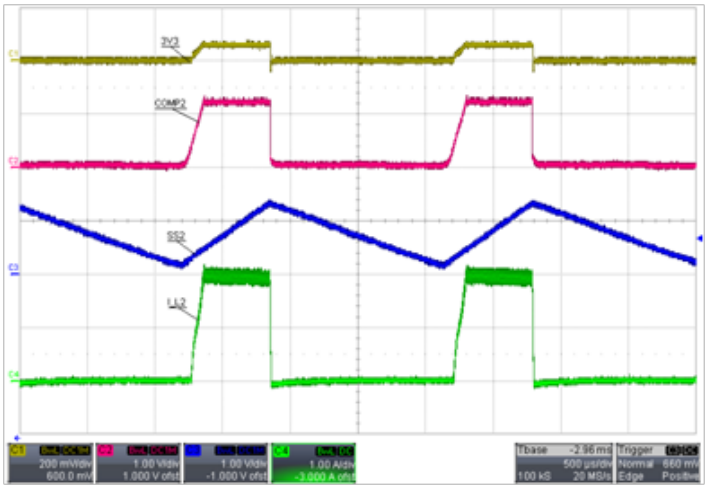

Figure 3: Synchronous Buck Hiccup Mode Operation when V_{OUT} is Shorted to GND and C_{SS2} = 22 nF

CH1=V_{OUT}, CH2=COMP1, CH3=SS1, CH4=IL1, 500 µs/DIV

For the synchronous buck, hiccup mode is enabled when V_{SS2} = $V_{HIC2,EN}$ (1.2 V_{TYP}). If $V_{FB,ADJ}$ is less than 300 mV_{TYP} the number of over current pulses (OCP) is limited to only 30. If $V_{FB,ADJ}$ is greater than 300 mV_{TYP} the number of OCP pulses is increased to 120 to accommodate the possibility of starting into a relatively high output capacitance.

Low-Dropout Linear Regulators (LDOs)

The A4411 has three low-dropout linear regulators (LDOs), one 5 V / 200 mA_{MAX} ($V5_{CAN}$), one 5 V / 150 mA_{MAX} ($V5_{SNR}$), and one high-voltage protected 5 V / 120 mA_{MAX} (V5P). The switching pre-regulator efficiently regulates the battery voltage to an intermediate value to power the LDOs. This pre-regulator topology reduces LDO power dissipation and junction temperature.

All linear regulators provide the following protection features:

1. Undervoltage and overvoltage detection
2. Current limit with foldback short-circuit protection (see Figure 4)

The protected 5 V regulator (V5P) includes protection against accidental short-circuit to the battery voltage. This makes this output most suitable for powering remote sensors or circuitry via a wiring harness where short-to-battery is possible.

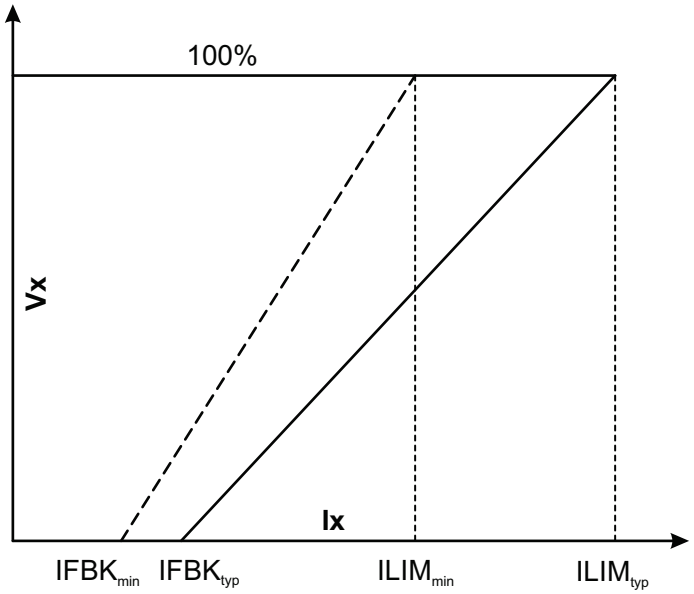

Figure 4: LDO Foldback Characteristics

Tracking Input (TRACK)

The V5P LDO is a tracking regulator. It can be set to use either V5 or $V_{FB,ADJ}$ as its reference by setting the TRACK input pin to a logic low or high. If the TRACK input is left unconnected an internal current source will set the TRACK pin to a logic high.

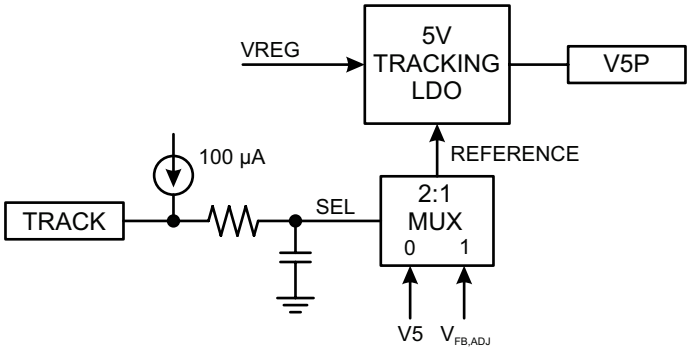

Figure 5: The V5P reference is set by the TRACK input.

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Pulse-Width Window Watchdog (PWWD)

The A4411 pulse-width window watchdog circuit monitors an external clock applied to the WD_{IN} pin. This clock should be generated by the primary microcontroller or DSP. The A4411 watchdog measures the time between two clock edges, either rising or falling. So the watchdog effectively measures both the "high" and "low" pulse widths, as shown in Figure 16.

If an incorrect pulse width is detected, the watchdog increments its fault counter by 10. If a correct pulse width is detected, the watchdog decrements its fault counter by 2. If the watchdog's fault counter exceeds 160, then the WD fault latch will be set and the WD_{OUT} pin will transition low. This fault condition is shown in Figure 16.

The watchdog and its fault latch will be reset if:

1. The WD_{ENn} pin is set high (i.e. WD is disabled), or
2. NPOR goes low (i.e. ENB and ENBAT are low), or
3. The internal rail, VCC, is low (i.e. V_{VIN} is removed), or
4. The bandgap, BG1, transitions low.

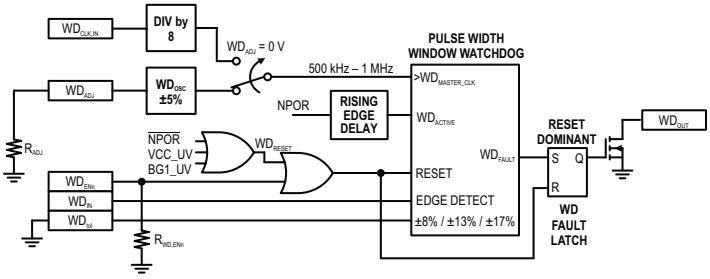

Figure 6: Pulse-Width Window Watchdog

The expected pulse width (PW) is programed by connecting a resistor (R_{ADJ}) from the WD_{ADJ} pin to ground. The relationship between R_{ADJ} and PW is:

$$R_{ADJ} = 22.1 \times PW$$

where PW is in ms and R_{ADJ} is the required external resistor value in kΩ. The typical range for PW is 1 to 2 ms.

The watchdog will be enabled if the following two conditions are satisfied:

1. The WD_{ENn} pin is a logic low, and
2. NPOR transitions high and remains high for at least $WD_{START,DLY}$ (2 ms_{TYP}). This requires all regulators to be above their undervoltage thresholds.

This startup delay allows the microcontroller or DSP to complete its initialization routines before delivering a clock to the WD_{IN} pin. The $WD_{START,DLY}$ time is shown in Figure 16.

After startup, if no clock edges are detected at WD_{IN} for at least $WD_{START,DLY}$ + $WD_{EDGE,TO}$, the A4411 will set the WD latch and WD_{OUT} will transition low. $WD_{EDGE,TO}$ varies with the value of R_{ADJ} as shown in the Electrical Characteristics table. The "edge timeout" condition is shown as (1) in Figure 17.

During normal operation, if clock activity is no longer detected at WD_{IN} for at least $WD_{ACT,TO}$, the A4411 will set the WD latch and WD_{OUT} will transition low. $WD_{ACT,TO}$ varies with the value of R_{ADJ} as shown in the Electrical Characteristics table. The "loss of clock activity" condition is shown as (2) in Figure 17.

The nominal WD_{IN} pulse width is set by the value of R_{ADJ}. However, the pulse widths generated by a microcontroller or DSP depend on many factors and will have some pulse-to-pulse variation. The A4411 accommodates pulse-width variations by allowing the designer to select a "window" of allowable variations. The size of the window is chosen based on the voltage at the WD_{TOL} pin, as shown in Table 1.

Table 1: WDTOL Pin Voltage Determines the WDIN Pulse Width Tolerance or "Window"

WD_{TOL} (V)	Allowed WD_{IN} Pulse-Width Tolerance
Low (0 V)	±8%
Float (Open)	±13%
High (VCC)	±18%

The watchdog performs its calculations based on an internally generated clock. The internal clock typically has an accuracy of ±2.5%, but may vary as much as ±5% due to IC process shifts and temperature variations. Variations in this clock result in a shift of the "OK Region" (i.e. the expected pulse width) at WD_{IN}, shown as a green area in Figure 18.

If the internal clock does not provide enough pulse-width measurement accuracy, the A4411 allows the designer to accept a high-precision clock at the $WD_{CLK,IN}$ pin. If the $WD_{CLK,IN}$ pin is used, then the WD_{ADJ} pin must be grounded. Figure 7 shows an example where a crystal and a tiny 6-pin driver (74LVC1GX04 by TI or NXP) are used to generate an external clock. The external clock should be in the 4 to 8 MHz frequency range for corresponding WD_{IN} pulse widths of 1 to 2 ms.

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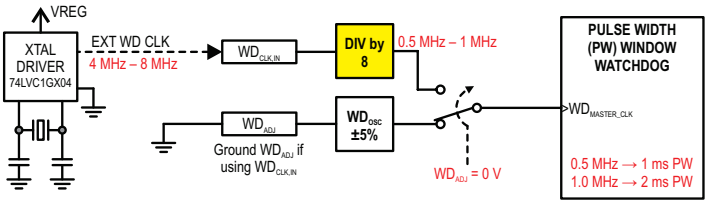

Figure 7: Applying an External Clock

Applying an external clock to the $WD_{CLK,IN}$ pin allows extremely accurate pulse-width measurements.

Dual Bandgaps (BG_{VREF}, BG_{FAULT})

Dual bandgaps, or references, are implemented within the A4411. One bandgap (BG_{VREF}) is dedicated solely to closed-loop control of the output voltages. The second bandgap (BG_{FAULT}) is employed for fault monitoring functions. Having redundant bandgaps improves reliability of the A4411.

If the reference bandgap is out of specification (BG_{VREF}), then the output voltages will be out of specification and the monitoring bandgap will report a fault condition by setting NPOR and/or POK5V low.

If the monitoring bandgap is out of specification (BG_{FAULT}), then the outputs will remain in regulation, but the monitoring circuits will report a fault condition by setting NPOR and/or POK5V low.

The reference and monitoring bandgap circuits include two smaller secondary bandgaps that are used to detect undervoltage of the main bandgaps during power-up.

Adjustable Frequency and Synchronization (FSET/SYNC)

The PWM switching frequency of the A4411 is adjustable from 250 kHz to 2.4 MHz. Connecting a resistor from the FSET/SYNC pin to ground sets the switching frequency. An FSET resistor with ±1% tolerance is recommended. The FSET resistor can be calculated using the following equation:

$$R_{FSET} = \left(\frac{f_{OSC}}{12724}\right)^{-1.175}$$

where R_{FSET} is in kΩ and f_{OSC} is the desired oscillator (PWM) frequency in kHz.

A graph of switching frequency versus FSET resistor values is shown in Figure 8.

The PWM frequency of the A4411 may be increased or decreased by applying a clock to the FSET/SYNC pin. The clock must satisfy the voltage thresholds and timing requirements shown in the Electrical Characteristics table.

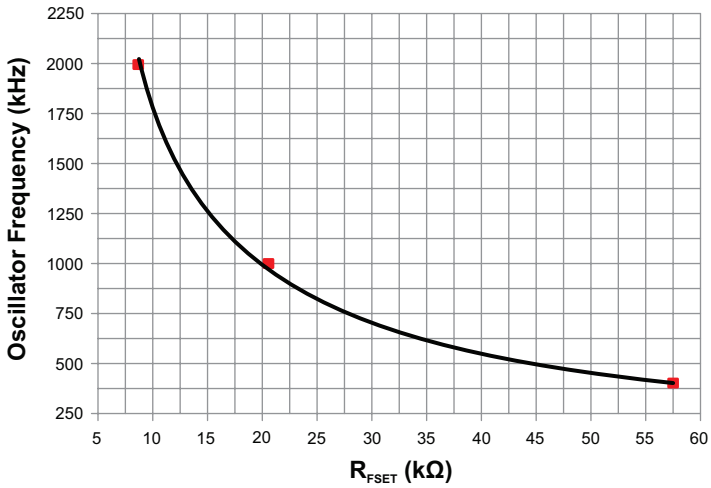

Figure 8: Switching Frequency vs. FSET Resistor Values

Frequency Dithering and LX1 Slew Rate Control

The A4411 includes two innovative techniques to help reduce EMI/EMC for demanding automotive applications.

First, the A4411 performs pseudo-random dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the base frequency set by R_{FSET}. A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at f_{OSC}, and at higher frequency multiples of f_{OSC}. Conversely, the A4411 spreads the spectrum around f_{OSC}, thus creating a lower magnitude at any comparable frequency. Frequency dithering is disabled if SYNC is used or V_{VIN} drops below approximately 8.3 V.

Second, the A4411 includes a pin to adjust the turn-on slew rate of the LX1 pin by simply changing the value of the resistor from the SLEW pin to ground. Slower rise times of LX1 reduce ringing and high-frequency harmonics of the regulator. The rise time may be adjusted to be quite long and will increase thermal dissipation of the pre-regulator if set too slow. Typical values of rise time versus R_{SLEW} are listed in Table 2.

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Table 2: Typical LX1 Rising Slew Rate vs. R_{SLEW}

R_{SLEW} (kΩ)	LX1 Rise Time (ns)
8.66	7
44.2	11
100	20

Enable Inputs (ENB, ENBAT)

Two enable pins are available on the A4411. A logic high on either of these pins enables the A4411. One enable (ENB) is logic level compatible for microcontroller or DSP control. The other input (ENBAT) must be connected to the high-voltage ignition (IGN) or accessory (ACC) switch through a relatively low-value series resistance, 2 to 3.6 kΩ. For transient suppression, it is strongly recommended that a 0.22 to 0.47 µF capacitor be placed after the series resistance to form a low-pass filter to the ENBAT pin as shown in the Applications Schematic.

Bias Supply (V_{CC})

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure reliable operation of the A4411. These features include:

1. Input voltage (V_{VIN}) undervoltage lockout
2. Undervoltage detection
3. Short-to-ground protection
4. Operation from either V_{VIN} or V_{VREG}, whichever is higher

Charge Pump (VCP, CP1, CP2)

A charge pump provides the voltage necessary to drive the high-side n-channel MOSFETs in the pre-regulator and the linear regulators.

Two external capacitors are required for charge pump operation. During the first half of the charge pump cycle, the flying capacitor between pins CP1 and CP2 is charged from either V_{VIN} or V_{VREG}, whichever is highest. During the second half of the charge pump cycle, the voltage on the flying capacitor charges the VCP capacitor. For most conditions, the V_{VCP} minus V_{VIN} voltage is regulated to approximately 6.5 V.

The charge pump can provide enough current to operate the pre-regulator and the LDOs at 2.2 MHz (full load) and 125°C ambient, provided V_{VIN} is greater than 6 V. Optional components D3, D4, and CP3 (refer to Figure 9) must be included if V_{VIN} drops below 6 V. Diode D3 should be a silicon diode rated for at least 200 mA/50 V with less than 50 µA of leakage current when V_R = 13 V and T_A = 125°C. Diode D4 should be a 1 A Schottky diode with a very low forward voltage (V_F) rated to withstand at least 30 V.

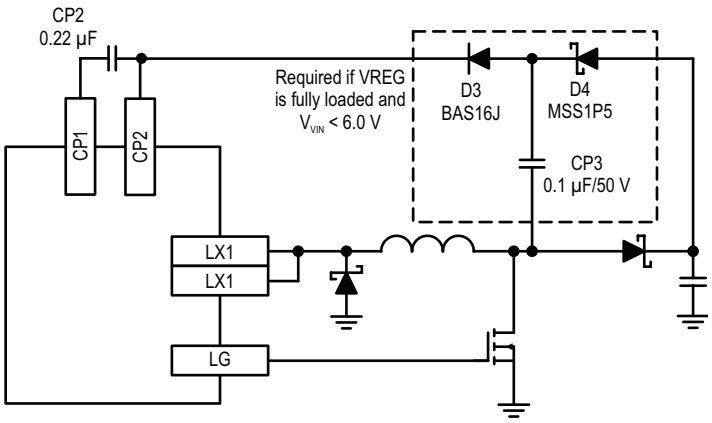

Figure 9: Charge pump enhancement components D3, D4, and CP3 are required if V_{VIN} < 6 V.

The charge pump incorporates some protection features:

1. Undervoltage lockout of PWM switching
2. Overvoltage "latched" shutdown of the A4411

Startup and Shutdown Sequences

The startup and shutdown sequences of the A4411 are fixed. If no faults exist and ENBAT or ENB transition high, the A4411 will perform its startup routine. If ENBAT and ENB are low for at least $EN_{td,FILT}$ + $td_{LDO, OFF}$ (typically 65 µs), the A4411 will enter a shutdown sequence. The startup and shutdown sequences are summarized in Table 3 and shown in a timing diagram in Figure 11.

Fault Reporting (NPOR, POK5V)

The A4411 includes two open-drain outputs for error reporting. The NPOR comparator monitors the feedback pin of the synchronous buck ($V_{FB,ADJ}$) for under- and overvoltage, as shown in Figure 10, Figure 11, and Figure 14. The POK5V comparators monitor the $V5_{CAN}$, $V5_{SNR}$, and V5P pins for under- and overvoltage, as shown in Figure 10, Figure 11, and Figure 15.

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The NPOR circuit includes a 2 ms delay after the synchronous buck output has risen above its undervoltage threshold. This delay allows the microcontroller or DSP plenty of time to power-up and complete its initialization routines. There is minimal NPOR delay if the synchronous buck output falls below its undervoltage threshold. The NPOR pin incorporates a 4 ms delay if the synchronous buck output exceeds its overvoltage threshold.

There are no significant delays on the POK5V output after $V5_{CAN}$, $V5_{SNR}$, and V5P have risen above or fallen below their undervoltage thresholds. Similar to the NPOR pin, the POK5V pin incorporates a 4 ms delay if any of the 5 V outputs exceed its overvoltage threshold.

The V5P monitor is unique: if V5P is accidently connected to the battery voltage, then POK5V will bypass the normal 4 ms overvoltage delay and set itself low immediately.

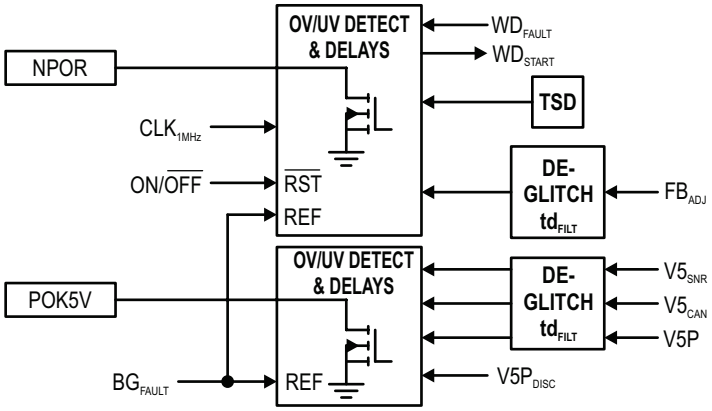

Figure 10: Fault Reporting Circuit

The fault modes and their effects on NPOR and POK5V are covered in detail in Table 4.

Table 3: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

A4411 Status Signals							Regulator Control Bits (0 = OFF, 1 = ON)			A4411 MODE
ON/$\overline{OFF}$	MPOR	VREG UV	SS1 LOW	ADJ UV	SS2 LOW	3×LDO UV	VREG ON	ADJ ON	LDOs ON	
X	1	1	1	1	1	1	0	0	0	RESET
0	0	1	1	1	1	1	0	0	0	OFF
1	0	1	1	1	1	1	1	0	0	STARTUP
1	0	0	0	1	1	1	1	1	0	↓
1	0	0	0	0	0	1	1	1	1	↓
1	0	0	0	0	0	0	1	1	1	RUN
0	0	0	0	0	0	0	1	1	1	DEGLITCH + DELAY
0	0	0	0	0	0	0	1	1	0	SHUTTING DOWN
0	0	0	0	0	X	1	1	0	0	↓
0	0	0	X	1	1	1	0	0	0	↓
0	0	1	1	1	1	1	0	0	0	OFF

X = DON'T CARE

ON/$\overline{OFF}$ = ENBAT + ENB

3×LDO UV = $V5_{SNR}$_UV + $V5_{CAN}$_UV + V5P_UV

MPOR = VIN_UV + VCC_UV + VCP_UV + BG1_UV + BG2_UV + TSD + VCP_OV (latched) + $D1_{MISSING}$ (latched) + $I_{LIM,LX1}$ (latched)

Table 4: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	A4411 RESPONSE TO FAULT	NPOR $V_{FB,ADJ}$	POK5V $V5_{SNR}$/ $V5_{CAN}$/V5P	LATCHED FAULT?	RESET METHOD
V5P short-to-VBAT	POK5V goes low when a V5P disconnect occurs. The other two 5 V LDOs remain active.	Not affected	Low if V5P disconnect occurs	NO	Check for short-circuits on V5P
Either $V5_{SNR}$, $V5_{CAN}$, or V5P are overvoltage (OV)	If OV condition persists for more than td_{OV} then set POK5V low. The other two 5 V LDOs must remain active.	Not affected	Low if $t > td_{OV}$	NO	Check for short-circuits on $V5_{SNR}$, $V5_{CAN}$, V5P
FB_{ADJ} overvoltage (OV)	If OV condition persists for more than td_{OV} then set NPOR low. All 5 V LDOs must remain active.	Low if $t > td_{OV}$	Not affected	NO	Check for short-circuits on FB_{ADJ}
Either $V5_{SNR}$, $V5_{CAN}$, or V5P are undervoltage (UV)	Closed-loop control will try to raise the LDOs voltage but may be constrained by the foldback current limit. Note: LDO(s) may be soft-starting.	Not affected	Low	NO	Decrease the load or wait for SS to finish
FB_{ADJ} undervoltage (UV)	Closed-loop control will try to raise the voltage but may be constrained by the pulse-by-pulse current limit. The ADJ regulator may need to enter hiccup mode. Also, the ADJ regulator may be simply soft-starting.	Low	Not affected	NO	Decrease the load or wait for SS to finish
Either $V5_{SNR}$, $V5_{CAN}$, or V5P are overcurrent (OC)	Foldback current limit will reduce the output voltage of the overloaded LDO. The other 5 V LDOs must operate normally.	Not affected	Low if any 5 V output voltage droops	NO	Decrease the load
FB_{ADJ} pin open circuit after soft-start is finished. Soft-start finished if SS1 and POK5V are high.	A small internal current sink pulls the voltage at the FB_{ADJ} pin high and mimics an ADJ regulator overvoltage condition.	Low because $V_{FB,ADJ} > V_{FB,ADJ,OV,H}$	Not affected	NO	Connect the FB_{ADJ} pin
FB_{ADJ} pin open circuit before soft-start is finished. Soft-start not finished if SS1 is high and POK5V is low.	A small internal current sink pulls the voltage at the FB_{ADJ} pin high and mimics an ADJ regulator overvoltage condition.	Low because $V_{FB,ADJ} > V_{FB,ADJ,OV,H}$	Low, Stuck in soft-start sequence	N/A Stuck in soft-start sequence	Connect the FB_{ADJ} pin
FB_{ADJ} regulator overcurrent (i.e. hard short-to-ground) $V_{SS2} < V_{HIC2,EN}$, $V_{FB,ADJ} < 300$ mV	Continue to PWM but turn off LX2 when the high-side MOSFET current exceeds I_{LIM2}.	Low	Not affected	NO	Remove the short-circuit
FB_{ADJ} regulator overcurrent (i.e. hard short-to-ground) $V_{SS2} > V_{HIC2,EN}$, $V_{FB,ADJ} < 300$ mV	Enters hiccup mode after 30 OCP faults.	Low	Not affected	NO	Decrease the load
FB_{ADJ} regulator overcurrent (i.e. soft short-to-ground) $V_{SS2} > V_{HIC2,EN}$, $V_{FB,ADJ} > 300$ mV	Enters hiccup mode after 120 OCP faults.	Low if $V_{FB,ADJ} < V_{FB,ADJ,UV,L}$	Not affected	NO	Decrease the load
VREG pin open circuit	V_{VREG} will decay to 0 V and LX1 will switch at max. duty cycle. The voltage on the VREG output capacitors will be very close to VIN/VBAT.	Low if ADJ output voltage droops	Low if any 5 V output voltage droops	NO	Connect the VREG pin
VREG overcurrent (i.e. hard short-to-ground) $V_{VREG} < 1.3$ V, $V_{COMP1} = EA1_{VO(MAX)}$	Enters hiccup mode after 30 OCP faults.	Low	Low	NO	Decrease the load
VREG overcurrent (i.e. soft short-to-ground) $V_{VREG} > 1.3$ V, $V_{COMP1} = EA1_{VO(MAX)}$	Enters hiccup mode after 120 OCP faults.	Low if ADJ output voltage droops	Low if any 5 V output voltage droops	NO	Decrease the load

Continued on next page...

Table 4: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4411 RESPONSE TO FAULT	NPOR $V_{FB,ADJ}$	POK5V $V5_{SNR}$/ $V5_{CAN}$/V5P	LATCHED FAULT?	RESET METHOD
VREG overvoltage (OV) V_{VREG} > $V_{REGOV,HI}$	Control loop will temporarily stop PWM switching of LX1. LX1 will resume switching when V_{VREG} returns to its normal range.	Low if ADJ output voltage droops	Low if any 5 V output voltage droops	NO	None
VREG asynchronous diode (D1) missing	Results in a Master Power-On Reset (MPOR) after 1 detection. All regulators are shut off.	Low if ADJ output voltage droops	Low if any 5 V output voltage droops	YES	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short-circuited or LX1 shorted to ground	Results in an MPOR after 1 detection of the high-side MOSFET current exceeding $I_{LIM,LX1}$, so all regulators are shut off.	Low if ADJ output voltage droops	Low if any 5 V output voltage droops	YES	Remove the short then cycle EN or VIN
LX2 shorted to ground	If LX2 is less than V_{VREG} – 1.2 V after the internal blanking time (~60 ns), the high-side FET will be shut off.	Low if ADJ output voltage droops	Not affected	NO	Remove the short
Slew pin open circuit (SLEW_OV)	Results in a “default” Slew Rate of 1.5 V/ns for LX1	Operates normally	Operates normally	NO	Place the slew rate resistor
Slew pin shorted to ground (SLEW_UV)	Results in a “default” Slew Rate of 1.5 V/ns for for LX1	Operates normally	Operates normally	NO	Place the slew rate resistor
FSET/SYNC pin open circuit (FSET/SYNC_OV)	Results in “default” PWM frequency of 1 MHz	Operates normally	Operates normally	NO	Connect the FSET/SYNC pin
FSET/SYNC pin shorted to ground (FSET/SYNC_UV)	Results in “default” PWM frequency of 1 MHz	Operates normally	Operates normally	NO	Remove the short-circuit
Charge pump (VCP) overvoltage (OV)	Results in an MPOR, so all regulators are off	Low	Low	YES	Check VCP/CP1/ CP2, then cycle EN or VIN
Charge pump (VCP) undervoltage (UV)	Results in an MPOR, so all regulators are off	Low	Low	NO	Check VCP/CP1/ CP2 components
CP1 or CP2 pin open circuit	Results in VCP_UV and an MPOR, so all regulators are off	Low	Low	NO	Connect CP1 or CP2 pins
CP1 pin shorted to ground	Results in VCP_UV and an MPOR, so all regulators are off	Low	Low	NO	Remove the short-circuit
CP2 pin shorted to ground	Results in high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR so all regulators are off.	Low	Low	N/A	Remove short-circuit, replace the A4411
BG_{VREF} or BG_{FAULT} undervoltage (UV)	Results in an MPOR, so all regulators are off	Low	Low	NO	Raise VIN or wait for BGs to power up
BG_{VREF} or BG_{FAULT} overvoltage (OV)	If BG_{VREF} is too high, all regulators will appear to be OV (because BG_{FAULT} is good). If BG_{FAULT} is too high, all regulators will appear to be UV (because BG_{VREF} is good)	Low	Low	N/A	Replace the A4411
VCC undervoltage or pin shorted to ground	Results in an MPOR, so all regulators are off	Low	Low	NO	Raise VIN or remove short at VCC pin
Thermal shutdown (TSD)	Results in an MPOR, so all regulators are off	Low	Low	NO	Let the A4411 cool down

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TIMING DIAGRAMS

(Not to Scale)

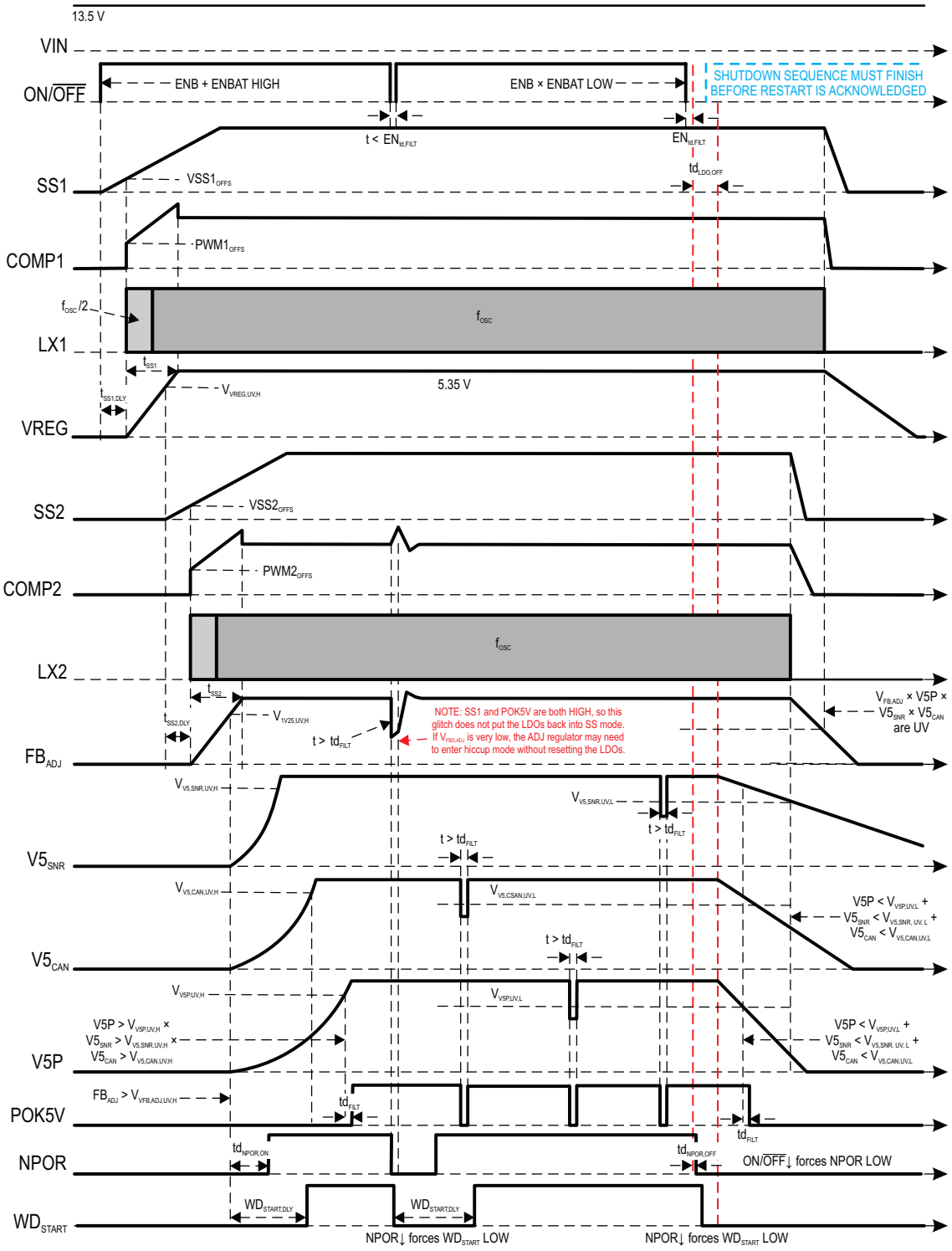

Figure 11: Startup and Shutdown by ENBAT or ENB (Also shows "glitch" reactions)

× is for "and", + is for "or"

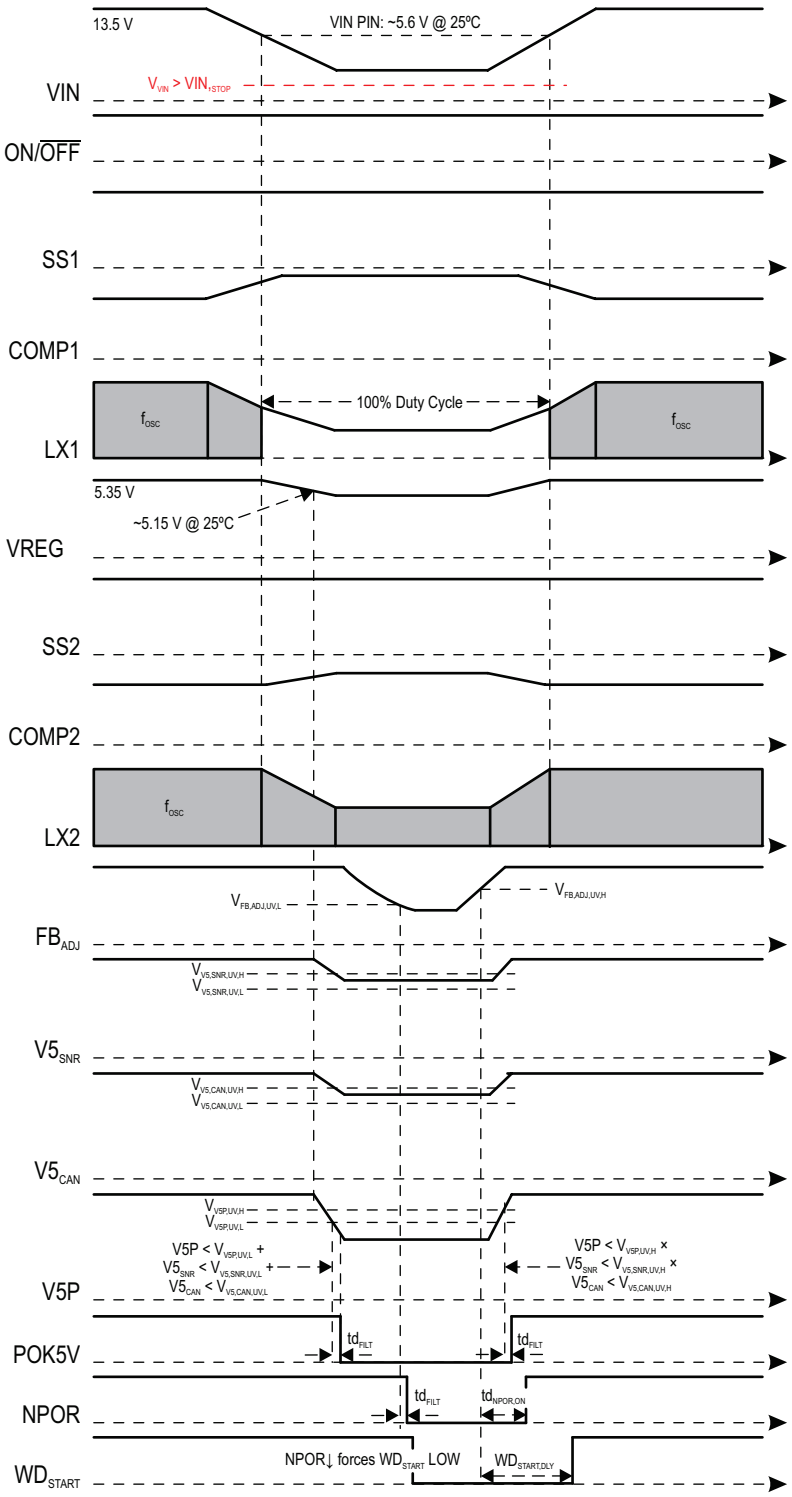

Figure 12: Input Voltage (VIN) Undervoltage, $V_{VIN} > VIN_{STOP}$

× is for "and", + is for "or"

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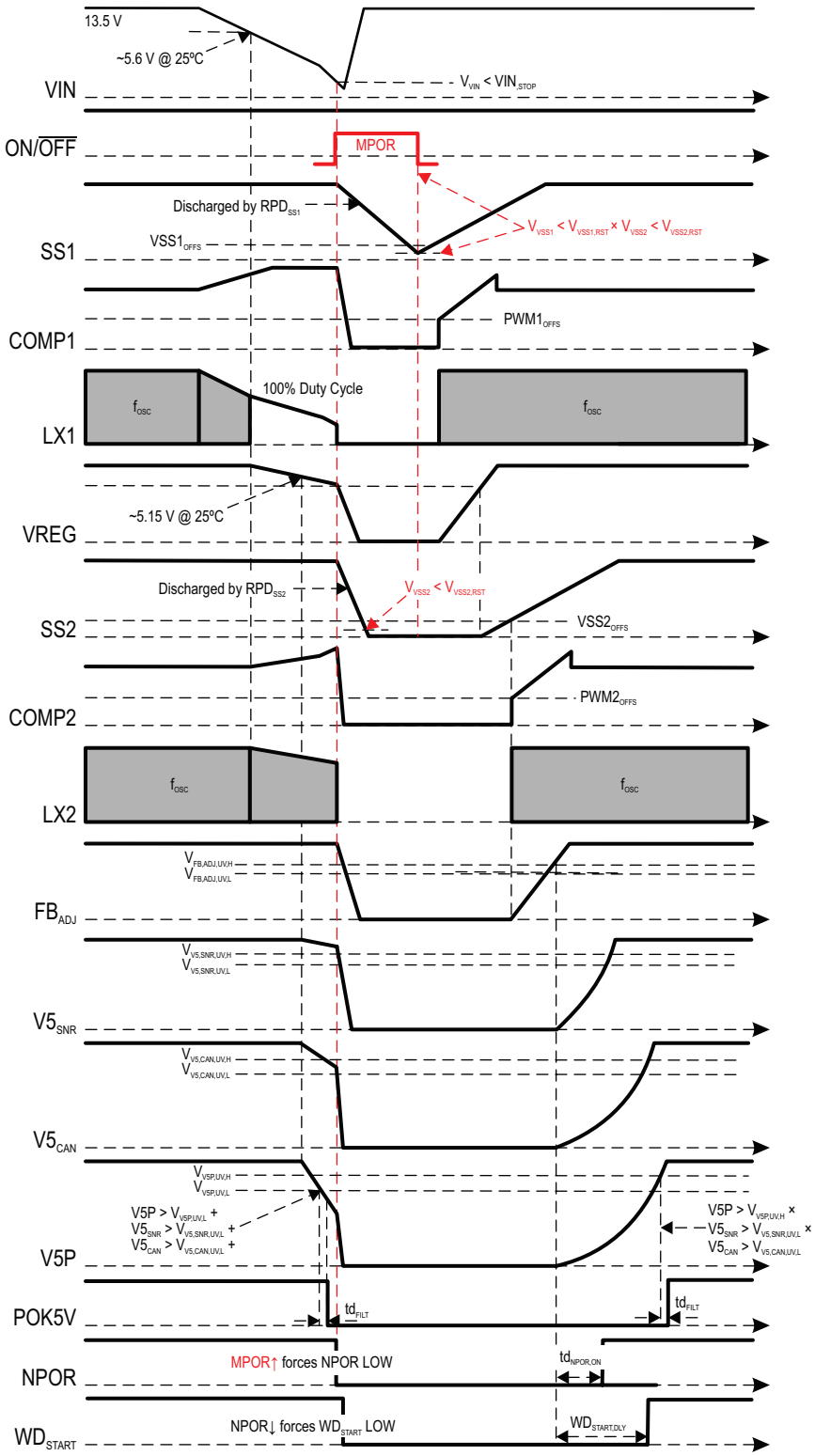

Figure 13: Input Voltage (VIN) Undervoltage, $V_{VIN} < VIN_{STOP}$

× is for "and", + is for "or"

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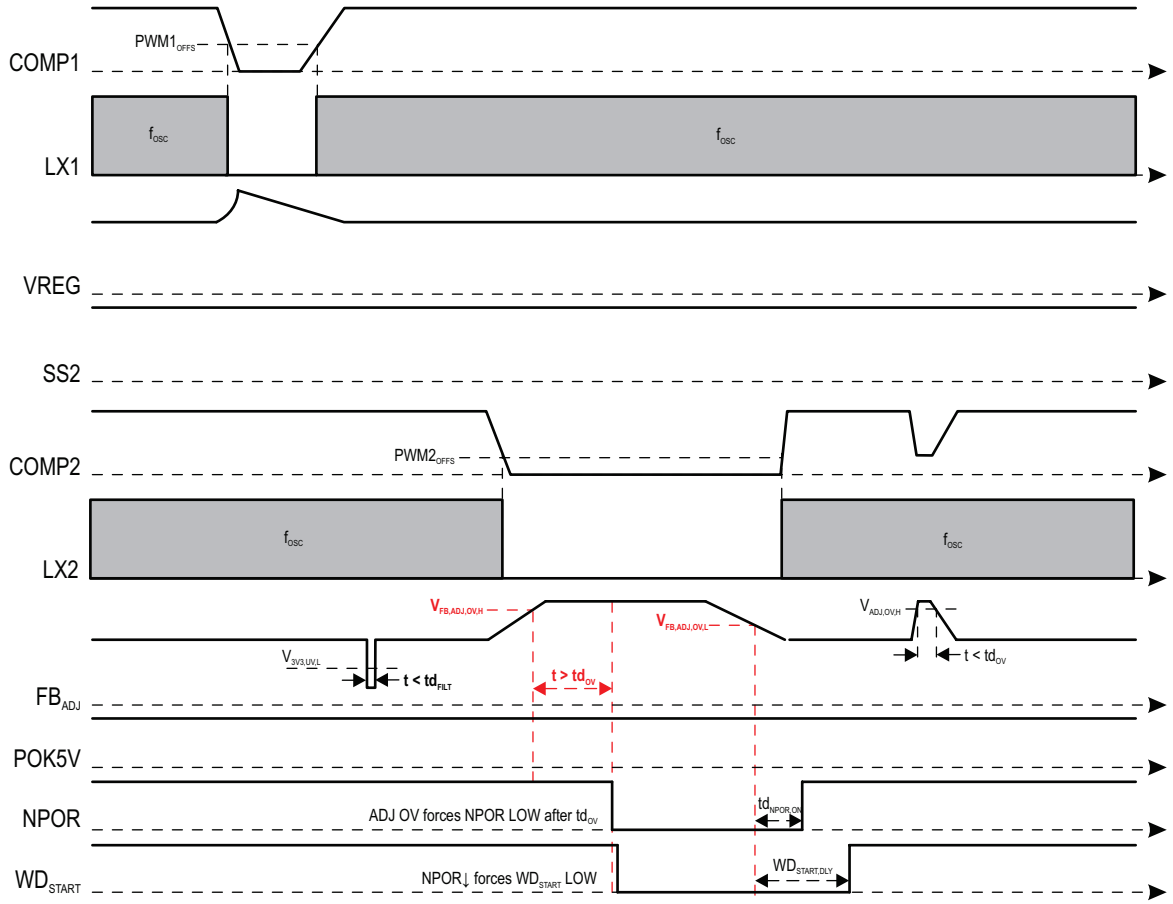

Figure 14: VREG and FB_{ADJ} Overvoltage Operation

× is for "and", + is for "or"

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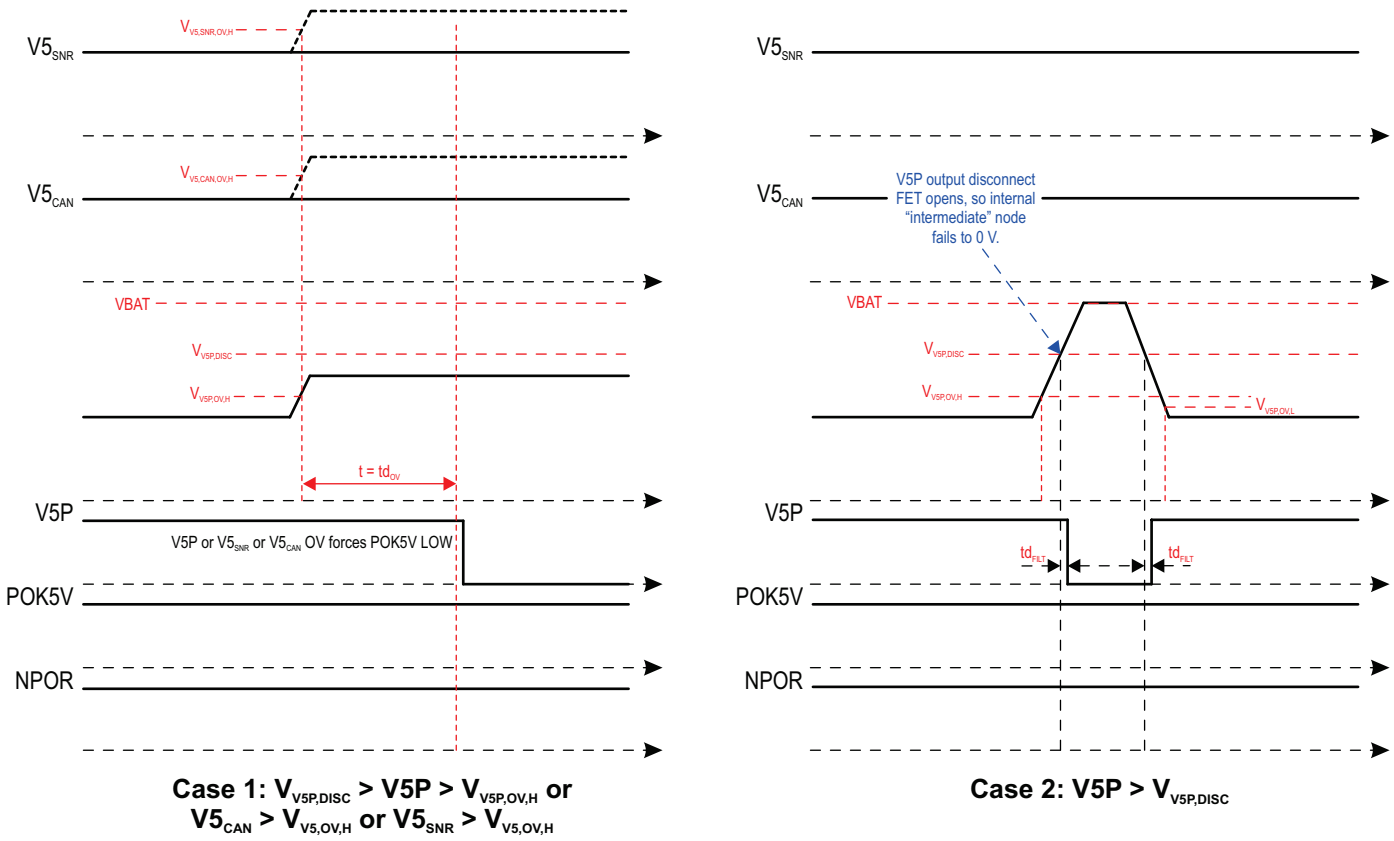

Case 1: $V_{V5P,DISC}$ > V5P > $V_{V5P,OV,H}$ or $V5_{CAN}$ > $V_{V5,OV,H}$ or $V5_{SNR}$ > $V_{V5,OV,H}$

Case 2: V5P > $V_{V5P,DISC}$

Figure 15: Overvoltage Cases for V5P, $V5_{SNR}$, and $V5_{CAN}$

× is for "and", + is for "or"

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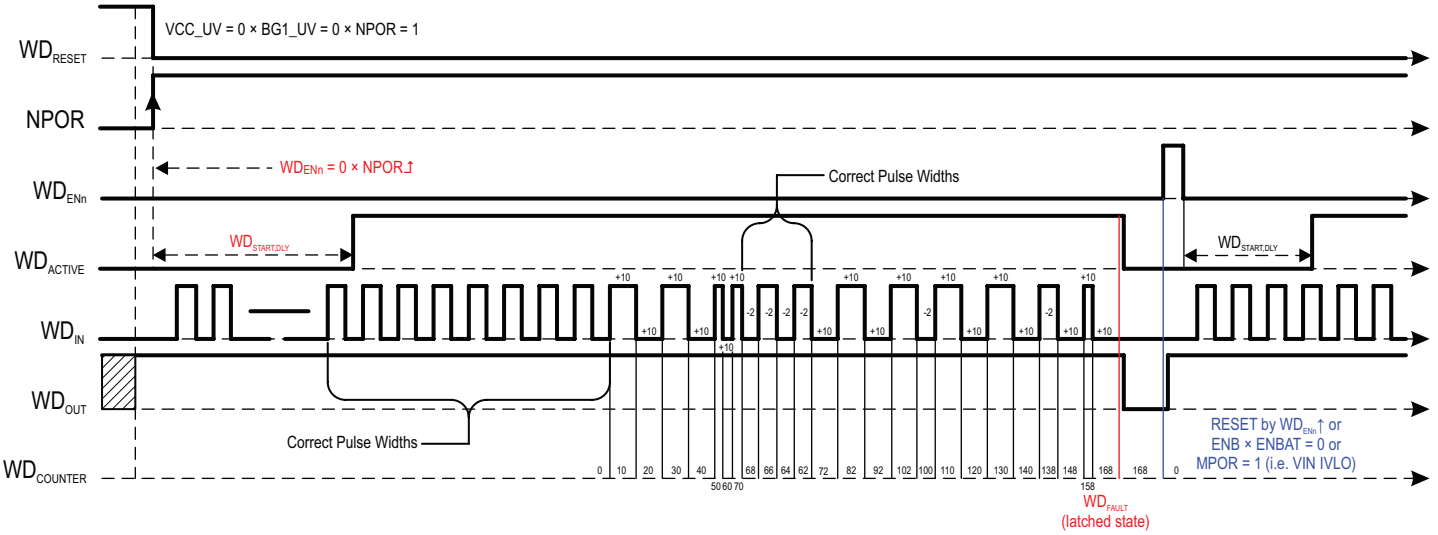

Figure 16: Watchdog (WD) Operation with Both Correct and Incorrect Pulse Widths

1. Incorrect pulse widths increment the WD counter by 10.
2. Correct pulse widths decrement the WD counter by 2.
3. A WD fault occurs if the total fault count exceeds 160.

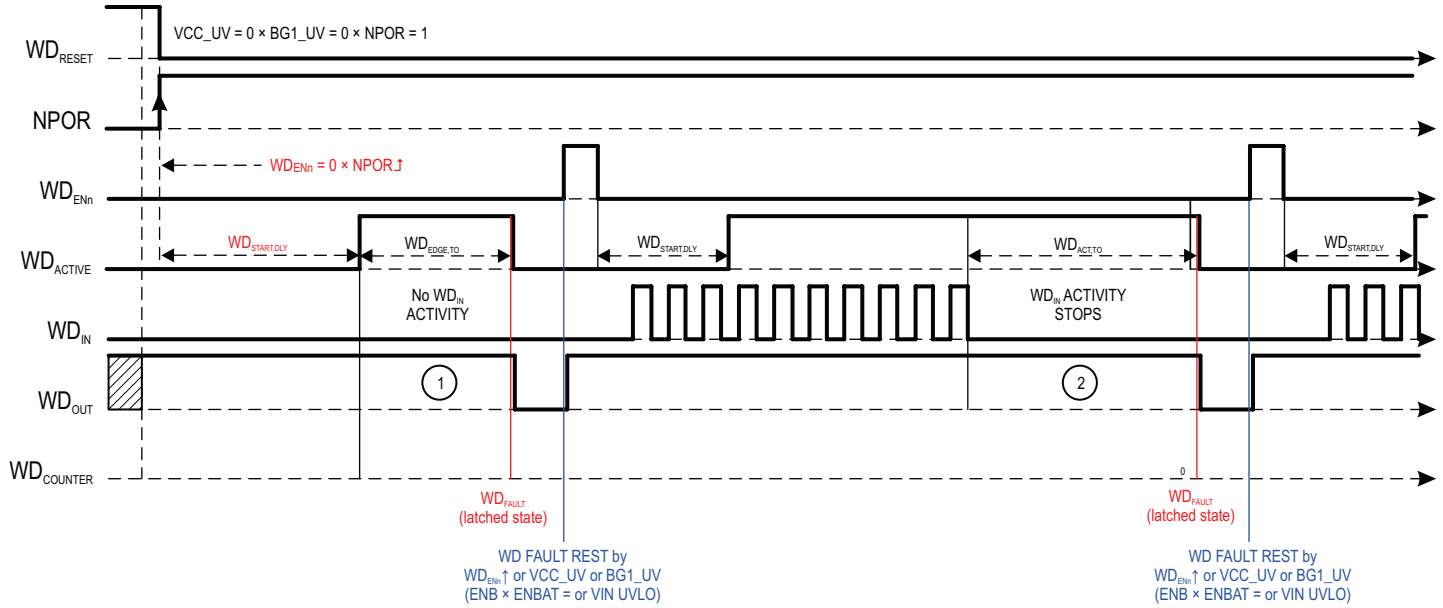

Figure 17: Watchdog Operation with Faults from:

1. No WD_{IN} Activity for $WD_{START,DLY}$ + $WD_{EDGE,TO}$
2. WD_{IN} Activity Stops

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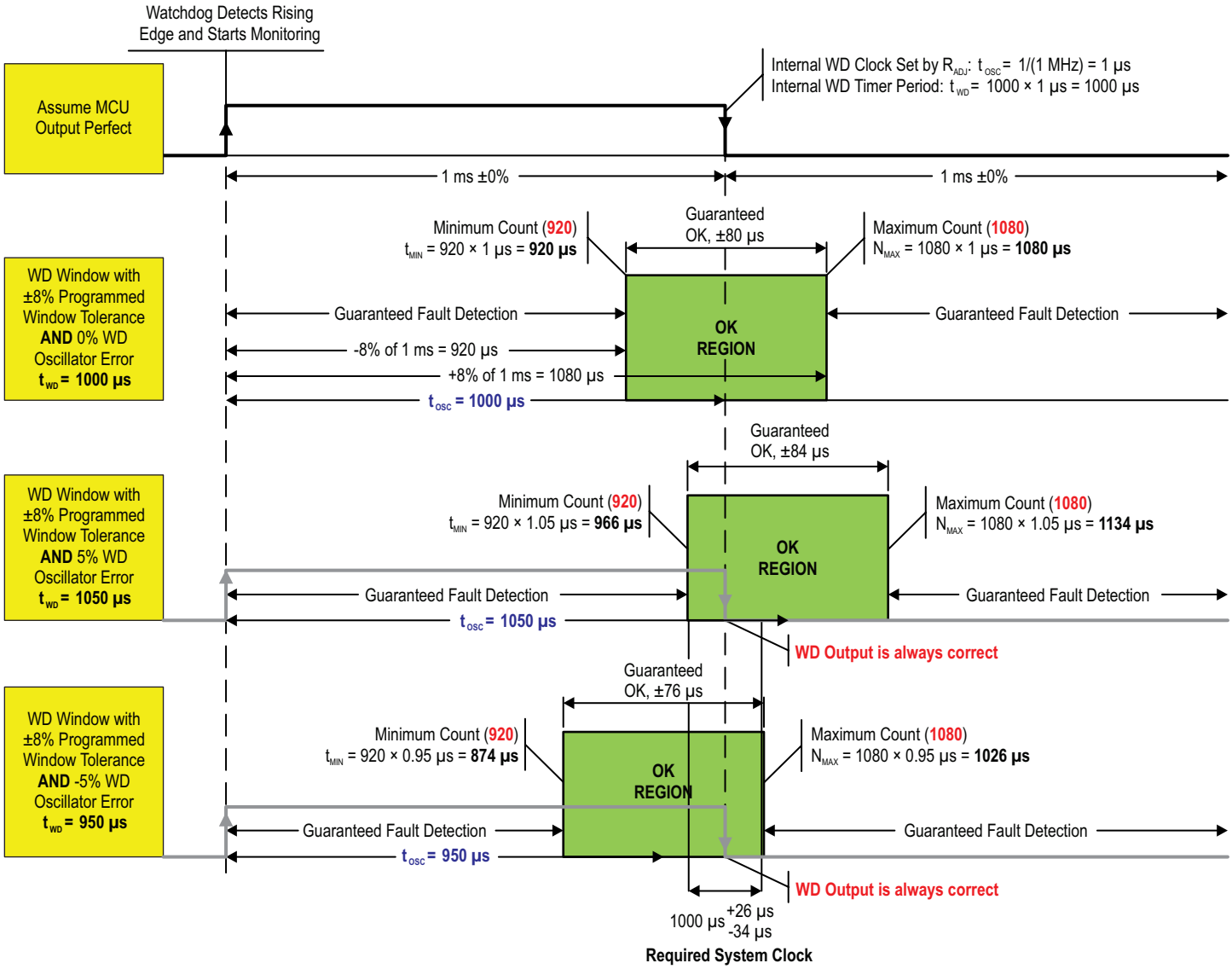

Figure 18: Watchdog Timer System Level Functionality (times are not to scale)

A4411 and System Operating Parameters:

1. 1 ms pulse widths coming from the microcontroller
2. ±8% WD Window Tolerance Selected (WDADJ = GND)
3. ±5% WD Oscillator Tolerance (worst case maximum)

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DESIGN AND COMPONENT SELECTION

PWM Switching Frequency (R_{FSET})

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A4411. If the system's required on-time is less than the A4411 minimum controllable on-time, then switch node jitter will occur and the output voltage will have increased ripple or oscillations.

The PWM switching frequency should be calculated using equation 1, where $t_{ON(MIN)}$ is the minimum controllable on-time of the A4411 (100 ns_{TYP}) and $V_{IN,MAX}$ is the maximum required operational input voltage (not the peak surge voltage).

$$f_{OSC} < \frac{5.35\ V}{t_{ON,MIN} \times V_{IN,MAX}} \quad (1)$$

If the A4411's synchronization function is used, then the base oscillator frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency according to equation 1.

Charge Pump Capacitors

The charge pump requires two capacitors: a 1 µF connected from pin VCP to VIN, and a 0.22 µF connected between pins CP1 and CP2. These capacitors should be high-quality ceramic capacitors, such as X5R or X7R, with voltage ratings of at least 16 V.

Pre-Regulator Output Inductor (L1)

For peak current mode control, it is well known that the system will become unstable when the duty cycle is above 50% without adequate Slope Compensation (S_E). However, the slope compensation in the A4411 is a fixed value based on the oscillator frequency (f_{OSC}). Therefore, it's important to calculate an inductor value so the falling slope of the inductor current (S_F) will work well with the A4411's fixed slope compensation.

Equation 2 can be used to calculate a range of values for the output inductor for the pre-regulator. In equation 2, slope compensation (S_{E1}) is a function of the switching frequency (f_{OSC}) according to equation 3, and V_F is the asynchronous diodes forward voltage.

$$\frac{(5.25\ V + V_F)}{S_{E1}} \le L1 \le \frac{(5.45\ V + V_F)}{\frac{S_{E1}}{2}} \quad (2)$$

$$S_{E1} = 0.00072 \times f_{OSC} + 0.0425 \quad (3)$$

When using equations 2 and 3, f_{OSC} is in kHz, S_{E1} is in A/µs, and L1 will be in µH.

If equation 2 yields an inductor value that is not a standard value, then the next highest standard value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The inductor should not saturate given the peak operating current according to equation 4. In equation 4, $V_{VIN,MAX}$ is the maximum continuous input voltage, such as 18 V, and V_F is the asynchronous diodes forward voltage.

$$I_{PEAK1} = 4.8\ A - \frac{S_{E1} \times (5.25\ V + V_F)}{1.1 \times f_{OSC} \times (V_{VIN,MAX} + V_F)} \quad (4)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum continuous input voltage and the highest expected ambient temperature.

The inductor ripple current can be calculated using equation 5.

$$\Delta I_{L1} = \frac{(V_{VIN} - 5.35\ V) \times 5.35\ V}{f_{OSC} \times L_1 \times V_{VIN}} \quad (5)$$

Pre-Regulator Output Capacitance

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

Within the first few PWM cycles, the deviation of V_{VREG} will depend mainly on the magnitude of the load step (ΔI_{LOAD1}), the value of the output inductor (L_1), the output capacitance (C_{OUT}), and the maximum duty cycle of the pre-regulator (D_{MAX1}). Equations 6 and 7 can be used to calculate a minimum output capacitance to maintain V_{VREG} within 0.5% of its target for a 750 mA load step at only 7 V_{IN}.

$$C_{OUT} \ge \frac{L1 \times (750\ mA)^2}{2 \times (7.0\ V - 5.25\ V) \times (0.005 \times 5.25\ V) \times D_{MAX1}} \quad (6)$$

$$D_{MAX} = \left(\frac{1}{f_{OSC}} - 80\ ns\right) \times f_{OSC} \quad (7)$$

After the load transient occurs, the output voltage will deviate

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from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z1}, C_{Z1}, C_{P1}) are discussed in more detail in the Pre-Regulator Compensation section of this datasheet.

The output voltage ripple (ΔV_{VREG}) is a function of the output capacitors parameters: C_{OUT}, ESR_{Co}, and ESL_{Co} according to equation 8.

$$\Delta V_{VREG} = \Delta I_L \times ESR_{Co} + \frac{V_{VIN} - V_{VREG}}{L_O} \times ESL_{Co} + \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (8)$$

The type of output capacitors will determine which terms of equation 8 are dominant. For the A4411 and automotive environments, only ceramic capacitors are recommended. The ESR_{CO} and ESL_{CO} of ceramic capacitors are virtually zero, so the peak-to-peak output voltage ripple of V_{VREG} will be dominated by the third term of equation 8.

$$\Delta V_{VREG,PP} = \frac{\Delta I_L}{8 \times f_{OSC} \times C_{OUT}} \quad (9)$$

Pre-Regulator Ceramic Input Capacitance

The ceramic input capacitors must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 10 can be used to calculate the minimum input capacitance,

$$C_{IN} \geq \frac{I_{VREG,MAX} \times 0.25}{0.90 \times f_{OSC} \times 50\,mV_{PP}} \quad (10)$$

where $I_{VREG,MAX}$ is the maximum current from the pre-regulator,

$$I_{VREG,MAX} = I_{V5,CAN} + I_{V5,SNR} + I_{V5P} + \frac{V_{OUT,ADJ} \times I_{OUT,ADJ}}{5.25\,V \times 80\%} + 20\,mA \quad (11)$$

A good design should consider the DC bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the capacitance value decreases. The X5R- and X7R-type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e. 1206/16 V or 1210/50 V).

Also, for improved EMI/EMC performance, it is recommended that two small capacitors be placed as close as physically possible to the VIN pins to address frequencies above 10 MHz. For example, a 0.1 µF/X7R/0603 and a 220 pF/COG/0402 capacitor will address frequencies up to 20 MHz and 200 MHz, respectively.

Pre-Regulator Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the A4411. Equation 4 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{VIN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

$$I_{AVG} = (1 - D_{BUCK}) \times I_{VREG,MAX} = 0.9 \times I_{VREG,MAX} \quad (12)$$

where $I_{VREG,MAX}$ is calculated using equation 11.

Pre-Regulator Boost MOSFET (Q1)

The maximum RMS current in the boost MOSFET (Q1) occurs when V_{VIN} is very low and the boost operates at its maximum duty cycle,

$$I_{Q1,RMS} = \sqrt{D_{MAX,BST} \times \left[\left(I_{PEAK1} - \frac{\Delta I_{L1}}{2}\right)^2 + \frac{\Delta I_{L1}}{12}\right]} \quad (13)$$

where I_{PEAK1} and ΔI_{L1} are derived using equations 4 and 5, respectively, and $D_{MAX,BST}$ is identified in the Electrical Characteristics table.

The boost MOSFET should have a total gate charge of less than 14 nC at a V_{GS} of 5 V. The V_{DS} rating of the boost MOSFET should be at least 20 V. Several recommended part numbers are shown in the Functional Block Diagram / Typical Schematic.

Pre-Regulator Boost Diode (D2)

The maximum average current in this diode is simply the output current, calculated with equation 11. However, in buck-boost mode, the peak currents in this diode may increase significantly. The A4411 will limit the current to the value calculated by equation 4.

Pre-Regulator Soft-Start and Hiccup Timing (C_{SS1})

The soft-start time of the pre-regulator is determined by the value of the capacitance at the soft-start pin (C_{SS1}).

If the A4411 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors ($I_{C,OUT} = C_{OUT} \times V_{OUT} / t_{SS}$) is higher than the pulse-by-pulse current threshold, as shown in Figure 19.

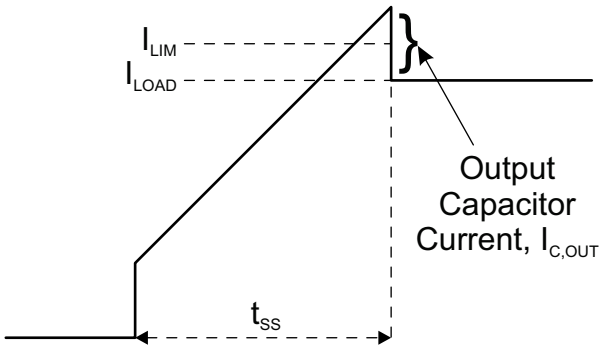

Figure 19: Output Current (I_{CO}) During Startup

To avoid prematurely triggering hiccup mode, the soft-start time (t_{SS1}) should be calculated using equation 14,

$$t_{SS1} = 5.35\ V \times \frac{C_{OUT}}{I_{C,OUT}} \quad (14)$$

where C_{OUT} is the output capacitance, and $I_{C,OUT}$ is the amount of current allowed to charge the output capacitance during soft-start (recommend 0.1 A < $I_{C,OUT}$ < 0.3 A). Higher values of $I_{C,OOUT}$ result in faster soft-start time, and lower values of $I_{C,OUT}$ ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an $I_{C,OUT}$ of 0.1 A and increasing it only if the soft-start time is too slow.

Then, C_{SS1} can be calculated based on equation 15:

$$C_{SS1} \geq \frac{I_{SS1,SU} \times t_{SS1}}{0.8\ V} \quad (15)$$

If a non-standard capacitor value for C_{SS1} is calculated, the next higher value should be used.

The voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ($I_{SS1,SU}$). However, PWM switching will not begin immediately because the voltage at the soft-start pin must rise above the soft-start offset voltage ($V_{SS1,OFFS}$). The soft-start delay ($t_{SS1,DELAY}$) can be calculated using equation 16.

$$t_{SS1,DELAY} = C_{SS1} \times \frac{V_{SS1.OFFS}}{I_{SS1,SU}} \quad (16)$$

When the A4411 is in hiccup mode, the soft-start capacitor sets the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with $I_{SS1,SU}$ and discharges the same capacitor with $I_{SS1,HIC}$ between startup attempts.

Pre-Regulator Compensation (R_{Z1}, C_{Z1}, C_{P1})

Although the A4411 can operate in buck-boost mode at low input voltages, it still can be considered a buck converter when examining the control loop. The following equations can be used to calculate the compensation components.

First, select the target crossover frequency for the final system. While switching at over 2 MHz, the crossover is governed by the required phase margin. Since a type II compensation scheme is used, the system is limited to the amount of phase that can be added. Hence, a crossover frequency (f_{C1}) in the region of 40 kHz is selected. The total system phase will drop off at higher crossover frequencies. The R_{Z1} calculation is based on the gain required to set the crossover frequency and can be calculated by equation 17.

$$R_{Z1} = \frac{13.38 \times \pi \times f_{C1} \times C_{OUT}}{gm_{POWER1} \times gm_{EA1}} \quad (17)$$

The series capacitor (C_{Z1}) along with the resistor (R_{Z1}) set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency and should be kept to minimum value. Equation 18 can be used to estimate this capacitor value.

$$C_{Z1} > \frac{4}{2\pi \times R_{Z1} \times f_{C1}} \quad (18)$$

Allegro recommends adding a small capacitor (C_{P1}) in parallel with the series combination of R_{Z1}/C_{Z1} to roll off the error amps gain at high frequency. This capacitor usually helps reduce LX1 pulse-width jitter, but if too large, it will also decrease the loop's phase margin.

Allegro recommends using this capacitor to set a pole at approximately 8× the loop's crossover frequency (f_{C1}), as shown in equation 19. If a non-standard capacitor value results, the next higher available value should be used.

$$C_{P1} \approx \frac{1}{2\pi \times R_{Z1} \times 8 \times f_{C1}} \quad (19)$$

Finally, look at the combined bode plot of both the power stage and the compensated error amp—the red curves shown in Figure 20. Careful examination of this plot shows that the magnitude and phase of the entire system are simply the sum of the error amp response (blue) and the power stage response (green). As shown in Figure 20, the bandwidth of this system (f_{C1}) is 43 kHz, the phase margin is 67 degrees, and the gain margin is 23 dB.

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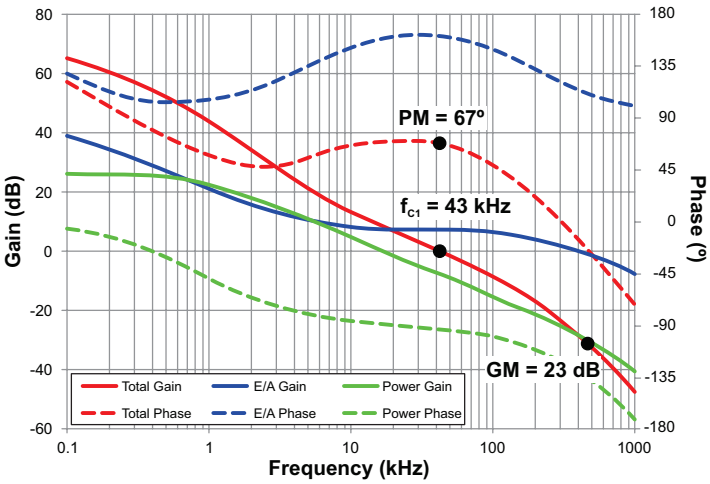

Figure 20: Bode Plot for the Pre-Regulator

R_{Z1} = 22.1 kΩ, C_{Z1} = 1.5 nF, C_{P1} = 15 pF
Lo = 4.7 µH, Co = 5 × 10 µF/16 V/1206

Synchronous Buck Component Selection

Similar design methods can be used for the synchronous buck; however, the complexity of variable input voltage and boost operation are removed.

Setting the Output Voltage (R_{FB1} and R_{FB2})

The A4411 allows the user to program the output voltage of the synchronous buck from 0.8 to 3.3 V. This is achieved by adding a resistor divider from its output to ground and connecting the center point to the FB_{ADJ} pin; see Figure 21 below.

The ratio of the feedback resistors can be calculated based on equation 20.

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT,ADJ}}{800\ mV} - 1\right) \qquad (20)$$

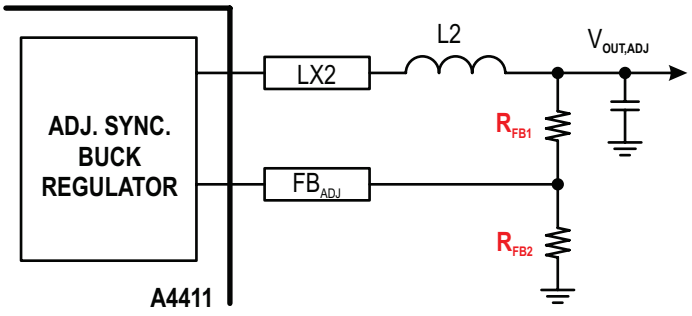

Figure 21: Setting the Synchronous Buck Output

Synchronous Buck Output Inductor (L2)

Equation 21 can be used to calculate a range of values for the output inductor for the synchronous buck regulator. Slope compensation (S_{E2}) can be calculated using equation 22.

$$\frac{V_{OUT,ADJ}}{2 \times S_{E2}} \le L2 \le \frac{V_{OUT,ADJ}}{S_{E2}} \qquad (21)$$

$$S_{E2} = 0.0003 \times f_{OSC} + 0.0175 \qquad (22)$$

When working with equations 21 and 22, f_{OSC} is in kHz, S_{E2} is in A/µs, and L2 will be in µH.

If equation 21 yields an inductor value that is not a standard value, then the next closest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% for inductor saturation.

The inductor should not saturate given the peak current at overload according to equation 23.

$$I_{PEAK2} = 2.4\ A - \frac{S_{E2} \times V_{OUT,ADJ}}{1.1 \times f_{OSC} \times 5.45\ V} \qquad (23)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Once the inductor value is known, the ripple current can be calculated using equation 24.

$$\Delta I_{L2} = \frac{(5.35\ V \times V_{OUT,ADJ}) \times V_{OUT,ADJ}}{f_{OSC} \times L2 \times 5.35\ V} \qquad (24)$$

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Synchronous Buck Output Capacitance

Within the first few PWM cycles, the deviation of $V_{OUT,ADJ}$ will depend mainly on the magnitude of the load step (ΔI_{LOAD2}), the value of the output inductor (L2), the output capacitance ($C_{OUT,ADJ}$), and the maximum duty cycle of the synchronous converter (D_{MAX2}). Equations 25 and 26 can be used to calculate a minimum output capacitance to maintain $V_{OUT,ADJ}$ within 0.5% of its target for a 400 mA load step.

$$C_{OUT,ADJ} \geq \frac{L2 \times (400\ mA)^2}{2 \times (5.25\ V - V_{OUT,ADJ}) \times (0.005 \times V_{OUT,ADJ}) \times D_{MAX2}} \quad (25)$$

$$D_{MAX2} = \left(\frac{1}{f_{OSC}} - 110\ ns\right) \times f_{OSC} \quad (26)$$

After the load transient occurs, the output voltage will deviate from its nominal value until the error amplifier can bring the output voltage back to its nominal value. The speed at which the error amplifier will bring the output voltage back to its setpoint will depend mainly on the closed-loop bandwidth of the system. Selection of the compensation components (R_{Z2}, C_{Z2}, C_{P2}) are discussed in more detail in the Synchronous Buck Compensation section of this datasheet.

Allegro recommends the use of ceramic capacitors for the synchronoous buck. The peak-to-peak voltage ripple of the synchronous buck ($\Delta V_{OUT,ADJ,PP}$) can be calculated with equation 27.

$$\Delta V_{VOUT,ADJ,PP} = \frac{\Delta I_{L2}}{8 \times f_{OSC} \times C_{OUT,ADJ}} \quad (27)$$

Synchronous Buck Compensation (R_{Z2}, C_{Z2}, C_{P2})

Again, similar techniques as used with the pre-regulator can be used to compensate the synchronous buck.

For the synchronous buck, select 55 kHz for the crossover frequency (f_{C2}) of the synchronous buck. Then, equation 28 can be used to calculate R_{Z2}.

$$R_{Z2} = \frac{V_{OUT,ADJ} \times 2\pi \times f_{C2} \times C_{OUT,ADJ}}{800\ mV \times gm_{POWER2} \times gm_{EA2}} \quad (28)$$

The series capacitor (C_{Z2}) along with the resistor (R_{Z2}) set the location of the compensation zero. This zero should be placed no lower than ¼ of the crossover frequency and should be kept to minimum value. Equation 29 can be used to estimate this capacitor value.

$$C_{Z2} > \frac{4}{2\pi \times R_{Z2} \times f_{C2}} \quad (29)$$

Allegro recommends adding a small capacitor (C_{P2}) in parallel with the series combination of R_{Z2}/C_{Z2} to roll off the error amp gain at high frequency. This capacitor usually helps reduce LX2 pulse-width jitter, but if too large, it will also decrease the loop's phase margin.

Allegro recommends using this capacitor to set a pole at approximately 8× the loop's crossover frequency (f_{C2}), as shown in equation 30. If a non-standard capacitor value results, use the next higher available value.

$$C_{P2} \approx \frac{1}{2\pi \times R_{Z2} \times 8 \times f_{C2}} \quad (30)$$

Finally, look at the combined bode plot of both the power stage and the compensated error amp—the red curves shown in Figure 22. The bandwidth of this system (f_{C2}) is 56 kHz, the phase margin is 70°, and the gain margin is 28 dB.

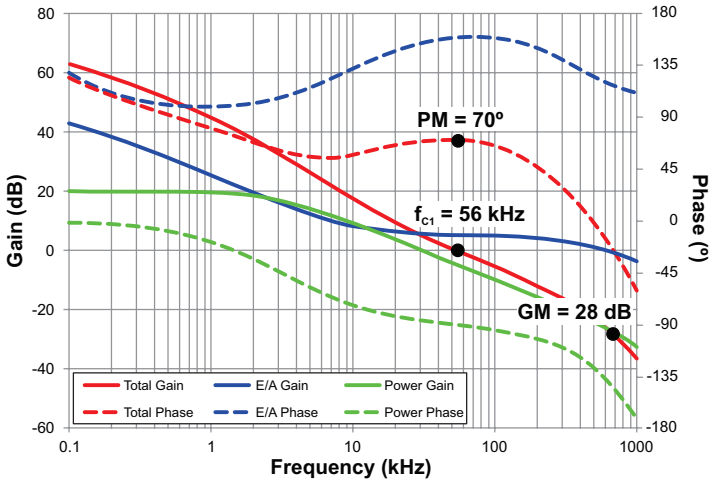

Figure 22: Bode Plot for the Sync. Buck at 3.3 V_{OUT}

R_{Z2} = 10 kΩ, C_{Z2} = 1.5 nF, C_{P2} = 15 pF
L2 = 4.7 µH, $C_{OUT,ADJ}$ = 2 × 10 µF/16 V/1206

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Synchronous Buck Soft-Start and Hiccup Timing

The soft-start time of the synchronous buck is determined by the value of the capacitance at the soft-start pin (C_{SS2}).

If the A4411 is starting into a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. To avoid prematurely triggering hiccup mode, the soft-start time (t_{SS2}) should be calculated according to equation 31,

$$t_{SS2} = V_{OUT,ADJ} \times \frac{C_{OUT,ADJ}}{I_{C,OUT}} \quad (31)$$

where $V_{OUT,ADJ}$ is the output voltage, $C_{OUT,ADJ}$ is the output capacitance, $I_{C,OUT}$ is the amount of current allowed to charge the output capacitance during soft-start (recommend 75 mA < $I_{C,OUT}$ < 150 mA). Higher values of $I_{C,OUT}$ result in faster soft-start times and lower values of $I_{C,OUT}$ ensure that hiccup mode is not falsely triggered. For the synchronous buck, Allegro recommends starting the design with an $I_{C,OUT}$ of 100 mA and increasing it only if the soft-start time is too slow.

Then, CSS2 can be selected based on equation 32,

$$C_{SS2} > \frac{I_{SS2,SU} \times t_{SS2}}{800\ mV} \quad (32)$$

If a non-standard capacitor value for C_{SS2} is calculated, the next larger value should be used.

The voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ($I_{SS2,SU}$). However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above the soft-start offset voltage ($V_{SS2,OFFS}$). The soft-start delay ($t_{SS2,DELAY}$) can be calculated using equation 33,

$$t_{SS2,DELAY} = C_{SS2} > \left(\frac{V_{SS2,OFFS}}{I_{SS2,SU}}\right) \quad (33)$$

When the A4411 is in hiccup mode, the soft-start capacitor sets the hiccup period. During a startup attempt, the soft-start pin charges the soft-start capacitor with $I_{SS2,SU}$ and discharges the same capacitor with $I_{SS1,HIC}$ between startup attempts.

Linear Regulators

The three linear regulators only require a single ceramic capacitor located near the A4411 to ensure stable operation. The range of acceptable values is shown in the Electrical Characteristics table. A 2.2 µF capacitor per regulator is a good starting point.

As the LDO outputs are routed throughout the PCB, it is recommended that a 0.1 µF/0603 ceramic capacitor be placed as close as possible to each load point for local filtering and high-frequency noise reduction.

Also, since the V5P output may be used to power remote circuitry, its load may include external wiring. The inductance of this wiring will cause LC-type ringing and negative spikes at the V5P pin if a “fast” short-to-ground occurs. It is recommended that a small Schottky diode be placed close to the V5P pin to limit the negative voltages, as shown in the Applications Schematic. The MSS1P5 (or equivalent) is a good choice.

Internal Bias (V_{CC})

The internal bias voltage should be decoupled at the VCC pin using a 1 µF ceramic capacitor. It is not recommended to use this pin as a source.

Signal Pins (NPOR, POK5V, WD_{OUT}, ENBATS)

The A4411 has many signal-level pins. The NPOR, POK5V, $WD_{OUT,}$ and ENBATS are open-drain outputs and require external pull-up resistors. Allegro recommends sizing the external pull-up resistors so each pin will sink less than 2 mA when it is a logic low.

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PCB LAYOUT RECOMMENDATIONS

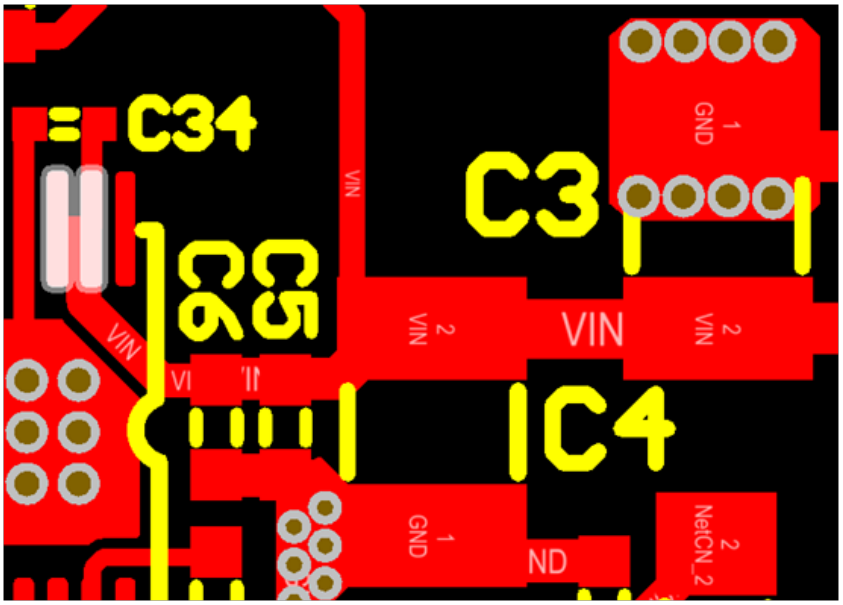

Figure 23: PCB Layout #1

The input ceramic capacitors (C3, C4, C5, C6, C34) must be located as close as possible to the VIN pins. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger capacitors (4.7 µF, 50 V, 1210) should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pin.

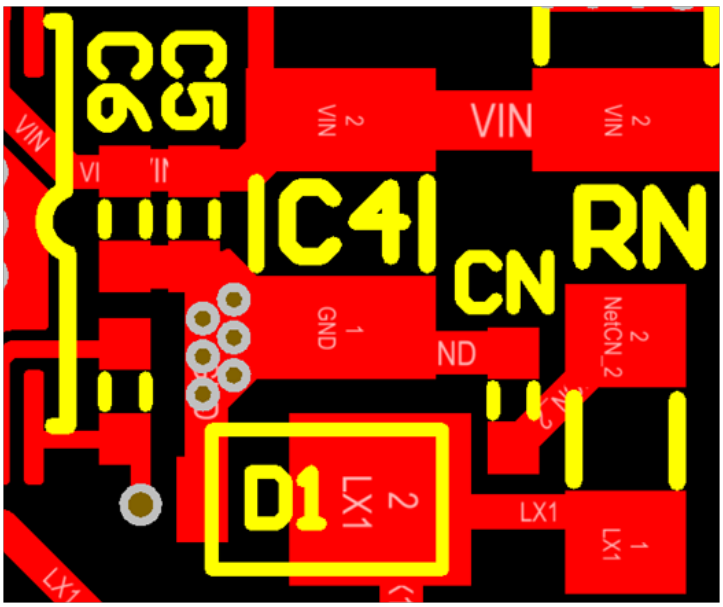

Figure 24: PCB Layout #2

The pre-buck asynchronous diode (D1), input ceramic capacitors (C4, C5, C6), and RC snubber (RN, CN) must be routed on one layer and "star" grounded at a single location with multiple vias.

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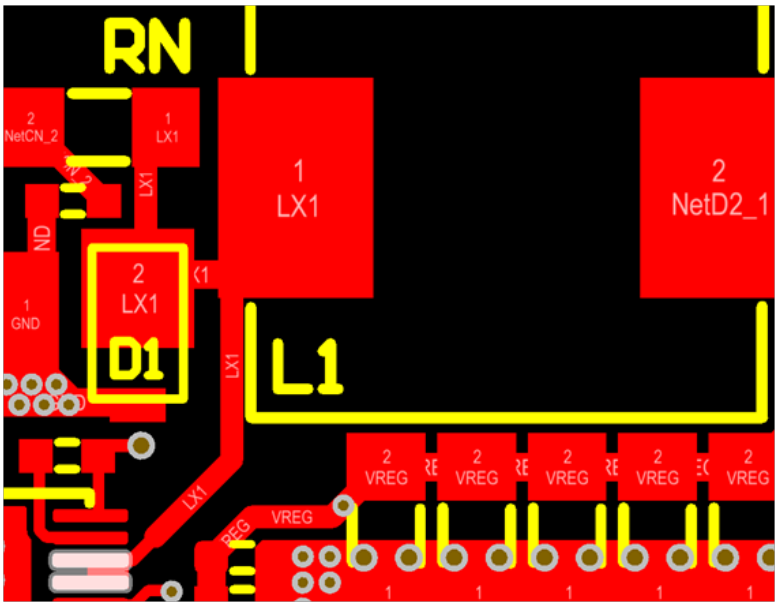

Figure 25: PCB Layout #3

The pre-buck output inductor (L1) should be located close to the LX1 pins.
The LX1 trace widths (to L1, D1, RN) should be relatively wide and preferably on the same layer as the IC.

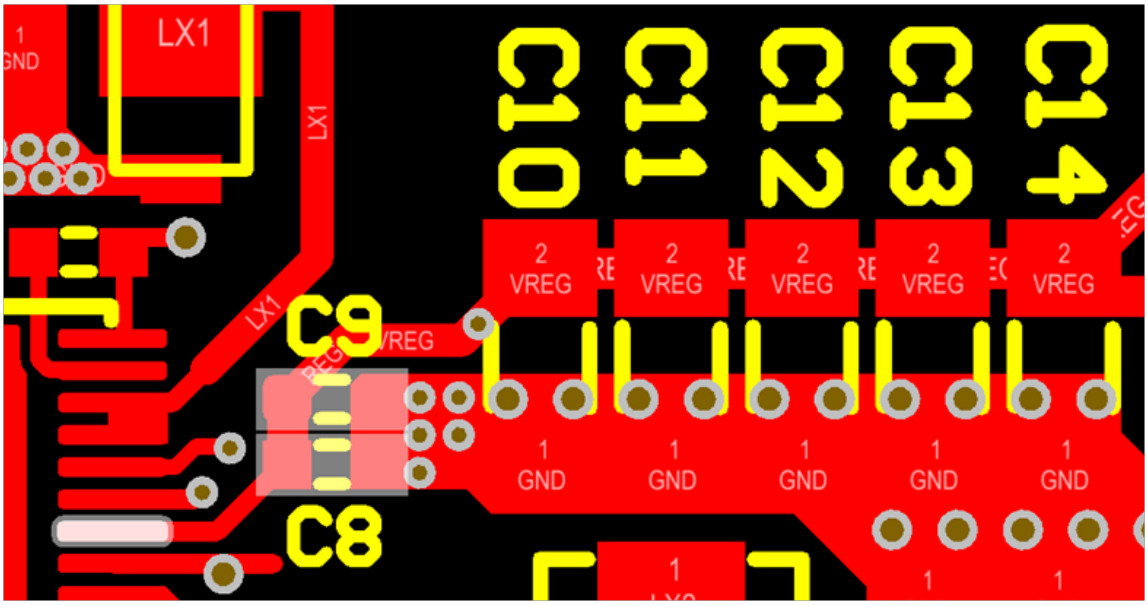

Figure 26: PCB Layout #4

The pre-buck regulators output ceramic capacitors (C10-C14) should be located near the VREG pin.
There must be 1 or 2 smaller ceramic capacitors (C8, C9) as close as possible to the VREG pin.

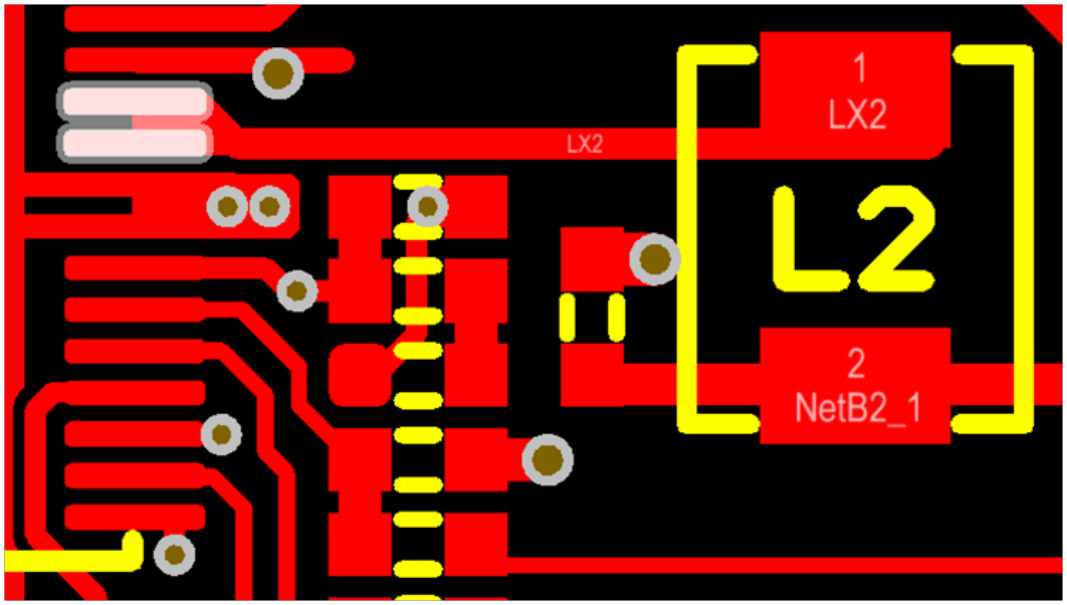

Figure 27: PCB Layout #5

The synchronous buck output inductor should be located near the LX2 pins. The trace from the LX2 pins to the output inductor (L2) should be relatively wide and preferably on the same layer as the IC.

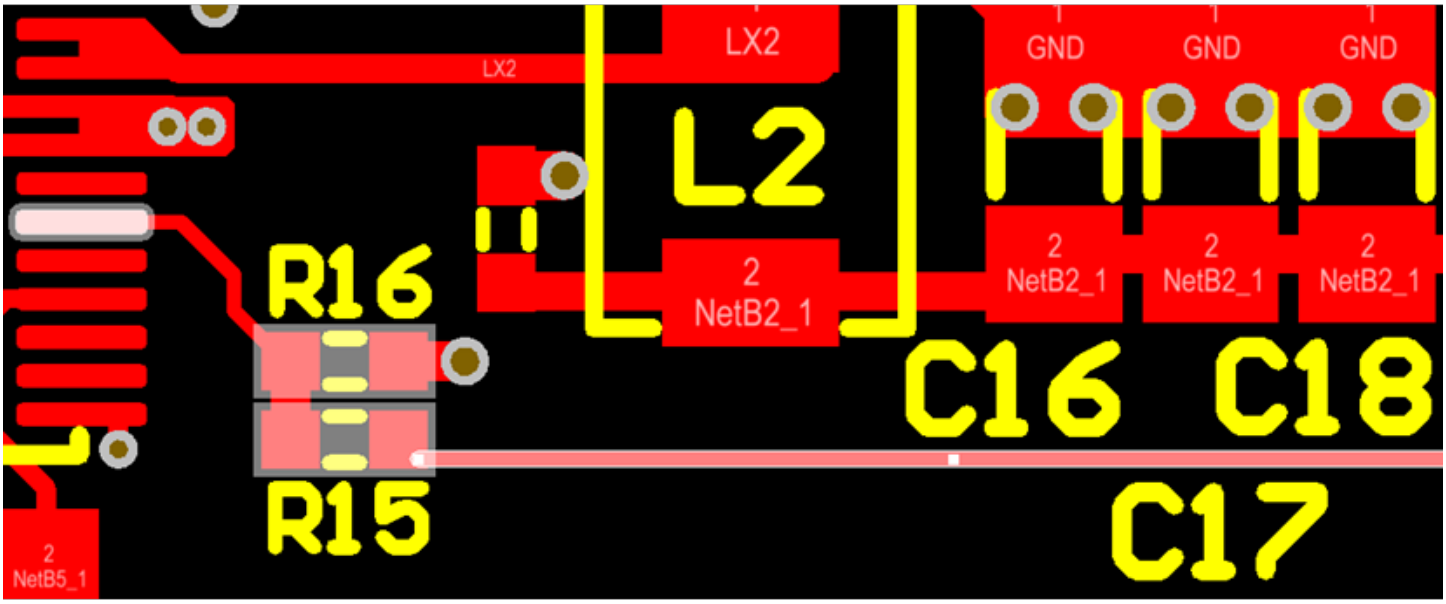

Figure 28: PCB Layout #6

The two feedback resistors (R15, R16) must be located near the FB_{ADJ} pin. The output capacitors (C16-C18) should be located near the load. The output voltage sense trace (to R15) must connect at the load for the best regulation.

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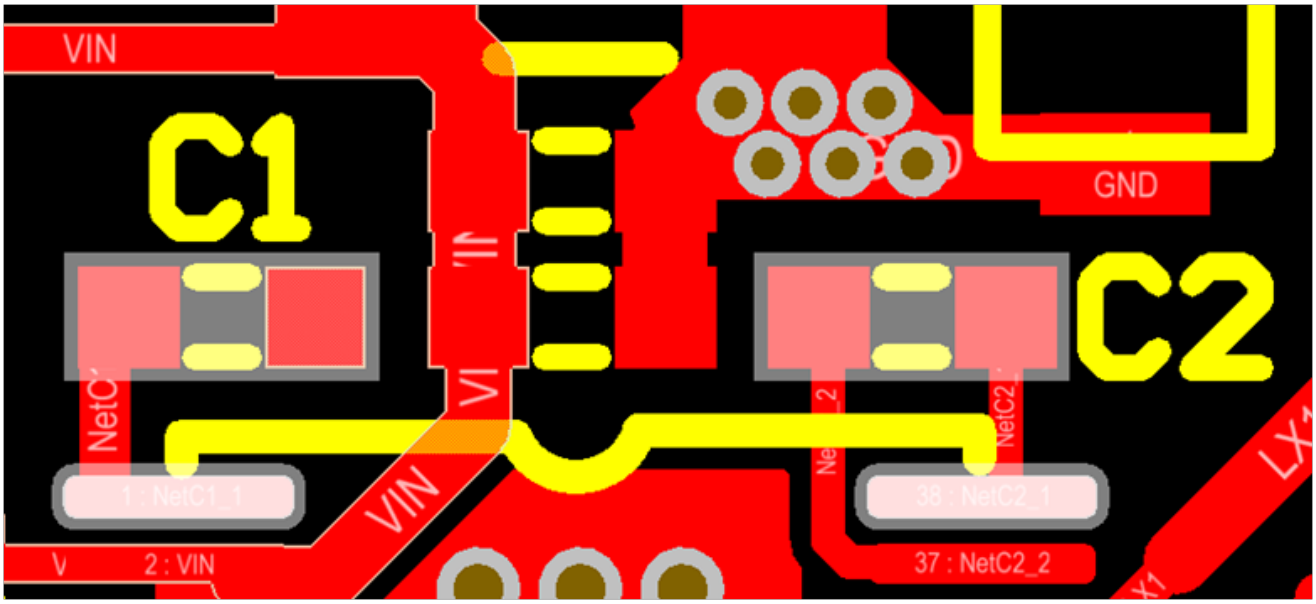

Figure 29: PCB Layout #7

The charge pump capacitors (C1, C2) must be placed as close as possible to VCP and CP1/CP2.

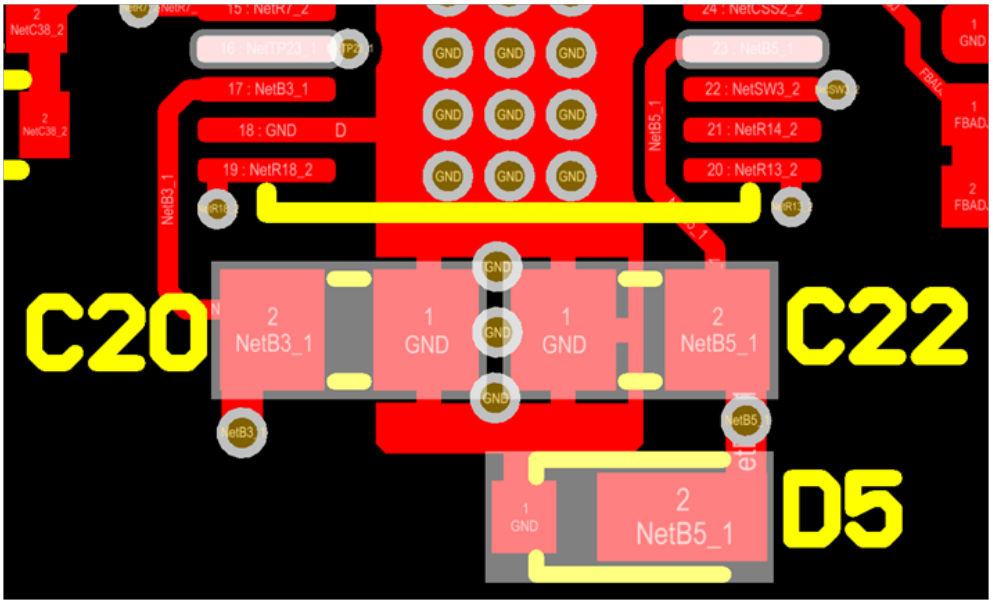

Figure 30: PCB Layout #8

The ceramic capacitors for the LDOs (3V3, V5, V5P, $V5_{CAN}$, $V5_{SNR}$, etc) must be placed near their output pins. The V5P output must have a 1 A/40 V schottky diode (D5) located very close to its pin to limit negative voltages.

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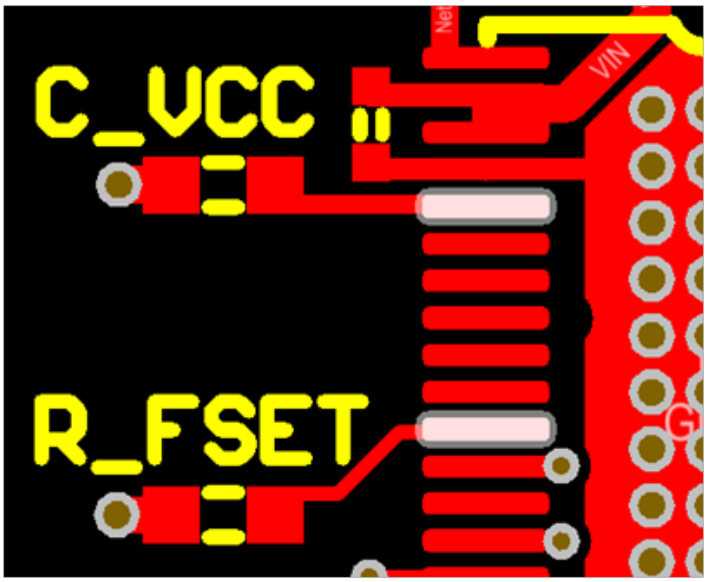


Figure 31: PCB Layout #9

The FSET resistor must be placed very close to the FSET/SYNC pin. Similarly, the VCC bypass capacitor must be placed very close to the VCC pin.

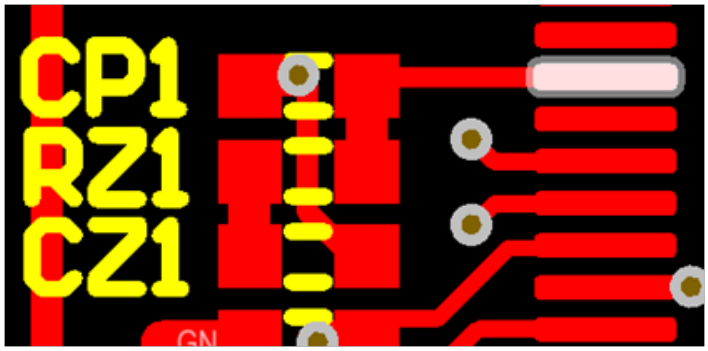


Figure 32: PCB Layout #10

The COMP network for both buck regulators (CZx, RZx, CPx) must be located very close to the COMPx pin.

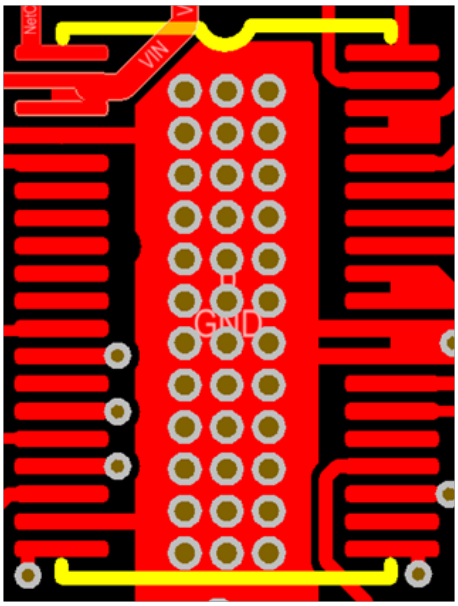


Figure 33: PCB Layout #11

The thermal pad under the A4411 must connect to the ground plane(s) with multiple vias.

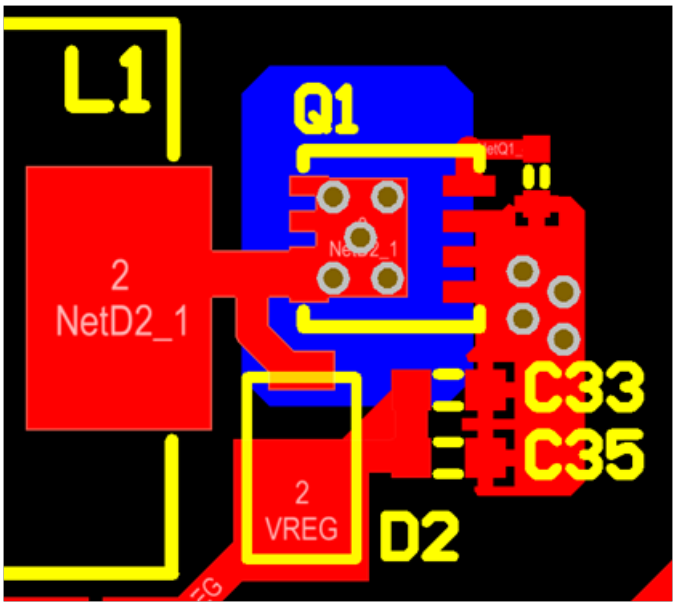
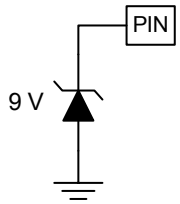


Figure 34: PCB Layout #12

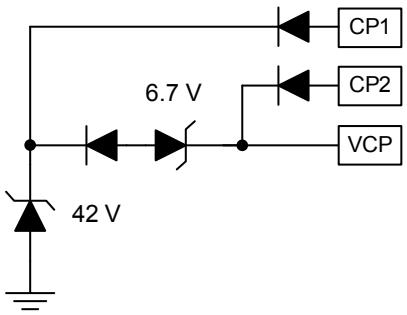
The boost MOSFET (Q1) and the boost diode (D2) must be placed very close to each other. Q1 should have thermal vias to a polygon on the bottom layer. Also, there should be "local" bypass capacitors (C33, C35).

INPUT/OUTPUT STRUCTURES

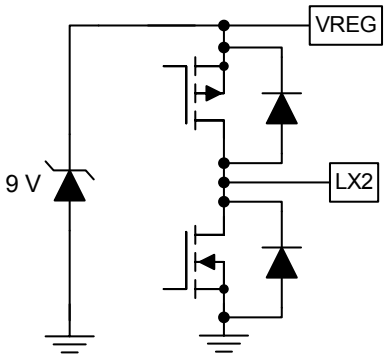
NPOR, POK5V, $V5_{CAN}$, $V5_{SNR}$, VREG, ENB, ENBAT, ENBATS, FB_{ADJ}, COMP1, COMP2, SS1, SS2, FSET/SYNC, TRACK, WD_{IN}, WD_{OUT}, $WD_{CLK,IN}$, WD_{ENn}, WD_{ADJ}, WD_{TOL}, VCC, LG



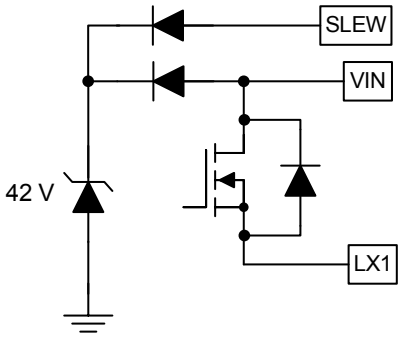
VCP, CP1, CP2



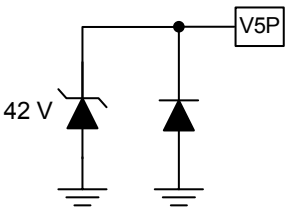
VREG, LX2



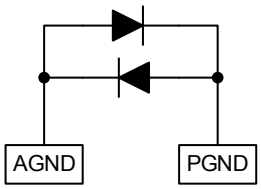
VIN, LX1, SLEW



V5P



AGND, PGND



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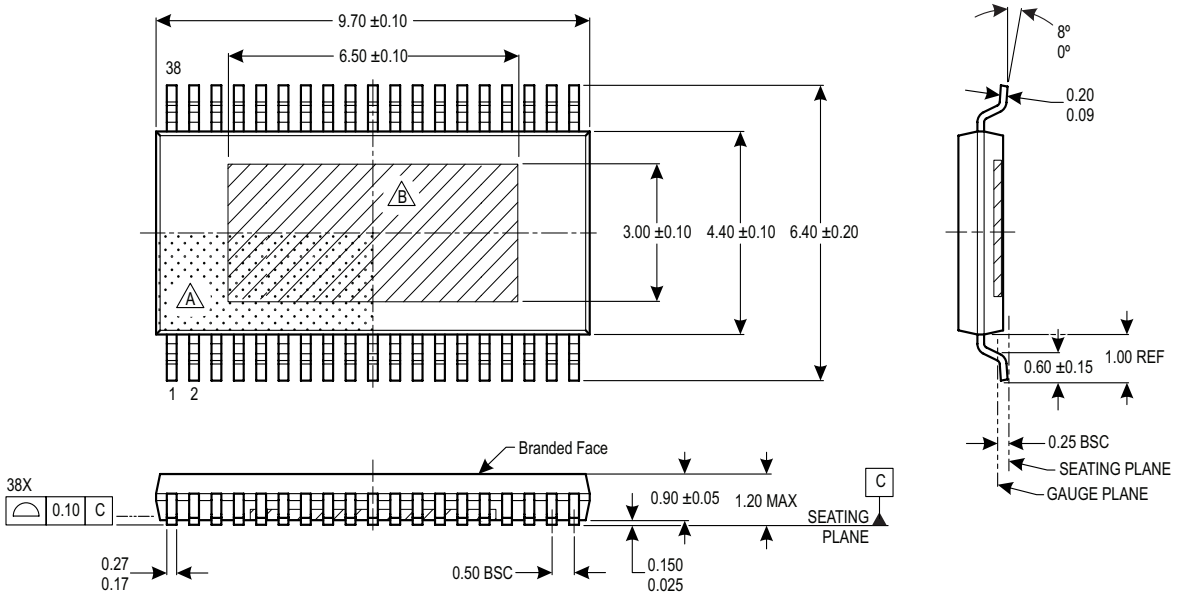
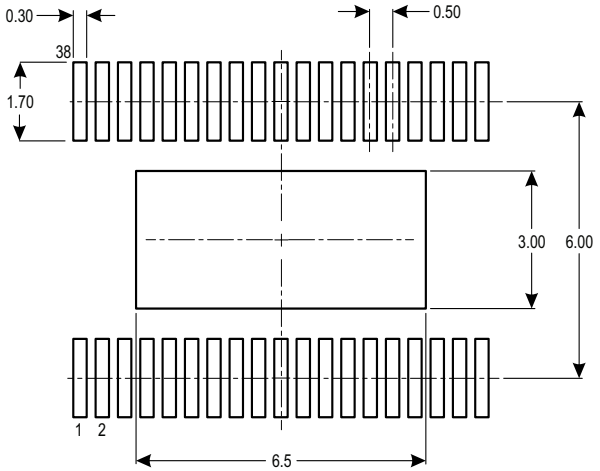
PACKAGE OUTLINE DRAWING

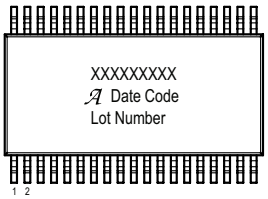
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153 BDT-1)
Dimensions in millimeters
NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 13 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P640X120-39M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Figure 35: Package LV, 38-Pin eTSSOP

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Revision History

Number	Date	Description
–	April 3, 2015	Initial Release
1	June 25, 2015	Dither/Slew START and STOP Threshold on page 8 updated to account for high temperature drift
2	October 26, 2015	Updated WD_{IN} Pulse-Width Programming minimum (page 17) and MPOR definition (page 23).
3	December 9, 2015	Corrected Functional Block Diagram (page 4), Figure 6 (page 20), and Figures 16 and 17 (page 31); updated Watchdog description (page 20).
4	July 15, 2016	Updated Missing Asynchronous Diode voltages (page 10) and NPOR OV/UV Thresholds (page 15).
5	September 2, 2016	Updated Operating Input Voltage, VIN UVLO Start Voltage, and VIN UVLO Stop Voltage values (page 8).
6	October 12, 2016	Updated VIN Dropout Voltages Buck Mode (page 8).
7	June 8, 2017	Added Input/Output Structures (page 44).
8	June 22, 2017	Updated Input/Output Structures (page 44).
9	September 29, 2017	Update Thermal Characteristics table (page 3).
10	October 12, 2018	Minor editorial updates.
11	February 5, 2019	Updated Functional Block Diagram (page 4, L2 component)
12	April 15, 2021	Minor editorial updates; updated Electrical characteristics table, Supply Quiescent Current maximum (page 8) and V5P Accuracy and Load Regulation minimum and maximum (page 13)
13	April 19, 2022	Updated package drawing (page 45)

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