

## Wide Input 5 V, 50 mA, Automotive Regulator with Output Short-to-Battery Protection and Power OK

### FEATURES AND BENEFITS

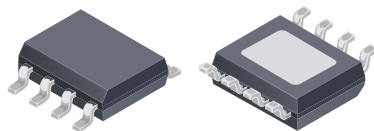
- Automotive AEC-Q100 qualified
- Wide operating range of 3.5 to 28 V, with 40 V load dump rating
- Linear regulator output with foldback short-circuit and short-to-battery protection
- Boost function to maintain output when input is low
- Power OK (POK) flag
- High-voltage logic-level enable input (ENB) for microprocessor or ignition control
- Pin-to-pin and pin-to-ground tolerant at every pin

### APPLICATIONS

- Microcontroller power
- Transceivers (CAN, LIN, etc.) power supplies
- Sensors

### PACKAGE

8-pin SOIC with exposed thermal pad (suffix LJ)



Not to scale

### DESCRIPTION

The A4480 is a wide input regulator with complete control, diagnostics, and protection features that address many requirements of automotive applications. It includes a boost function to allow operation with input voltages from 3.5 to 28 V, while maintaining a 5 V output voltage. The A4480 is able to supply up to 50 mA of load current.

An enable pin (ENB) allows control of the regulator output. This pin is rated to operate at up to 40 V, so it can be connected directly to a car battery.

Diagnostic output from the A4480 includes an open-drain Power OK (POK) output to alert the microprocessor that a fault has occurred.

Protection features include input undervoltage lockout (UVLO), foldback overcurrent protection, output under/overvoltage protections (UV/OVP), and thermal shutdown (TSD). In addition, the output is protected from a short-to-battery event.

The A4480 device is available in an 8-pin eSOIC package with exposed pad for enhanced thermal dissipation. It is lead (PB) free, with 100% matte tin leadframe plating.

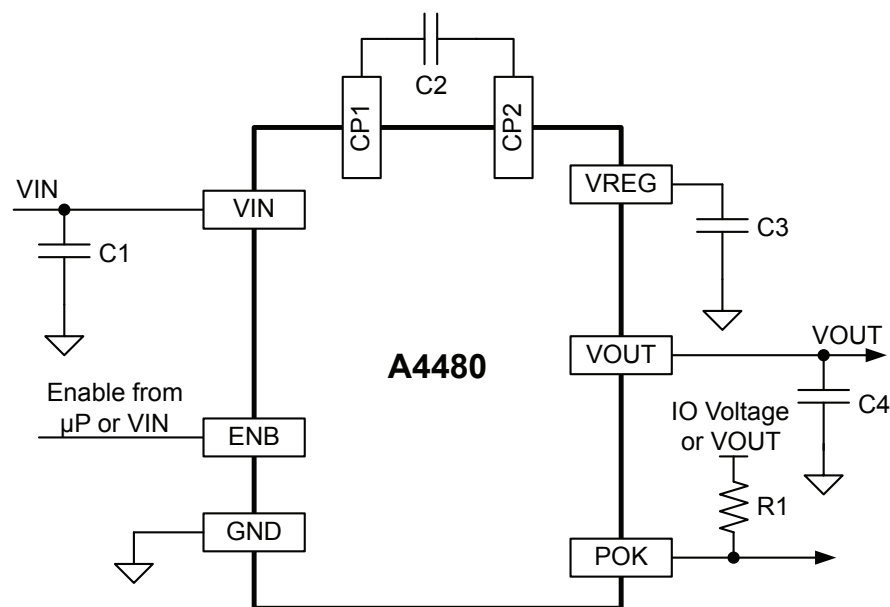


Figure 1: Typical Application Circuit

# A4480

## Wide Input 5 V, 50 mA, Automotive Regulator with Output Short-to-Battery Protection and Power OK

### SELECTION GUIDE

| Part Number  | Temperature Range (°C) | Package                              | Leadframe | Packing*                   |
|--------------|------------------------|--------------------------------------|-----------|----------------------------|
| A4480KLJTR-T | -40 to 150             | 8-pin eSOIC with exposed thermal pad | Matte Tin | 3000 pieces per 7-in. reel |

\*Contact Allegro for additional packing options.



### ABSOLUTE MAXIMUM RATINGS\*

| Characteristic   | Symbol   | Notes                          | Rating     | Unit |
|--|--|--------------------------------|------------|------|
| V <sub>IN</sub> , ENB, CP1                             | V <sub>IN</sub> , V <sub>ENB</sub> , V <sub>CP1</sub>  |                                | -0.3 to 40 | V    |
| V <sub>CP2</sub> , V <sub>REG</sub> , V <sub>POK</sub> | V <sub>CP2</sub> , V <sub>REG</sub> , V <sub>POK</sub> |                                | -0.3 to 20 | V    |
| V <sub>OUT</sub>                                       | V <sub>OUT</sub>                                       | Independent of V <sub>IN</sub> | -1 to 40   | V    |
| Junction Temperature Range                             | T <sub>J</sub>   |                                | -40 to 165 | °C   |
| Storage Temperature Range                              | T <sub>stg</sub>                                       |                                | -40 to 150 | °C   |

\*Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### THERMAL CHARACTERISTICS\*: May require derating at maximum conditions; see application section for optimization

| Characteristic                                   | Symbol           | Test Conditions*   | Value | Unit |
|--|------------------|--|-------|------|
| Package Thermal Resistance (Junction to Ambient) | R <sub>θJA</sub> | eSOIC-8 with thermal pad (LJ) package on 4-layer PCB based on JEDEC standard | 35    | °C/W |

\*Additional thermal information available on the Allegro website.

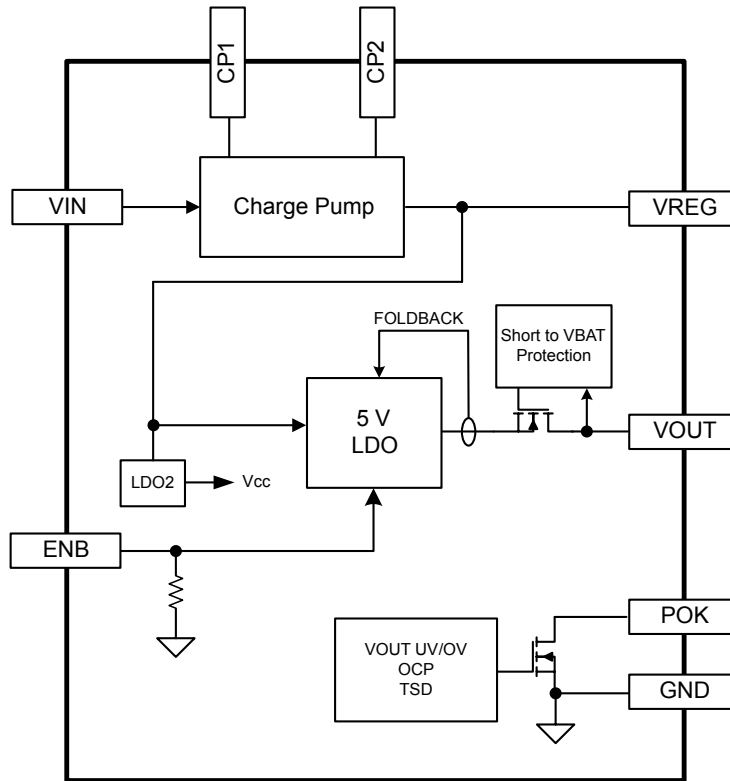
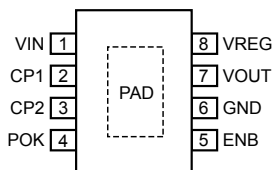


Figure 2: Functional Block Diagram

### Pinout Diagram



### Terminal List Table

| Number | Name | Function   |
|--------|------|--|
| 1      | VIN  | Connection for input voltage. Connect a 2.2 $\mu$ F capacitor from this pin to GND. Keep capacitor close to A4480.   |
| 2      | CP1  | Internal charge pump flying capacitor connection, connect a 0.47 $\mu$ F ceramic capacitor from this pin to the CP2 pin. Keep capacitor close to A4480.      |
| 3      | CP2  | Internal charge pump flying capacitor connection, use a 0.47 $\mu$ F capacitor to CP1.   |
| 4      | POK  | Open-drain active-high Power OK signal. Use a 100 k $\Omega$ pull-up resistor to system IO rail or VOUT.   |
| 5      | ENB  | Regulator active high enable input. Can be connected to VIN or logic level signal.   |
| 6      | GND  | Ground pin.  |
| 7      | VOUT | Regulated output pin. It is recommended to use a 4.7 $\mu$ F ceramic capacitor from this pin to GND. Keep capacitor close to A4480.                          |
| 8      | VREG | Charge pump output which is input to internal linear regulator. Connect a 2.2 $\mu$ F ceramic capacitor from this pin to GND. Keep capacitor close to A4480. |

**ELECTRICAL CHARACTERISTICS** [1]: Valid at  $3.5\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ ,  $-40^\circ\text{C} \leq T_{\text{J}} \leq 150^\circ\text{C}$ , unless otherwise specified

| Characteristics                      | Symbol                   | Test Conditions   | Min. | Typ. | Max.  | Units         |
|--------------------------------------|--------------------------|---|------|------|-------|---------------|
| <b>INPUT VOLTAGE</b>                 |                          |   |      |      |       |               |
| Operating Input Voltage              | $V_{\text{IN}}$          | ENB high and after $V_{\text{IN}} > 6.0\text{ V}$   | 3.5  | 13.5 | 28    | V             |
| VIN UVLO Start Voltage               | $V_{\text{IN(START)}}$   | $V_{\text{IN}}$ rising, ENB high  | 3.1  | –    | 3.45  | V             |
| VIN UVLO Stop Voltage                | $V_{\text{IN(STOP)}}$    | $V_{\text{IN}}$ falling, ENB high   | 2.6  | –    | 2.9   | V             |
| VIN UVLO Hysteresis                  | $V_{\text{IN(HYS)}}$     | $V_{\text{IN(START)}} - V_{\text{IN(STOP)}}$  | –    | 0.6  | –     | V             |
| <b>INPUT CURRENT</b>                 |                          |   |      |      |       |               |
| Input Quiescent Current [1]          | $I_{\text{Q}}$           | $V_{\text{IN}} = 13.5\text{ V}$ , ENB high  | –    | 4    | –     | mA            |
| Input Sleep Supply Current [1]       | $I_{\text{Q(SLEEP)}}$    | $V_{\text{IN}} = 13.5\text{ V}$ , ENB low   | –    | 1    | 10    | $\mu\text{A}$ |
| <b>CHARGE PUMP</b>                   |                          |   |      |      |       |               |
| Output Voltage                       | $V_{\text{REG}}$         | ENB high, $5\text{ mA} \leq I_{\text{OUT}} \leq 50\text{ mA}$ , $V_{\text{IN}} = 3.95\text{ V}$           | 5.25 | –    | 7     | V             |
|                                      |                          | ENB high, $5\text{ mA} \leq I_{\text{OUT}} \leq 33\text{ mA}$ , $V_{\text{IN}} = 3.5\text{ V}$            | 5.25 | –    | 7     | V             |
| Switching Frequency                  | $f_{\text{SW}}$          |   | –    | 325  | –     | kHz           |
| Doubler to Pass Through Switchover   | $V_{\text{DOUBLER(H)}}$  | $V_{\text{IN}}$ rising  | 7.8  | –    | 8.65  | V             |
| Pass Through to Step Down Switchover | $V_{\text{STEPDOWN(H)}}$ | $V_{\text{IN}}$ rising  | 11.5 | –    | 12.45 | V             |
| Step Down to Pass Through Switchover | $V_{\text{STEPDOWN(L)}}$ | $V_{\text{IN}}$ falling   | 10.5 | –    | 11.7  | V             |
| Pass Through to Doubler Switchover   | $V_{\text{DOUBLER(L)}}$  | $V_{\text{IN}}$ falling   | 6.9  | –    | 7.5   | V             |
| <b>5 V LINEAR REGULATOR</b>          |                          |   |      |      |       |               |
| Accuracy and Load Regulation         | $V_{\text{OUT}}$         | $5\text{ mA} \leq I_{\text{OUT}} \leq 50\text{ mA}$ , $3.95\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ | 4.9  | 5.0  | 5.1   | V             |
|                                      |                          | $5\text{ mA} \leq I_{\text{OUT}} \leq 33\text{ mA}$ , $3.5\text{ V} \leq V_{\text{IN}} < 3.95\text{ V}$   | 4.9  | 5.0  | 5.1   | V             |
| Output Capacitance Range [2]         | $C_{\text{OUT}}$         |   | 3    | –    | 10    | $\mu\text{F}$ |
| Startup Time [2]                     | $t_{\text{START}}$       | $C_{\text{OUT}} \leq 4.7\text{ }\mu\text{F}$ , Load = $125\text{ }\Omega \pm 5\%$ (50 mA)                 | 1.4  | 2.2  | 3.0   | ms            |
| <b>LOGIN ENABLE (ENB) INPUT</b>      |                          |   |      |      |       |               |
| ENB Threshold                        | $V_{\text{ENB(H)}}$      | $V_{\text{ENB}}$ rising   | –    | –    | 2.0   | V             |
|                                      | $V_{\text{ENB(L)}}$      | $V_{\text{ENB}}$ falling  | 0.8  | –    | –     | V             |
| ENB Resistance                       | $R_{\text{ENB}}$         |   | –    | 100  | –     | k $\Omega$    |
| ENB Filter/Deglintch Time            | $t_{\text{d(EN,FILT)}}$  |   | 10   | 15   | 20    | $\mu\text{s}$ |

Continued on next page...

**ELECTRICAL CHARACTERISTICS (continued)** <sup>[1]</sup>: Valid at  $3.5\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$ ,  $-40^\circ\text{C} \leq T_{\text{J}} \leq 150^\circ\text{C}$ ,  
unless otherwise specified

| <b>OVERCURRENT PROTECTION (OCP)</b>             |                       |  |      |      |      |    |
|---|-----------------------|--|------|------|------|----|
| Current Limit <sup>[1]</sup>                    | $I_{\text{LIM}}$      | $V_{\text{OUT}} = 5\text{ V}$  | -60  | -100 | -140 | mA |
| Foldback Current <sup>[1]</sup>                 | $I_{\text{FBK}}$      | $V_{\text{OUT}} = 0\text{ V}$  | -15  | -30  | -45  | mA |
| <b>THERMAL PROTECTION (TSD)</b>                 |                       |  |      |      |      |    |
| Thermal Shutdown Threshold <sup>[2]</sup>       | $T_{\text{TSD}}$      | $T_{\text{J}}$ rising  | 165  | -    | -    | °C |
| Thermal Shutdown Hysteresis <sup>[2]</sup>      | $T_{\text{HYS}}$      |  | -    | 15   | -    | °C |
| <b>VOUT OV/UV PROTECTIONS</b>                   |                       |  |      |      |      |    |
| VOUT OV Thresholds                              | $V_{\text{OV(H)}}$    | $V_{\text{OUT}}$ rising, $V_{\text{IN}} = 13.5\text{ V}$                     | 5.15 | 5.33 | 5.50 | V  |
|   | $V_{\text{OV(L)}}$    | $V_{\text{OUT}}$ falling, $V_{\text{IN}} = 13.5\text{ V}$                    | -    | 5.30 | -    | V  |
| VOUT OV Hysteresis                              | $V_{\text{OV(HYS)}}$  | $V_{\text{OV(H)}} - V_{\text{OV(L)}}$ , $V_{\text{IN}} = 13.5\text{ V}$      | 15   | -    | 50   | mV |
| VOUT UV Thresholds                              | $V_{\text{UV(H)}}$    | $V_{\text{OUT}}$ rising, $V_{\text{IN}} = 13.5\text{ V}$                     | -    | 4.71 | -    | V  |
|   | $V_{\text{UV(L)}}$    | $V_{\text{OUT}}$ falling, $V_{\text{IN}} = 13.5\text{ V}$                    | 4.50 | 4.68 | 4.85 | V  |
| VOUT UV Hysteresis                              | $V_{\text{UV(HYS)}}$  | $V_{\text{UV(H)}} - V_{\text{UV(L)}}$ , $V_{\text{IN}} = 13.5\text{ V}$      | 15   | -    | 50   | mV |
| VOUT Output Disconnect Threshold                | $V_{\text{DISC}}$     | $V_{\text{OUT}}$ rising, $V_{\text{IN}} = 13.5\text{ V}$                     | -    | 7.2  | -    | V  |
| <b>POK OUTPUTS</b>                              |                       |  |      |      |      |    |
| POK Output Low Voltage                          | $V_{\text{POK(L)}}$   | ENB high, $V_{\text{IN}} \geq 3.5\text{ V}$ , $I_{\text{POK}} = 1\text{ mA}$ | -    | 150  | 400  | mV |
| POK Leakage Current <sup>[1]</sup>              | $I_{\text{POK(LKG)}}$ | $V_{\text{POK}} = 3.3\text{ V}$  | -    | -    | 35   | μA |
| OV and UV Filter/Deglintch Times <sup>[2]</sup> | $t_{\text{d(FILT)}}$  | Applies to undervoltage of the $V_{\text{OUT}}$ voltages                     | 10   | 15   | 20   | μs |

<sup>[1]</sup> For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

<sup>[2]</sup> Ensured by design and characterization, not production tested.

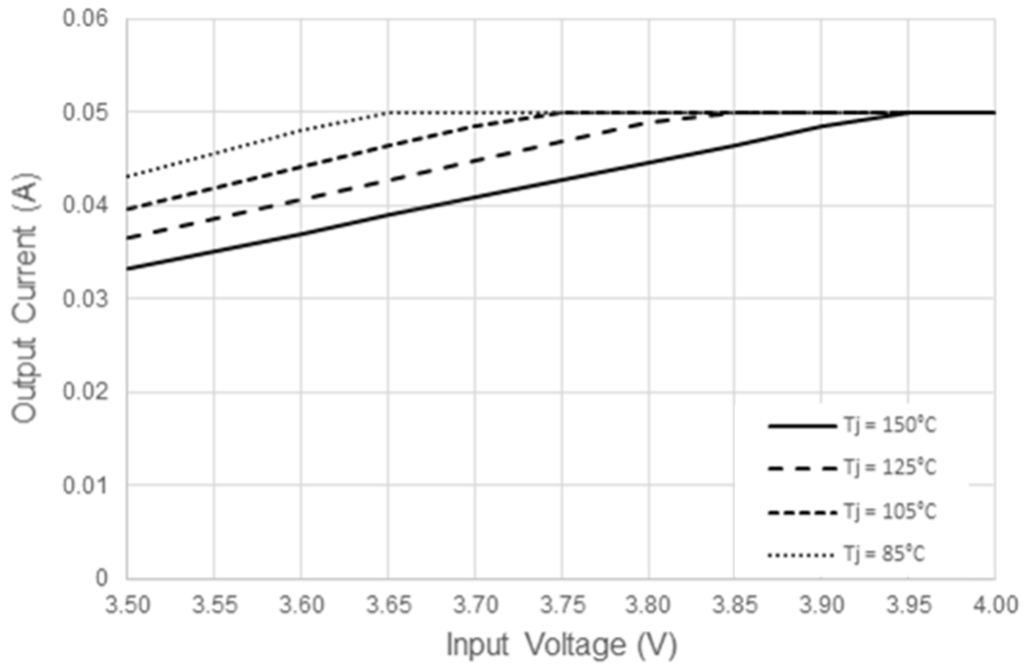


Figure 3: Output Current Derating versus Input Voltage

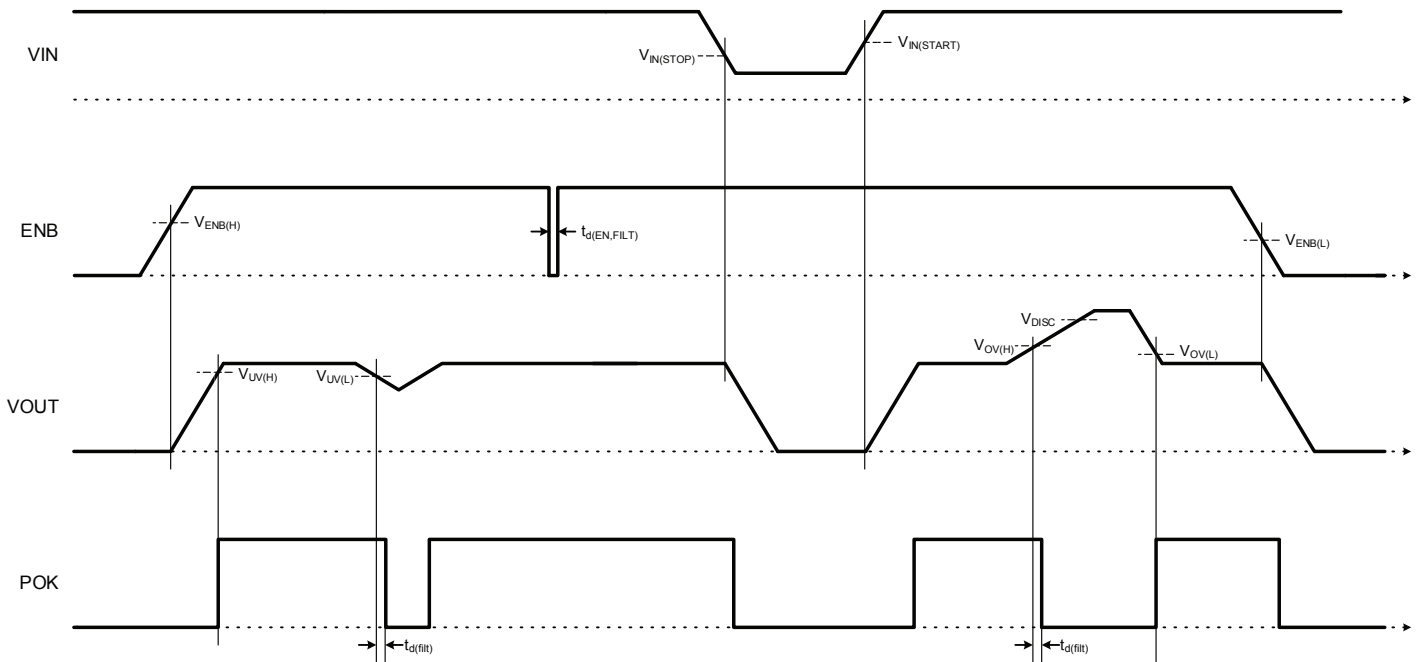
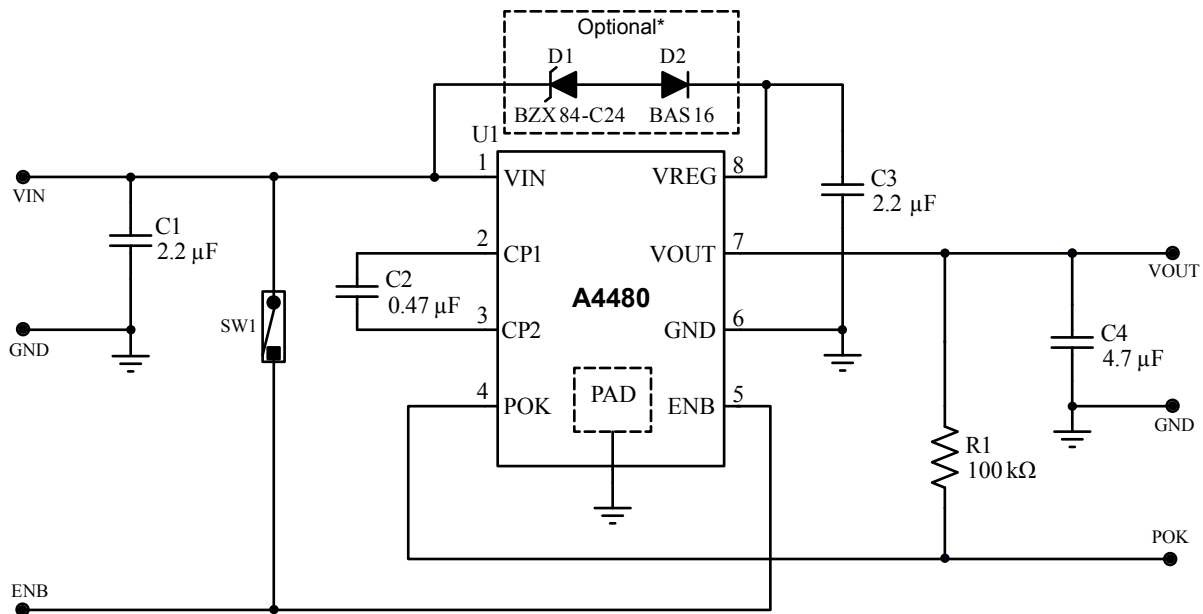


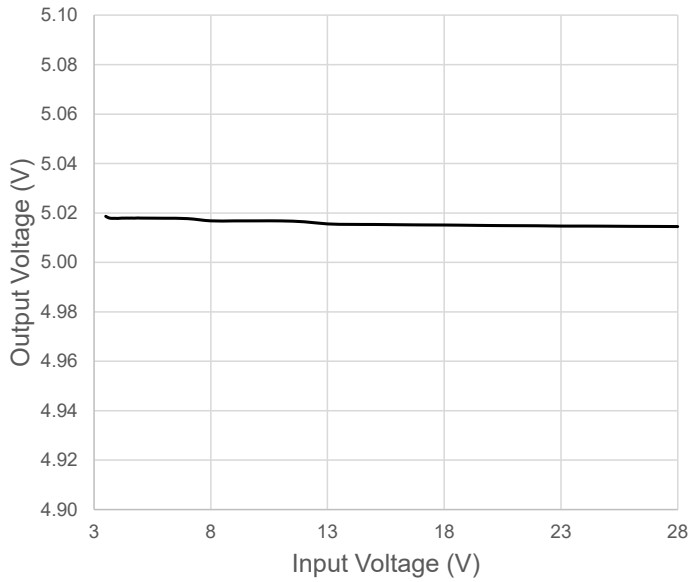
Figure 4: Timing Diagram (not to scale)



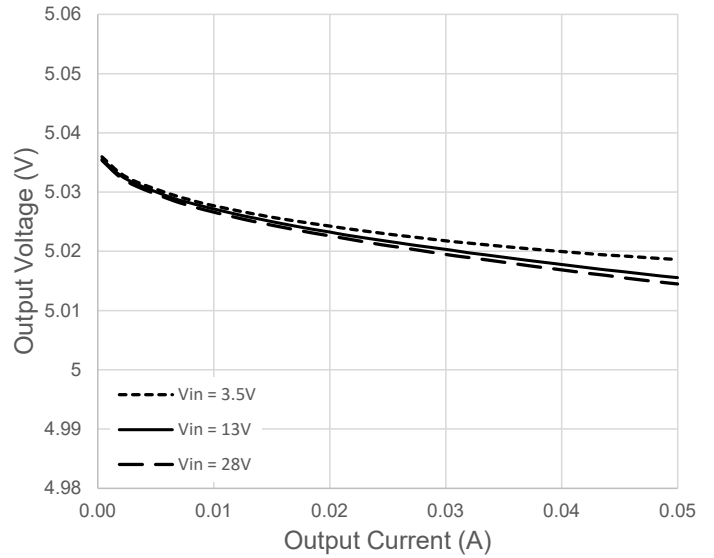
\* Diodes D1 and D2 are only required if A4480 must be enabled when  $V_{IN}$  is greater than 28 V. If A4480 is already enabled before  $V_{IN}$  is greater than 28 V or if A4480 is off then operation to 40 V is possible without D1 and D2 diodes.

**Figure 5: Typical Application Schematic**

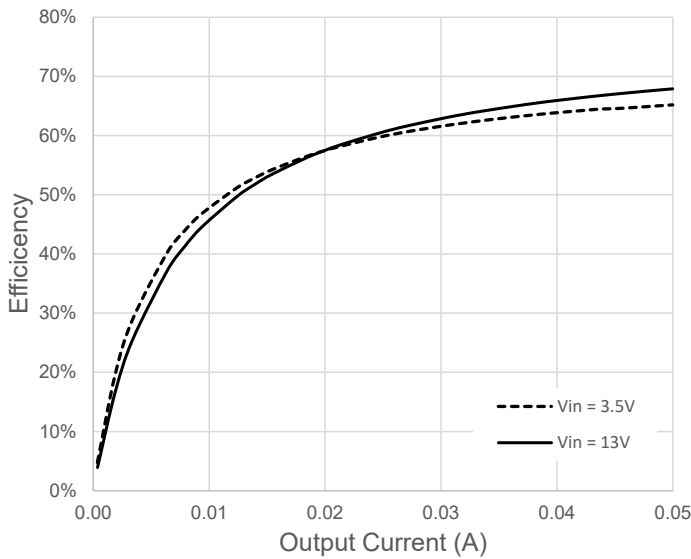
### PERFORMANCE DATA



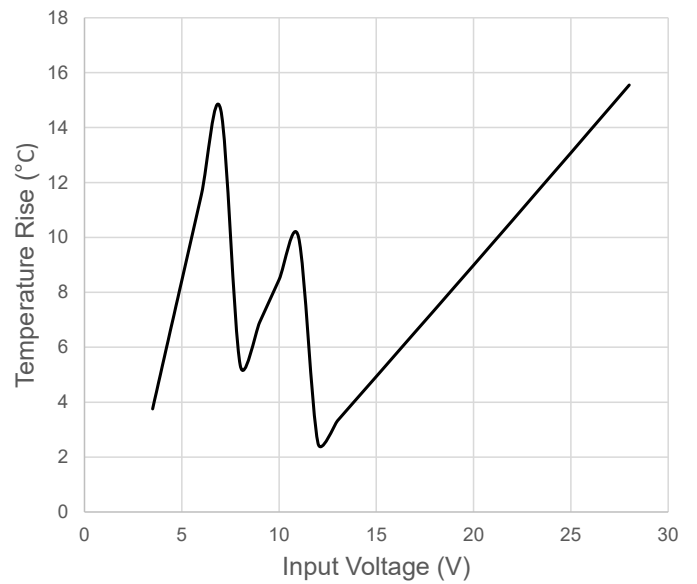
**Line Regulation at 50 mA**



**Load Regulation**



**Typical Efficiency**



**Estimated Temperature Rise**



### PCB LAYOUT GUIDELINES

The A4480 contains a switching charge pump circuit, so care must be taken when placing this part on the system PCB. The four decoupling capacitors (C1, C2, C3, and C4) must be placed as close to the A4480 as possible. Figure 6 below shows the recommend layout. The input capacitor C1 is placed next to pin 1 of

the A4480 (U1). It connects directly to the pin 6 using copper on the top side of the PCB. The charge pump flying capacitor (C2) connects directly to pins 2 and 3 of A4480. The VREG capacitor connects to pins 8 and 6; top-side copper should only be used for this connection. The output capacitor (C4) connects to pins 7 and 8.

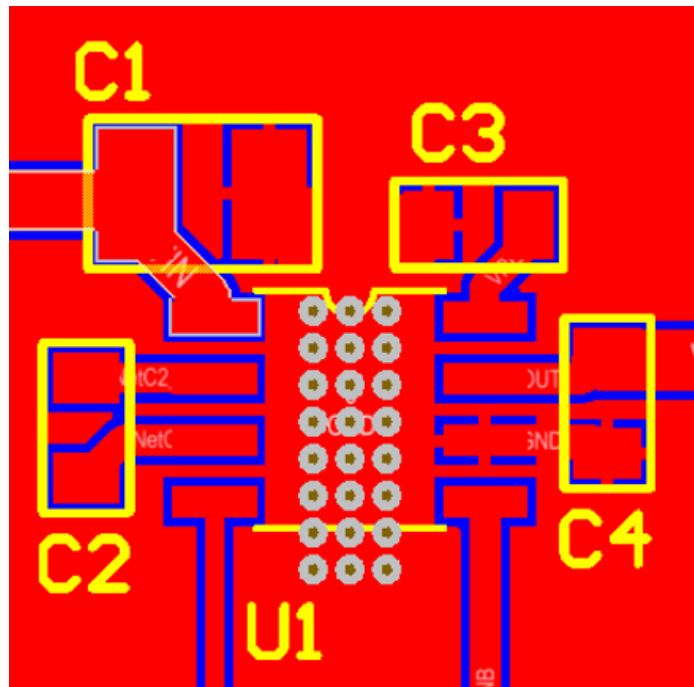


Figure 6: Typical Layout of the A4480

The vias under the A4480 are recommended for improved thermal performance. The ground copper plane should be as large as possible to reduce the junction to ambient thermal impedance of the A4480.

### PACKAGE OUTLINE DRAWING

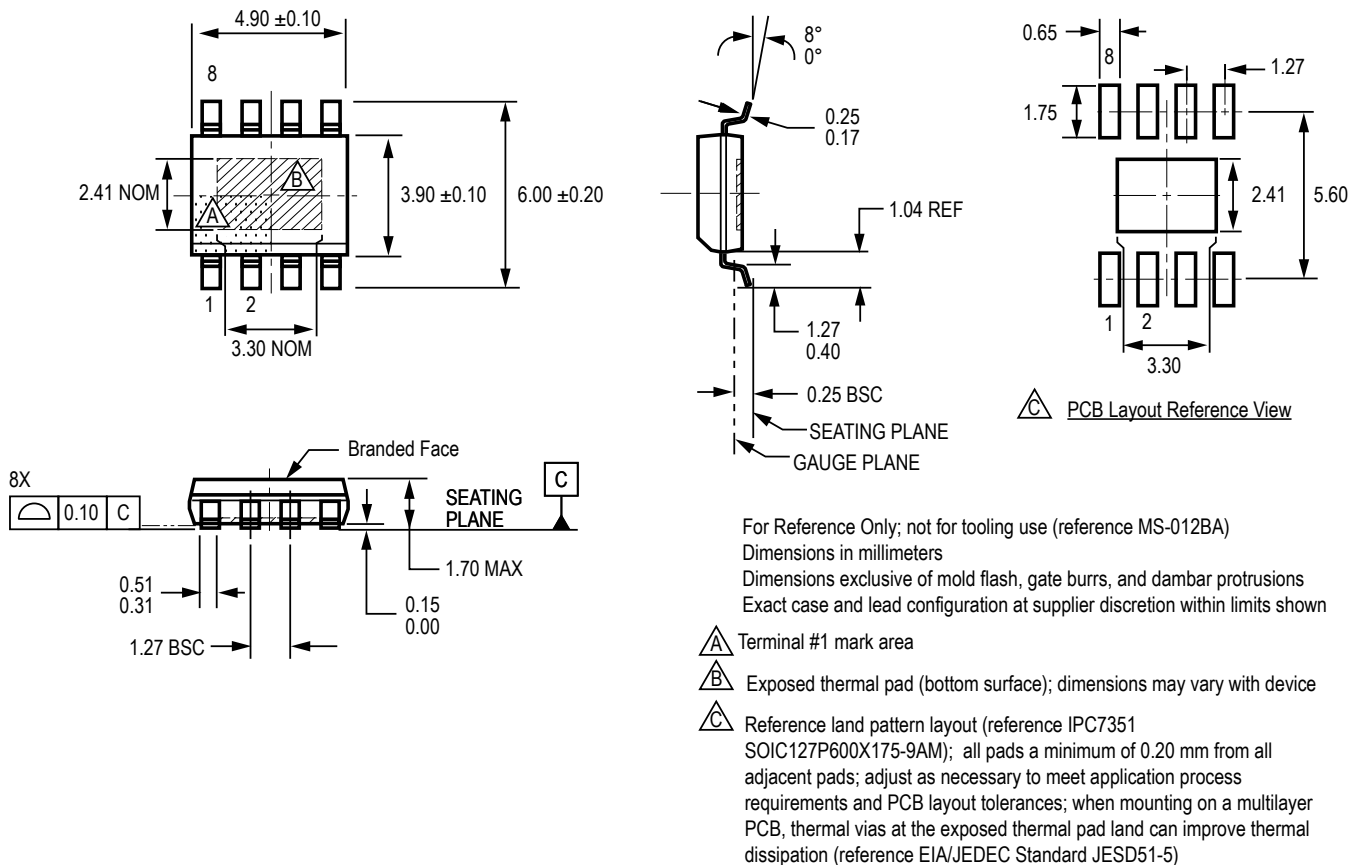


Figure 7: Package LJ, 8-Pin eSOIC

**Revision History**

| Number | Date          | Description  |
|--------|---------------|--|
| –      | June 1, 2017  | Initial release  |
| 1      | July 10, 2017 | Updated Charge Pump Output Voltage test conditions (page 4), Accuracy and Load Regulation test conditions (page 4), and Figure 3 (page 6). |
| 2      | July 5, 2018  | Minor editorial updates  |
| 3      | July 12, 2019 | Minor editorial updates  |

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