

## Automotive Three-Phase MOSFET Driver

### FEATURES AND BENEFITS

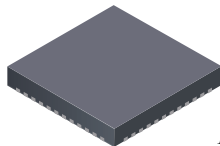
- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low-supply-voltage operation
- Top-off charge pump for 100% pulse-width modulation (PWM)
- Programmable gate-drive voltage and strength
- 4.5 to 50 V supply-voltage operating range
- Integrated logic supply
- Three programmable current-sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- ASIL Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual



### PACKAGES

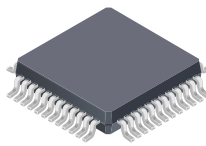
48-pin QFN with exposed thermal pad and wettable flank

(suffix EV)



48-pin LQFP with exposed thermal pad

(suffix JP)



Not to scale

### DESCRIPTION

The A4918 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as brushless DC (BLDC) motors.

A unique charge-pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the A4918 to operate with a reduced gate drive down to 4.5 V. Gate-drive voltage and strength are programmable to help reduce electromagnetic-compatibility (EMC) issues. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs with an additional above-battery charge pump to ensure that the bootstrap capacitors remain charged when held in the on state.

Full control is provided over all six power MOSFETs in the three-phase bridge. This allows motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power-bridge faults, and can be configured to protect the power MOSFETs in most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface. The serial interface is provided to alter programmable settings and read back detailed diagnostic data.

The A4918 was developed in accordance with ISO 26262 as a hardware safety element out-of-context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The A4918 is supplied in a 48-terminal wettable-flank quad-flat no-lead (QFN) package (suffix EV) and a 48-pin quad-flat package (QFP) (suffix JP), both with exposed thermal pad. These packages are lead (Pb) free with 100% matte tin leadframe plating.

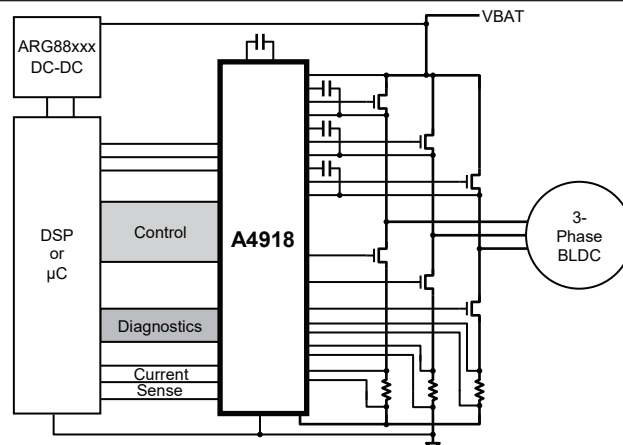


Figure 1: Typical Application

## SELECTION GUIDE

Part Number	I/O Logic	Packing	Package
A4918KEVSR-1A-3-T	3.3 V	4000 pieces per 13-inch reel	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank
A4918KEVSR-1A-5-T	5 V		
A4918KJPTR-1A-3-T	3.3 V	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-lead QFP with exposed thermal pad
A4918KJPTR-1A-5-T	5 V		



## PACKAGE OUTLINE DRAWINGS

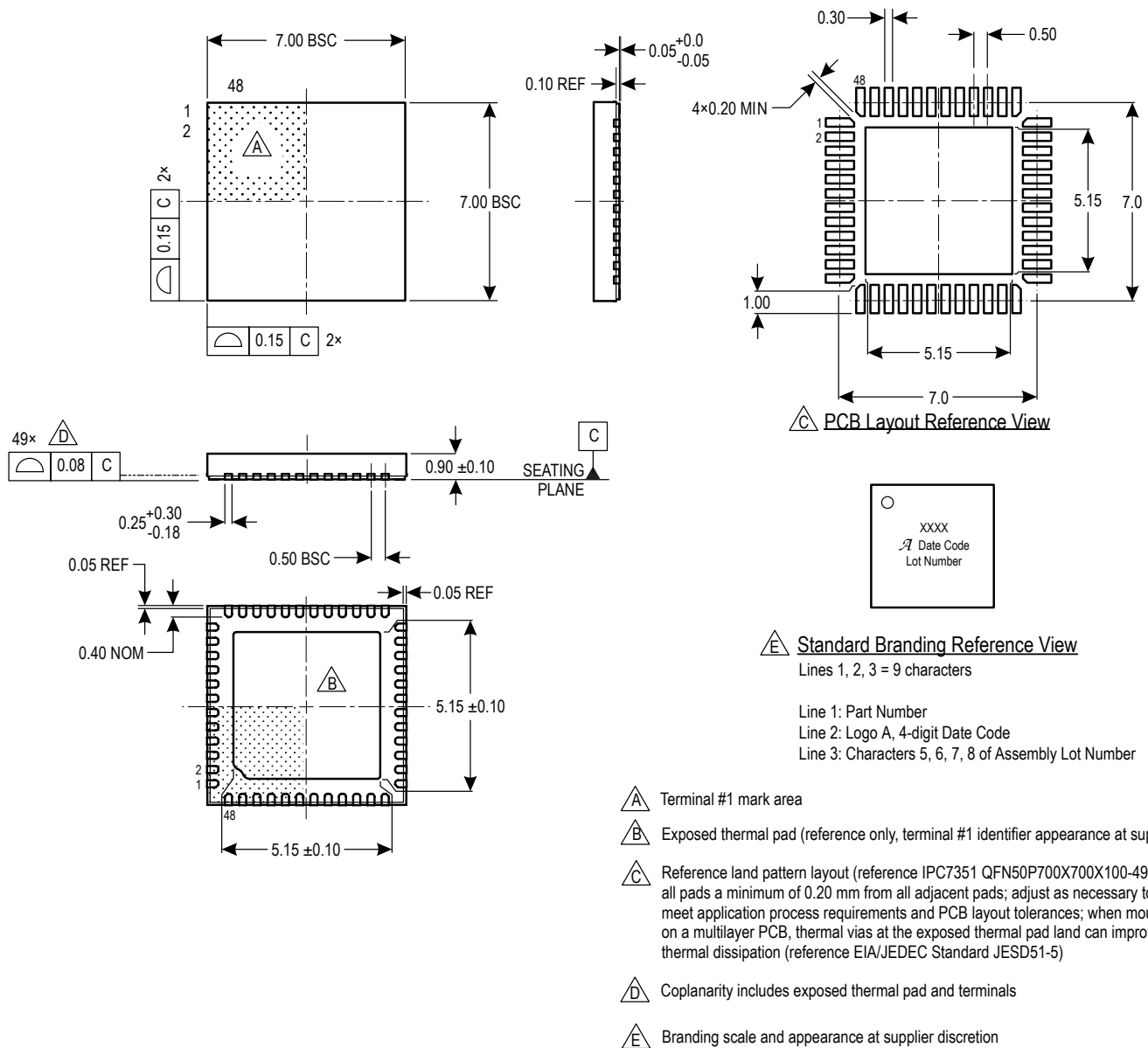
**For Reference Only – Not for Tooling Use**

(Reference DWG-0000378, Rev. 3)

Dimensions in millimeters

NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown



**Figure 2: EV Package, 48-Pin QFN with Exposed Thermal Pad and Wettable Flank**

## For Reference Only – Not for Tooling Use

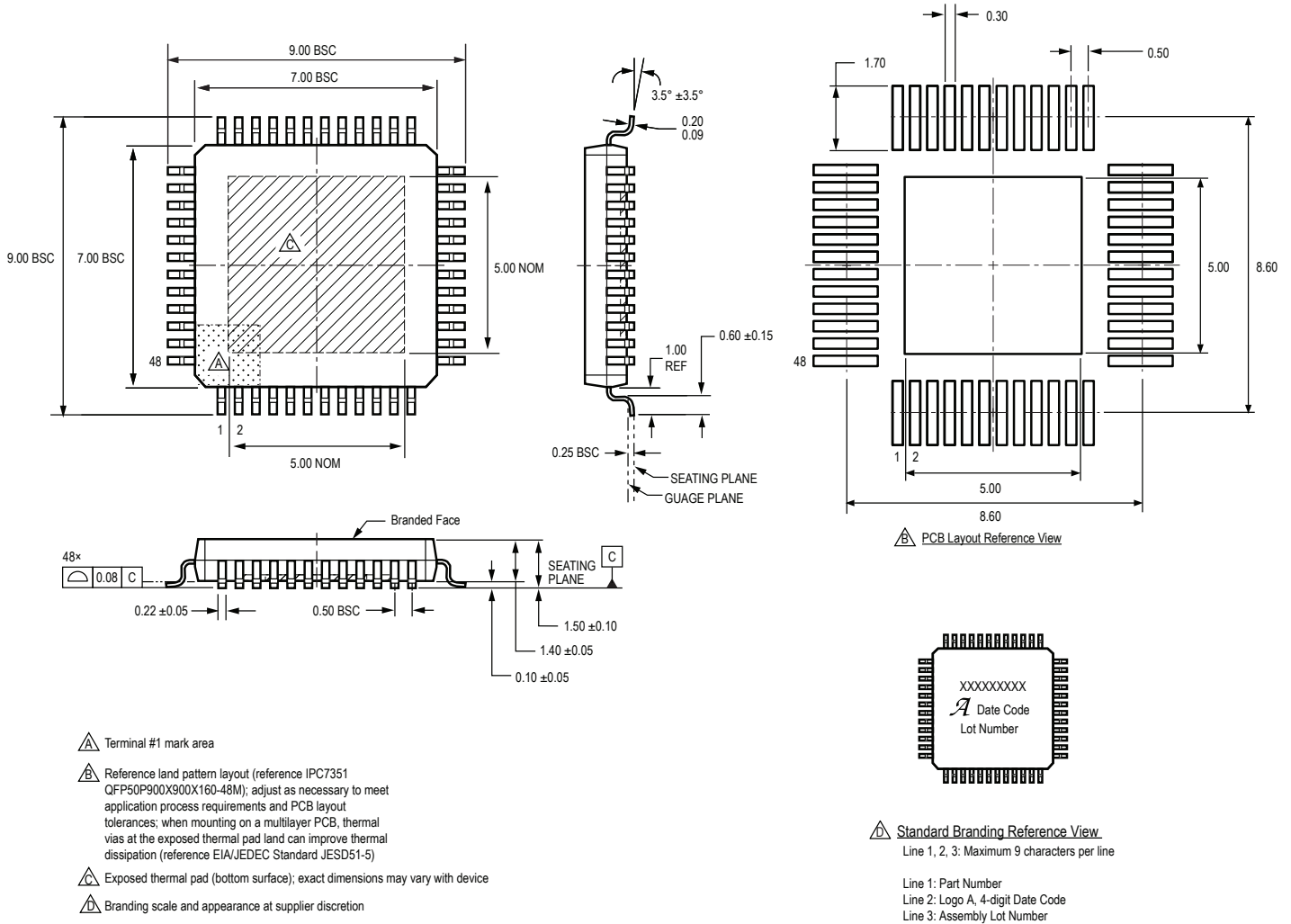
(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown



**Figure 3: JP Package, 48-Pin LQFP with Exposed Thermal Pad**

## Revision History

Number	Date	Description
–	February 9, 2021	A4918-1A initial release. Derived from A4918-A datasheet dated 2 Dec 2019. Part numbers amended (page 2)
1	March 2, 2022	Updated package drawings (pages 69-70)
2	April 11, 2024	Changed logic I/O characteristic of input pull-down STRn to “input pull-up STRn” (page 8), updated DIAG output temperature range test conditions (page 11), updated bridge terminal connection verification diagram (page 36), updated serial register definition (page 43)
3	September 18, 2024	Created short-form variant of long-form datasheet
4	December 15, 2025	Updated ASIL branding and text (page 1) and made minor editorial and formatting modifications throughout (all pages)

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