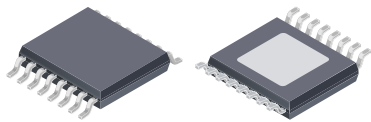# Three-Phase Fan Driver

FEATURES AND BENEFITS

- 180° sinusoidal drive
- PWM speed input
- Analog speed input
- FG speed output
- Lock detection
- Overcurrent protection
- Short circuit protection
- Wide power supply range
- Soft start

PACKAGE

16-pin TSSOP
with exposed thermal pad
(LP package)

Not to scale

DESCRIPTION

The A4944 three-phase motor driver incorporates sinusoidal control to minimize audible noise and vibration as well as to provide highly efficient operation of appliance or personal computer (PC) fans.

Pulse-width modulation (PWM) or analog voltage input can be used to control motor speed. This allows system cost savings by eliminating external variable power supply. Alternatively, the speed can be controlled by varying power supply amplitude over a wide range (4 to 17 V).

A soft-start circuit reduces the demand on the power supply at startup. When the motor is forced to a stop by a rotor lock condition, a lock-detection circuit, which does not require external components, disables the output driver.

The A4944 is supplied in a low-profile 16-pin thin-shrink small-outline package (TSSOP) with exposed thermal pad (suffix LP). The package is lead (Pb) free with 100% matte tin leadframe plating.

FUNCTIONAL BLOCK DIAGRAM
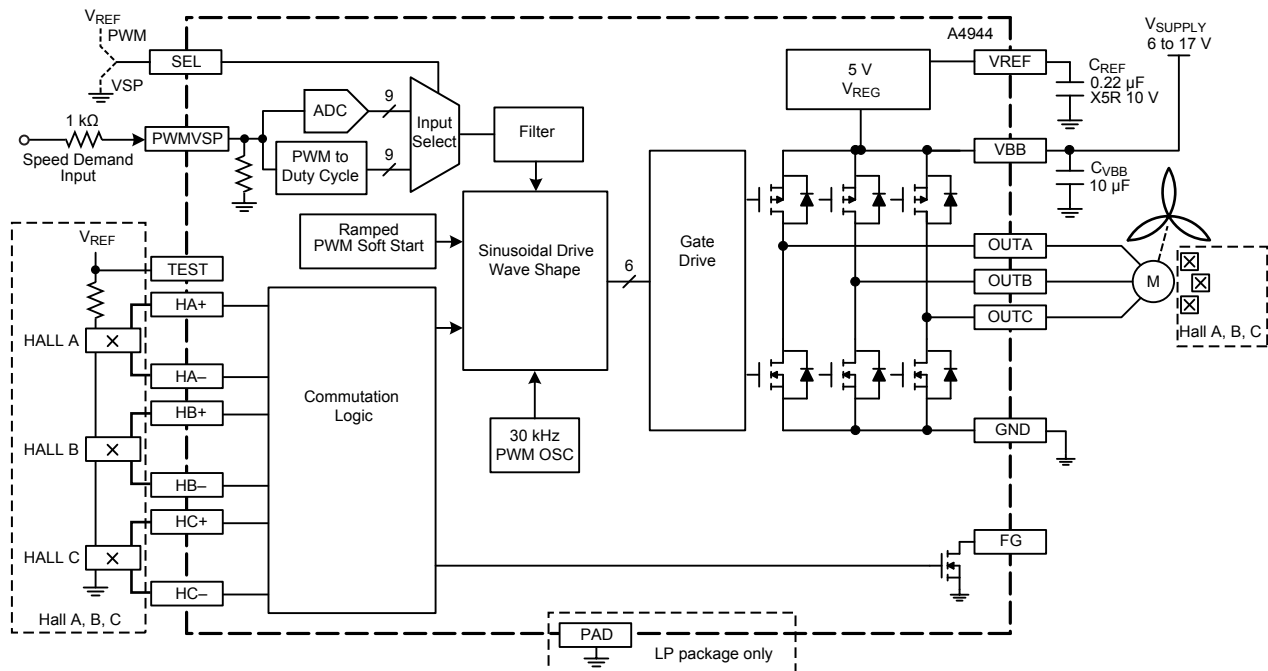
SELECTION GUIDE

Part Number	Packing	Package
A4944GLPTR-T	4000 pieces per 13-inch reel	16-pin TSSOP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		18	V
Logic Input Voltage Range	V_{IN}	PWMVSP and SEL pins	–0.3 to 6	V
Logic Output	V_O	FG pin	V_{BB}	V
Output Current	I_{OUT}		1.2	A
Hall Inputs	V_{Hx}		6	V
Output Voltage	V_{OUT}		V_{BB} + 1	V
Reference Voltage	V_{REF}		5.5	V
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP package, 2-sided PCB with 3.8 in.^{2} copper each side	43	°C/W
		LP package, 4-layer PCB based on JEDEC standard	34	°C/W

PINOUT DIAGRAM AND TERMINAL LIST TABLE

```
HA+  1  ⚬              16  PWMVSP
HA−  2                 15  SEL
HB+  3                 14  FG
HB−  4   ┌ ─ ─ ─ ┐    13  OUTA
HC+  5   │  PAD  │    12  GND
HC−  6   └ ─ ─ ─ ┘    11  OUTB
TEST 7                 10  OUTC
VREF 8                  9  VBB
```
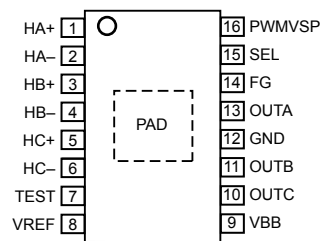
LP Package Pinout

Terminal List Table

Number	Name	Function
1	HA+	Input Hall element A
2	HA−	Input Hall element A
3	HB+	Input Hall element B
4	HB−	Input Hall element B
5	HC+	Input Hall element C
6	HA−	Input Hall element C
7	TEST	Connect to VREF
8	VREF	Analog output
9	VBB	Input supply
10	OUTC	Motor terminal phase C
11	OUTB	Motor terminal phase B
12	GND	Ground
13	OUTA	Motor terminal phase A
14	FG	Speed output
15	SEL	Analog input
16	PWMVSP	Logic Input
–	PAD	Exposed thermal pad

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{BB}		6	–	17	V
Output Current	I_{OUT}		–	–	600	mA
Hall Input Amplitude	V_{HALL}	Peak to peak	50	–	–	mV
PWM Input Frequency	f_{PWM}		2.5	–	35	kHz
Hall Bias Current	I_{HALL}		–	–	10	mA

ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{BB} = 4 to 17 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Current	I_{BB}	PWMVSP = 50%, I_{HALL} = 0 mA	–	9	15	mA
Output Driver Leakage	I_{LK}	PWMVSP = 0	–10	–	10	µA
Driver On-Resistance	$R_{DS(on)}$	Sink + Source; I_{OUTx} = 500 mA, T_J = 25°C, V_{BB} = 12 V	1	1.3	1.6	Ω
		Sink + Source; I_{OUTx} = 500 mA, T_J = 25°C, V_{BB} = 4 V	–	1.6	–	Ω
		Source only; I_{OUTx} = 500 mA, T_J = 25°C, V_{BB} = 12 V	–	0.85	–	Ω
		Sink only; I_{OUTx} = 500 mA, T_J = 25°C, V_{BB} = 12 V	–	0.45	–	Ω
VREF Pin Voltage	V_{REF}	I_{REF} = 0 to 10 mA, V_{BB} = 6 V	4.75	5	5.25	V
VREF Dropout	V_{REFDO}	I_{REF} = 10 mA, V_{BB} = 4 V	100	400	600	mV
Logic Input Low Level	V_{IL}	PWMVSP and SEL pins	–	–	0.8	V
Logic Input High Level	V_{IH}		2	–	–	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Input Current (SEL pin)	I_{SELIN}	V_{SELIN} = 5 V, (50 kΩ pull-down)	50	100	150	uA
Input Current (PWMVSP pin)*	I_{PWPIN}	V_{PWPIN} = 5V (100 kΩ pull-down)	25	50	75	uA
Output Saturation Voltage	V_{SAT}	I_{FG} = 5 mA	–	–	0.3	V
FG Output Leakage Current	I_{FG}	V_{FG} =18 V	–	–	1	uA
VSP ADC Input Range	V_{ADC}	PWMVSP pin, monotonic, V_{BB} = 6 V	0	–	4.35	V
PWM Signal Input Resolution	RES_{PWM}	PWMVSP pin	–	–	9	bit
VSP On-Threshold	V_{SPON}		1.02	1.12	1.22	V
VSP Off-Threshold	V_{SPOFF}		0.48	0.58	0.68	V
VSP Maximum Demand	V_{SPMAX}	V_{BB} = 6 V	4.15	4.25	4.35	V
Duty Cycle On-Threshold	D_{ON}		23.75	25	26.25	%
Duty Cycle Off-Threshold	D_{OFF}		11.88	12.5	13.12	%

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = 25°C, V_{BB} = 4 to 17 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
Lock Protection	t_{OFF}		7	8	9	s
	t_{ON}		0.9	1	1.1	s
VBB Undervoltage Lockout (UVLO)	V_{BBUVLO}	V_{BB} rising	3.5	3.8	3.98	V
VBB UVLO Hysteresis	V_{BBHYS}		160	300	480	mV
Dead Time	t_{DT}		325	400	475	ns
Motor PWM Frequency	f_{PWM}		28	30	32	kHz
Pulse Reject Filter	T_W		430	600	840	ns
Overcurrent Threshold	I_{CL}		0.8	1	1.2	A
Soft-Start Time	t_{SS}	PWM duty ramp 25% to 100% duty cycle	0.95	1.152	1.45	s
Hall Element Input Range	V_H		0.5	–	$V_{REF} - 1$	V
Hall Element Offset	V_{OFF}		−5	0	+5	mV
Hysteresis	V_{HYS}	Relative to V_{OFF}	5	13	21	mV
Hall Element Minimum Amplitude	V_H		50	–	–	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	T_{JHYS}	Recovery = $T_{JTSD} - T_{JHYS}$	–	20	–	°C

[1] Specified limits are tested at a single temperature and determined across the operating temperature range by design and characterization.

FUNCTIONAL DESCRIPTION

Lock Detect. A logic circuit monitors the inputs from the Hall position sensors in order to determine if the motor is running as expected. If a fault is detected, the motor drive is disabled for a period of 8 seconds before an auto-restart is attempted. The retry duration is 1 second. Because the on:off ratio is 8:1, neither the IC nor the motor overheat. This cycle continues until the fault condition is removed.

The lock-detect circuit is triggered by any of the following:

- Time between Hall sensor input transitions is less than 52 ms: That value is less than the expected running speed for fan motors (96 rpm for a 4-pole motor, 48 rpm for an 8-pole motor, etc.).

- Invalid Hall conditions:The three inputs from the Hall sensors (HA, HB, and HC) are either all low (000) or all high (111).

- Direction error: The motor is rotating in the wrong direction, which can occur if the Hall sensors are not wired correctly.

FG. This open-drain output provides speed data to the system. The system controller can use this data to make adjustments in relation to the speed-demand input, in order to achieve the required speed.

FG changes state in synchronization with the HC+ Hall sensor input, at a rate of one period per electrical rotation of the motor. This open-drain output is rated to 18 V. This allows the pull-up resistor to be connected to VBB.

Current Limit. During a locked rotor condition, the current ramps up to the internal current limit. Load current is monitored on the high-side MOSFETs. If the current reaches I_{CL}, the source driver is turned off for 24 µs, to allow the current to decay.

VREF. This 5 V reference powers internal logic and analog circuitry. VREF can be used to power the Hall sensor elements with a bias current of up to 10 mA, if required. Stabilize this circuit with a 0.22 µF or greater ceramic capacitor.

TEST. For factory test use only. Connect this pin to VREF.

PWMVSP. This is the speed-demand input pin. To select analog voltage control or PWM duty control, configure the logic state of SEL as follows:

- For PWM mode, tie SEL to VREF.

- For VSP (analog voltage) mode, connect SEL to GND.

Speed Demand Control. The speed-demand transfer function translates the analog or PWM signal on the PWMVSP pin into a percentage of the motor driver output range. The relationship is diagrammed in Figure 1.

When the device is configured for analog control (VSP), an increase in the voltage applied to the PWMVSP pin increases speed demand. This is performed by an internal 9-bit analog-to-digital (A-to-D) converter that translates the input into a speed demand. The resolution of the ADC is 8.4 mV.

The analog configuration also can be used where the system cannot provide a PWM frequency in an appropriate range. An external circuit can be used to translate a PWM-signal duty cycle to an appropriate analog signal. (For more information, see the Application Information section.)

When the device is configured for PWM duty-cycle control, an external PWM signal with a frequency in the range 2.5 to 35 kHz can be used. In this configuration, if the PWMVSP pin becomes open circuit, the motor coasts to a stop.
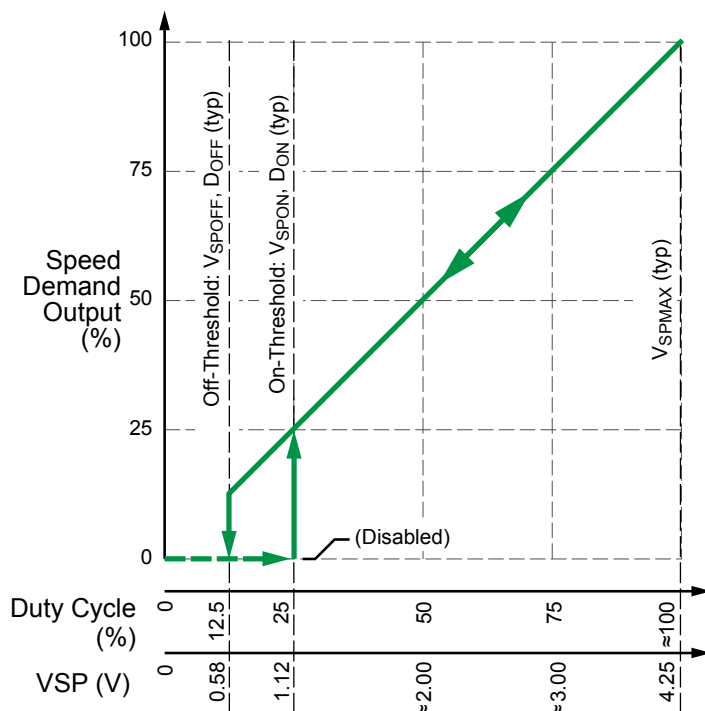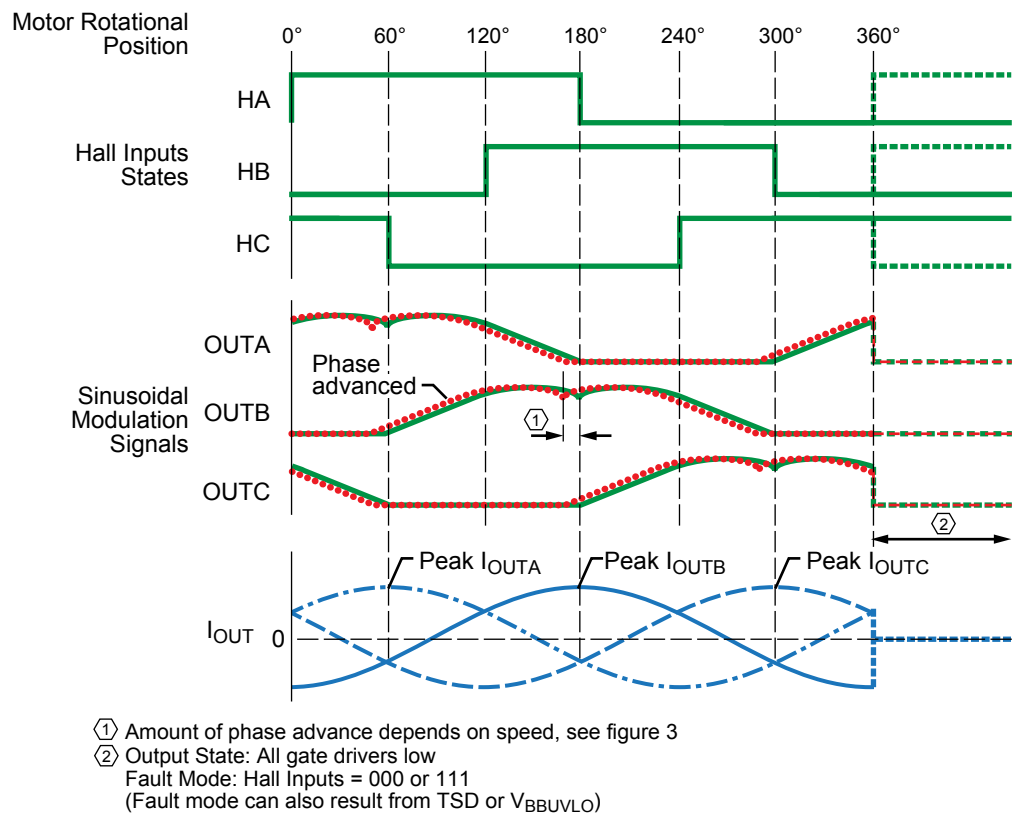

Figure 1: Duty and Voltage Input versus Speed-Demand Output

Commutation State Table

Hall Input State			Motor Driver Phase State			
HA	**HB**	**HC**	**OUTA**	**OUTB**	**OUTC**	**Operation Mode**
H	L	H	Sinusoidal PWM	Low	Sinusoidal PWM	Typical
H	L	L	Sinusoidal PWM	Sinusoidal PWM	Low	Typical
H	H	L	Sinusoidal PWM	Sinusoidal PWM	Low	Typical
L	H	L	Low	Sinusoidal PWM	Sinusoidal PWM	Typical
L	H	H	Low	Sinusoidal PWM	Sinusoidal PWM	Typical
L	L	H	Sinusoidal PWM	Low	Sinusoidal PWM	Typical
H	H	H	Z	Z	Z	Fault, all MOSFETS off
L	L	L	Z	Z	Z	Fault, all MOSFETS off

Note: Z indicates high impedance.

① Amount of phase advance depends on speed, see figure 3
② Output State: All gate drivers low
  Fault Mode: Hall Inputs = 000 or 111
  (Fault mode can also result from TSD or V_{BBUVLO})

Soft Start. The soft-start function is integrated into the IC. Soft start ramps both the speed-demand function (output duty cycle) and the current limit to reduce the load on the power supply and smoothly ramp the motor up to speed, as shown in Figure 2. During this ramping, the current takes several steps, at 200, 400, and 600 mA.

The A4944 starts up in trapezoidal-drive mode and switches to sine-drive mode as soon as the motor moves sufficiently fast

(t_{TRAP}). This typically occurs in less than 128 ms. The actual time depends on the motor, the load, and the supply voltage.

After sinusoidal-drive mode begins, the PWM duty cycle is held at D_{ON} until approximately 256 ms after startup, then ramps up to the final value, according to:

$$t_{SS} \ (ms) = 512 \times (Speed \ Demand \ (\%) - 25\%) \times 3 \ (ms)$$
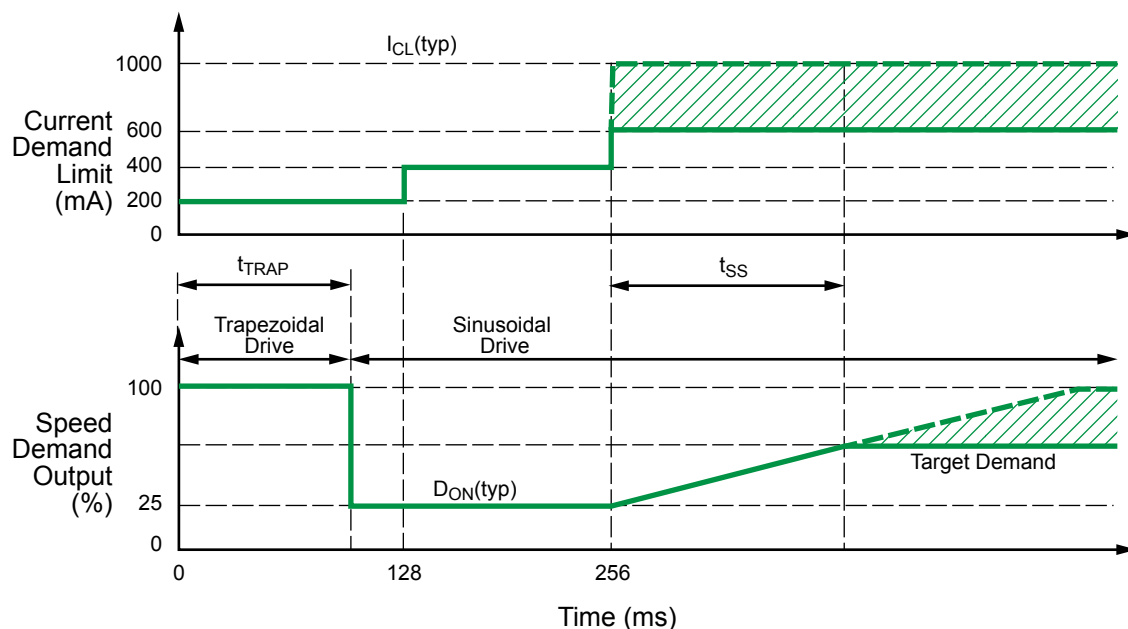
Figure 2: Effect of Soft-Start Operation on Output Current Limit and Speed-Demand Output
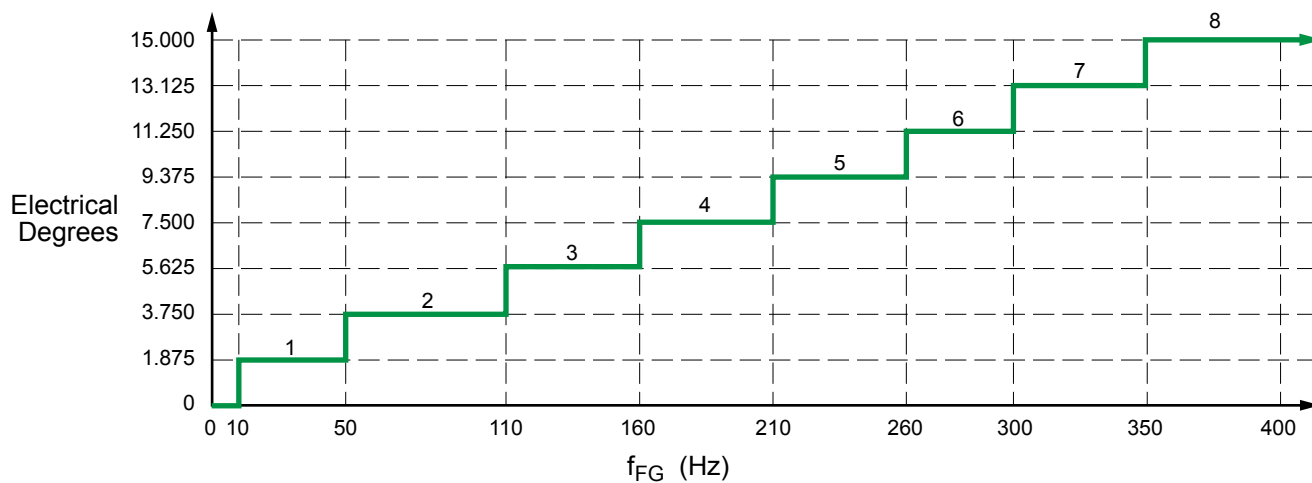
Figure 3: Dynamic Phase Advance

APPLICATION INFORMATION

Layout Notes

A typical layout is illustrated in Figure 4. The recommended component values for this layout are provided in Table 1.

The following guidelines for printed circuit board (PCB) layout should be observed:

- Add thermal vias to exposed pad area under the LP package.

- Connect ground planes on the top and bottom surfaces of the PCB.

- Place C_{VREF} and C_{VBB} as close as practical to the A4944.

- Route the Hall input traces (to HA, HB, and HC) away from the motor output traces (OUTA, OUTB, and OUTC). If possible, use the opposite sides of the PCB. For example, route the Hall input traces on the top layer, and route the output traces on the bottom layer.

- Place R_1 and R_2 near the Hall sensor devices.

Table 1: Recommended External Components

| Symbol	Value	Note
R_1 and R_2	330 Ω	Hall bias resistors selected to allow input voltages to be in common-mode range of Hall input pins (500 mV to V_{REF} − 1 V). Maximum V_{REF} current = 10 mA. Hall bias must result in the V_{p-p} of the Hall signals being greater than 50 mV.
C_{VREF}	0.22 μF/ X5R/10 V	Ceramic capacitor required.
C_{VBB}	10 to 47 μF	For power-supply stabilization; electrolytic or ceramic capacitor can be used.
R_{FG}	20 kΩ	Optional pull-up resistor for speed feedback.
C_H	Not Installed	Not required for typical applications because the IC has an internal noise filter.
D_1	Not Installed TVS Zener	Optional, to limit maximum V_{BB} if the power supply line is subject to transients. It is recommended to clamp below 18 V (for example: Fairchild SMBJ14A).
R_{PWM}	1 kΩ	Optional. If PWMVSP is wired to a connector, R_{PWM} isolates PWMVSP from noise and from overvoltage transients.
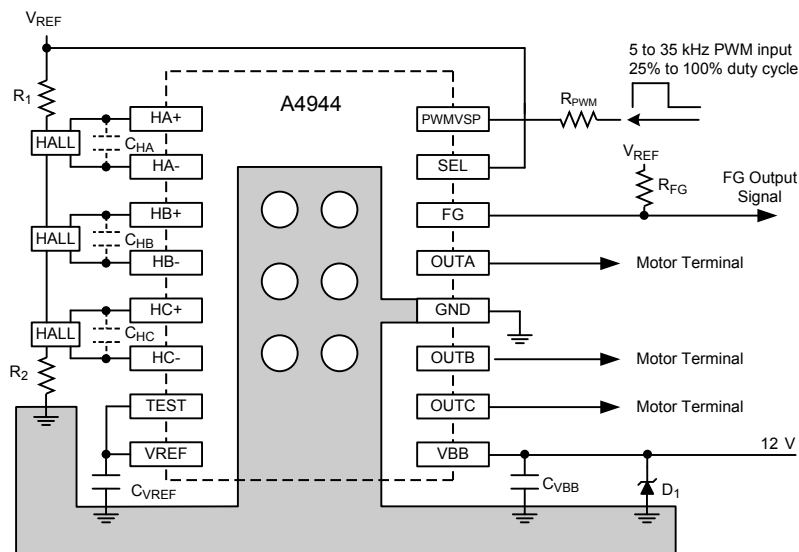
Figure 4: Typical Application Circuit

Hall Biasing

The suggested Hall element bias is a series connection, as shown in Figure 4. It is allowable to connect the bias supply in parallel, as shown in Figure 5. When connecting in parallel, it might be necessary to change the bias resistors (R1 and R2) from the recommended values shown in Table 1, in order to limit the maximum Hall element bias current to less than 10 mA.

Analog Input from System PWM

For proper operation with an external PWM speed-demand signal, the PWMVSP pin requires a frequency in the range of 5 to 35 kHz. If the system frequency is beyond this range, an external circuit can be used to translate the system PWM signal into an analog voltage that is appropriate for input to the PWMVSP pin. Use of an analog voltage input is selected by connecting the SEL pin to GND.

An example circuit is shown in Figure 6. Note:

- A filter composed of resistor R_F (2 kΩ) and capacitor C_F (1 μF) smooths the input PWM to the analog voltage used by the ADC.

- For low input PWM frequencies, it might be necessary to increase C_F.

- The resistor divider composed by R_3 (1.6 kΩ) and R_4 (10 kΩ) scales the input to 100% demand when a 100% PWM duty cycle is applied.
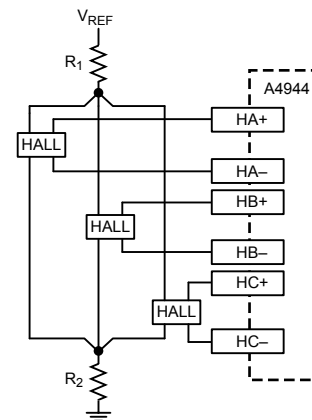

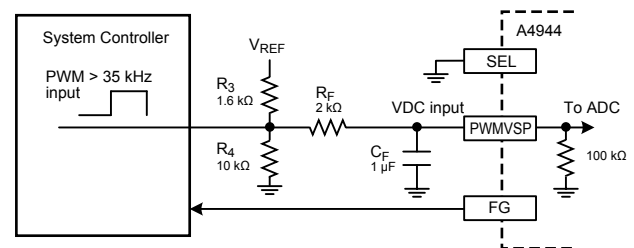**Figure 5: Alternative Parallel Circuit for Hall-Element Biasing**

Figure 6: Alternative Circuit for Providing Analog Speed-Demand Input from a High System PWM Signal

Fan System Integration

Alternative circuits for three methods of integration of the device into typical fan system applications—PWM control input, analog voltage control input, and supply voltage control—are provided in Figure 7.
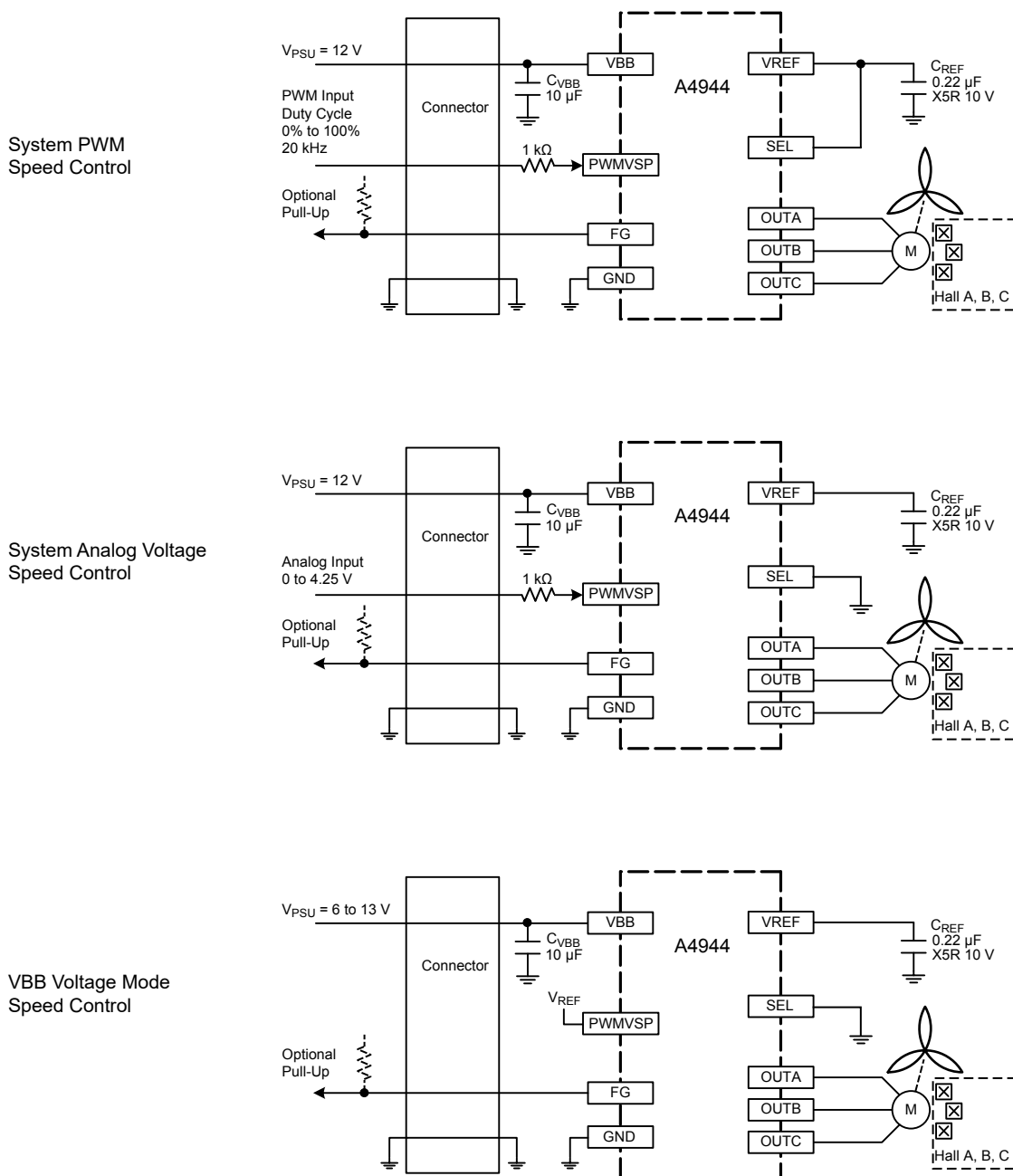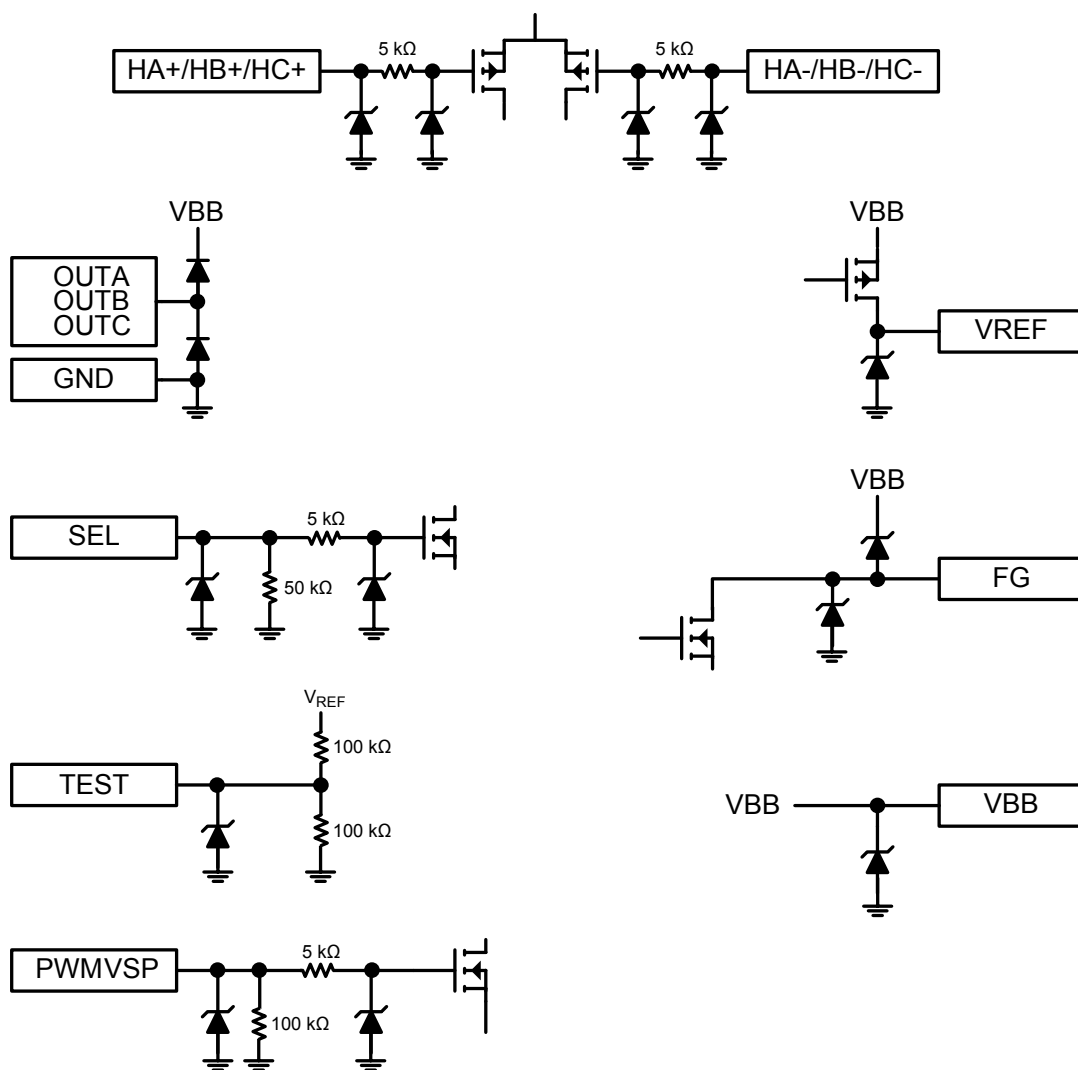
System PWM
Speed Control

System Analog Voltage
Speed Control

VBB Voltage Mode
Speed Control

Figure 7: Typical Fan System Configuration Using PWM Speed Control

PIN STRUCTURES

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
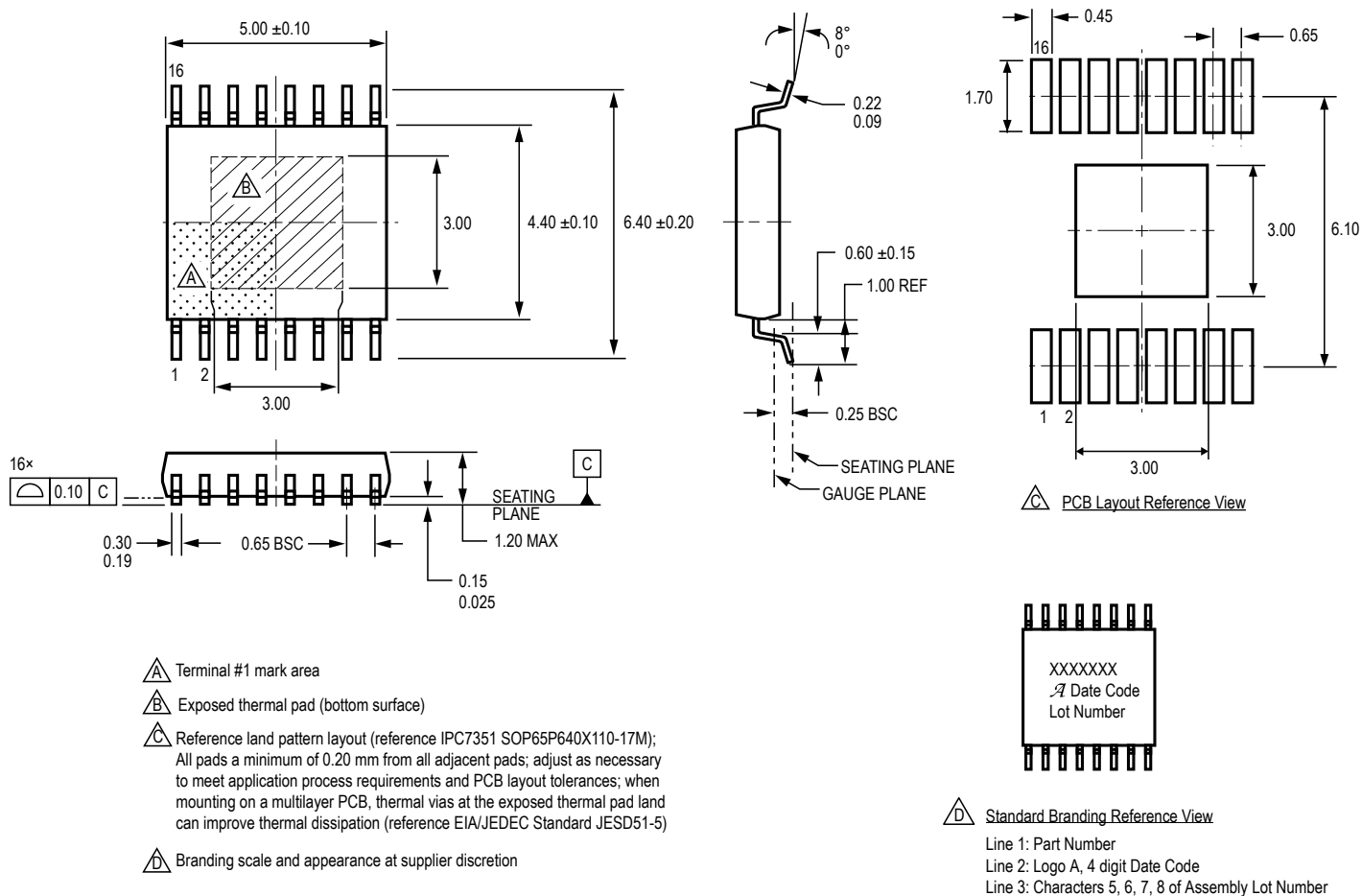Exact case and lead configuration at supplier discretion within limits shown

Ⓐ Terminal #1 mark area

Ⓑ Exposed thermal pad (bottom surface)

Ⓒ Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Ⓓ Branding scale and appearance at supplier discretion

Ⓒ PCB Layout Reference View

XXXXXXX
𝒜 Date Code
Lot Number

Ⓓ Standard Branding Reference View

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 8: Package LP, 16-Pin TSSOP with Exposed Thermal Pad

Revision History

Number	Date	Description
2	April 23, 2018	Minor editorial updates
3	July 2, 2019	Minor editorial updates
4	July 14, 2022	Updated LP package drawing (page 13); removed A4944LWTR-T package variant (page 1-3, page 14)
5	March 21, 2025	Removed limited distribution markings, made minor editorial changes, and updated source file format (all pages)

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