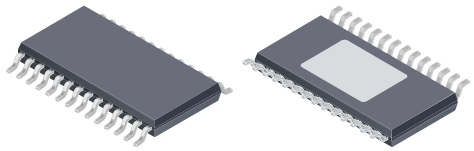
Microstepping DMOS Driver with Translator

FEATURES AND BENEFITS

- ±2.8 A, 40 V output rating
- Low $R_{DS(on)}$ outputs, 0.22 Ω source, 0.15 Ω sink typical
- Automatic current decay mode detection/selection
- 3 to 5.5 V logic supply voltage range
- Mixed, fast, and slow current decay modes
- Fault output
- Mixed decay for both rising/falling step option
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection
- Short-to-ground protection
- Short-to-VBB protection
- Shorted load protection

Package: 28-lead TSSOP (suffix LP) with exposed thermal pad



Not to scale

DESCRIPTION

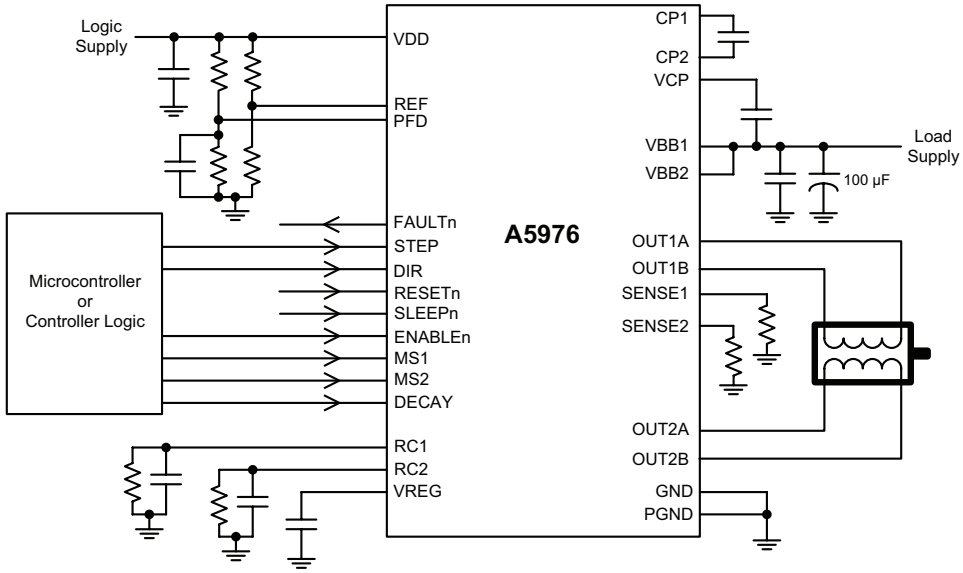
The A5976 is a complete microstepping motor driver with built-in translator. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes, with output drive capability of 40 V and ±2.8 A. The A5976 includes a fixed off-time current regulator that has the ability to operate in slow-, fast-, or mixed-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of the A5976. Simply inputting one pulse on the STEP input drives the motor one step (two logic inputs determine if it is a full-, half-, quarter-, or sixteenth-step). There are no phase sequence tables, high-frequency control lines, or complex interfaces to program. The A5976 interface is an ideal fit for applications where a complex microprocessor is unavailable or overburdened.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-up sequencing is not required.

The A5976 is supplied in a thin (<1.2 mm) 28-pin TSSOP with an exposed thermal pad (suffix LP). The package is lead (Pb) free (suffix -T), with 100% matte-tin leadframe plating.

Typical Application



SELECTION GUIDE

Part Number	Package	Packing
A5976GLPTR-T	28-pin TSSOP	4000 pieces per reel

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage	V_{BB}		40	V
Logic Supply Voltage	V_{DD}		7	V
Logic Input Voltage Range	V_{IN}	Pulsed, t_W > 30 ns	–0.3 to V_{DD} + 0.3	V
		Pulsed, t_W < 30 ns	–1 to V_{DD} + 1	V
SENSEx Voltage (DC)	V_{SENSE}		0.5	V
Reference Voltage	V_{REF}		V_{DD}	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±2.8	A
Operating Ambient Temperature	T_A	Range G	–40 to 105	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LP, on 4-layer PCB based on JEDEC standard	28	ºC/W

*Additional thermal information available on Allegro website.

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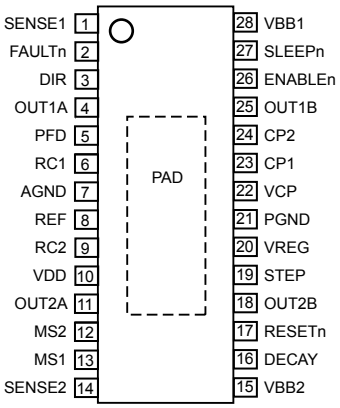
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP,
28-Pin TSSOP

Terminal List Table

Number	Name	Description
1	SENSE1	Sense resistor for bridge 1
2	FAULTn	Open-drain logic output
3	DIR	Logic input
4	OUT1A	DMOS full-bridge 1, output A
5	PFD	Analog input for mixed-decay setting
6	RC1	Analog input for fixed off-time, bridge 1
7	AGND*	Analog ground
8	REF	Gm reference input
9	RC2	Analog input for fixed off-time, bridge 2
10	VDD	Logic supply voltage
11	OUT2A	DMOS full-bridge 2, output A
12	MS2	Logic input
13	MS1	Logic input
14	SENSE2	Sense resistor for bridge 2
15	VBB2	Load supply for bridge 2
16	DECAY	Logic input
17	RESETn	Logic input
18	OUT2B	DMOS full-bridge 2, output B
19	STEP	Logic input
20	VREG	Regulator decoupling
21	PGND*	Power ground
22	VCP	Reservoir capacitor
23	CP1	Charge pump capacitor
24	CP2	Charge pump capacitor
25	OUT1B	DMOS full-bridge 1, output B
26	ENABLEn	Logic input
27	SLEEPn	Logic input
28	VBB1	Load supply for bridge 1
–	PAD*	Thermal pad

* GND, PGND, and thermal pad must be connected together externally under the device.

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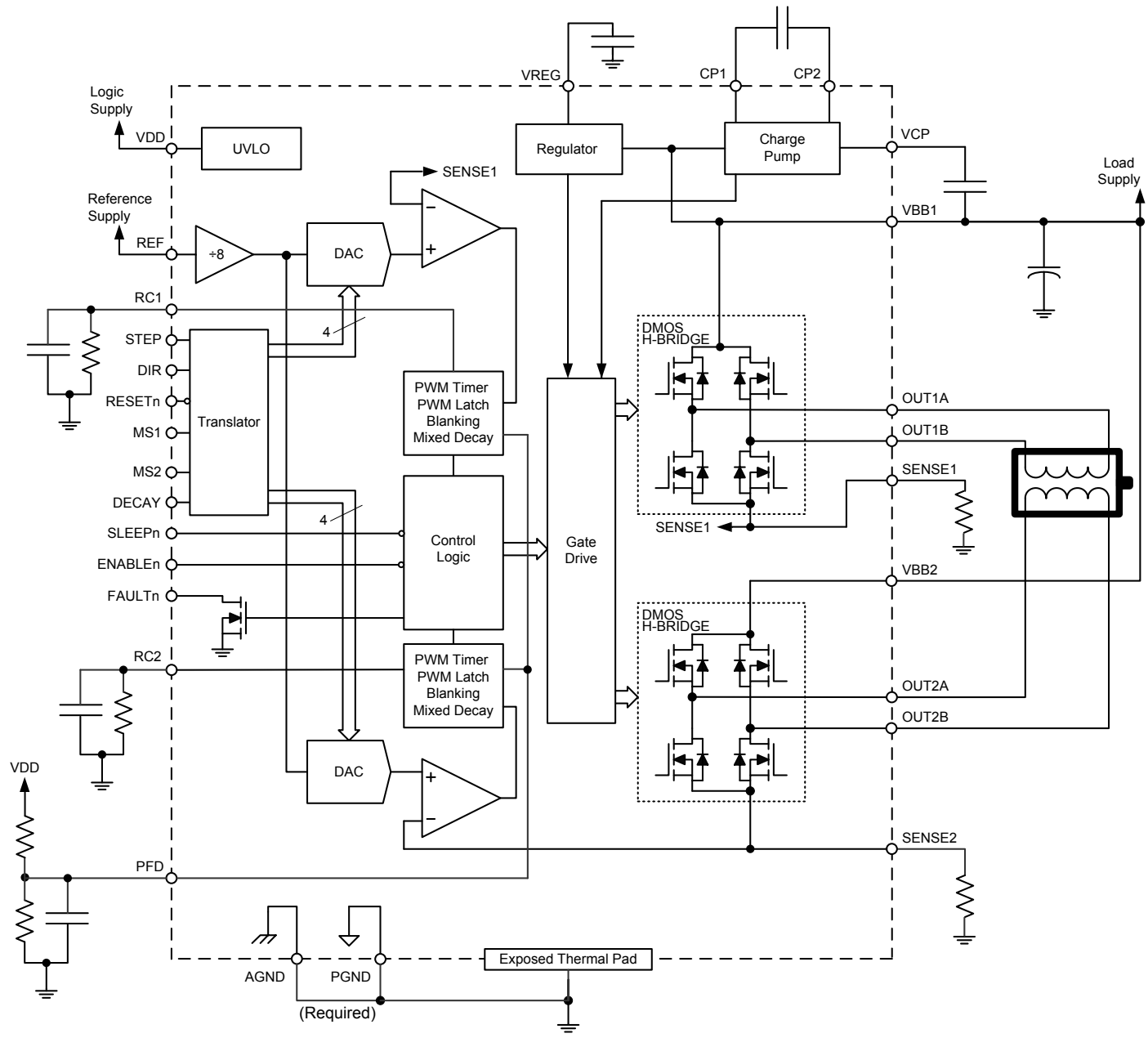
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS[1]: Valid at T_A = 25°C, V_{BB} = 40 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Load Supply Voltage Range	V_{BB}	Operating	8	–	40	V
		During sleep mode	0	–	40	V
Output Leakage Current	I_{DSS}	V_{OUT} = V_{BB}	–	<1	20	µA
		V_{OUT} = 0 V	–	<1	–20	µA
Output On-Resistance	$R_{DS(On)}$	Source driver, I_{OUT} = –2.5 A, T_J = 25°C	–	0.22	0.30	Ω
		Sink driver, I_{OUT} = 2.5 A, T_J = 25°C	–	0.15	0.24	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = –2.5 A	–	1	1.4	V
		Source diode, I_F = 2.5 A	–	1	1.4	V
VBB Supply Current	I_{BB}	f_{PWM} < 50 kHz, duty cycle = 50%	–	–	8	mA
		Operating, outputs disabled	–	–	6	mA
		Sleep mode	–	<1	20	µA
VDD Supply Current	I_{DD}	f_{PWM} < 50 kHz, duty cycle = 50%	–	–	12	mA
		Operating, outputs disabled	–	–	10	mA
		Sleep mode	–	<1	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3	–	5.5	V
Logic Input Voltage	$V_{IN(1)}$		0.7×V_{DD}	–	–	V
	$V_{IN(0)}$		–	–	0.3×V_{DD}	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 0.7×V_{DD}	–20	<1	20	µA
	$I_{IN(0)}$	V_{IN} = 0.3×V_{DD}	–20	<1	20	µA
Maximum Step Frequency[3]	f_{STEP}		500	–	–	kHz
FAULTn Output Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.5	V
Blank Time	t_{BLANK}	R_T = 56 kΩ, C_T = 680 pF	700	950	1200	ns
Fixed Off-Time	t_{OFF}	R_T = 56 kΩ, C_T = 680 pF	30	38	46	µs
Reference Input Voltage Range	V_{REFx}	Operating	0	–	V_{DD}	V
Reference Input Current	I_{REF}		–	–	±3	µA
Gain (G_m) Error[4]	E_G	V_{REF} = 2 V, phase current = 100.0%	–	–	±5	%
		V_{REF} = 2 V, phase current = 70.7%	–	–	±5	%
		V_{REF} = 2 V, phase current = 38.3%	–	–	±10	%
Crossover Dead Time	t_{DT}		100	475	800	ns
Motor Output Slew Time	t_{SR}	10% to 90% rising; 90% to 10% falling	20	–	120	ns
Protection Circuits						
VDD UVLO Threshold	$V_{UV(VBB)}$	V_{BB} rising	2.45	2.7	2.95	V
VDD UVLO Hysteresis	$V_{UV(VBB)HYS}$		50	100	–	mV
Overcurrent Protection Threshold	I_{OCPST}		3.5	–	–	A
Overcurrent Protection Blank Time	$t_{BLANK(OC)}$		–	1.5	–	µs
Thermal Shutdown Temperature	T_{JSD}		155	165	175	°C
Thermal Shutdown Hysteresis	T_{JSDHYS}		–	15	–	°C

[1] Typical data are for initial design estimations only and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[2] Negative current is defined as coming out of (sourcing from) the specified device pin.

[3] Operation at a step frequency greater than the specified minimum value is possible but not guaranteed.

[4] $E_G = ([V_{REF}/8] - V_{SENSE})/(V_{REF}/8)$.

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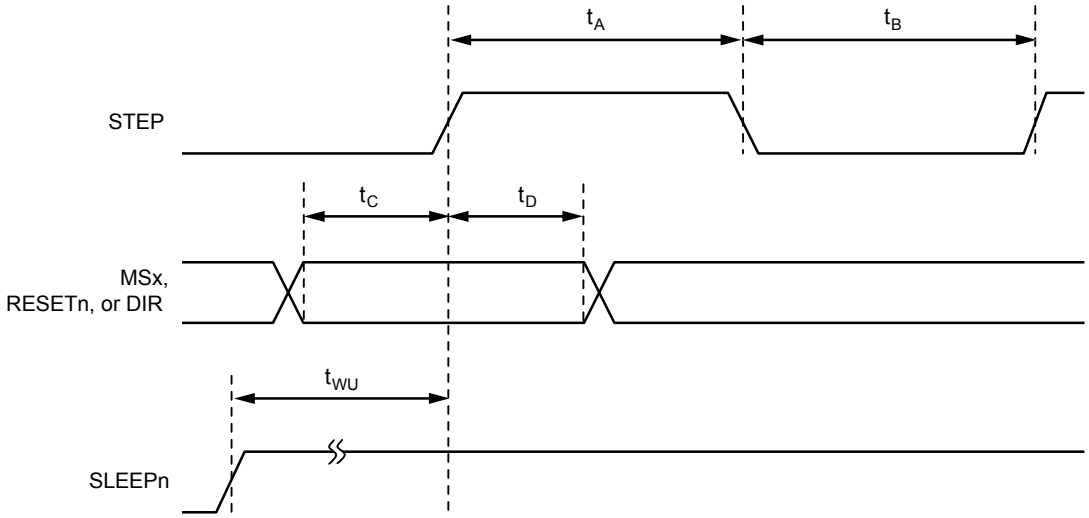

Time Duration	Symbol	Typ.	Unit
STEP Minimum, high pulse width	t_A	1	µs
STEP Minimum, low pulse width	t_B	1	µs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns
Maximum wakeup time	t_{WU}	1	ms

Figure 1: Logic Interface Timing Diagram

Table 1: Microstep Resolution Truth Table

MS2	MS1	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
L	H	Half Step	1-2 Phase
H	L	Quarter Step	W1-2 Phase
H	H	Sixteenth Step	4W1-2 Phase

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FUNCTIONAL DESCRIPTION

Device Operation

The A5976 is a complete microstepping motor driver with built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes. The current in each of the two output full-bridges, all N-channel DMOS, is regulated with fixed off-time pulse-width modulated (PWM) control circuitry. The full-bridge current at each step is set by the value of an external current-sense resistor (R_S), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-up, or reset, the translator sets the DACs and phase current polarity to the initial home state (see figures for home-state conditions), and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level (see Table 2 for the current level sequence and current polarity). The microstep resolution is set by inputs MS1 and MS2 as shown in Table 1. If the new DAC output level is lower than the previous level, the decay mode for that full-bridge will be set by the PFD input (fast, slow, or mixed decay). If the new DAC level is higher or equal to the previous level, then the decay mode for that full-bridge will be slow decay. This automatic current-decay selection will improve microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

The DECAY input determines how the decay mode is selected when stepping the motor. If the DECAY input is high, when stepping, if the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for that full-bridge is set to slow. If the DECAY input is high and the new output levels of the DACs are lower than their previous output levels, then the decay mode for that full-bridge is set by the state of the PFD input (see PFD input description). This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back-EMF of the motor. If the DECAY input is low, then the decay mode is always set by the state of the PFD input (see PFD input description). See Figure 6 on page 13 and Figure 7 on page 14 for decay mode detail.

Internal PWM Current Control

Each full-bridge is controlled by a fixed off-time PWM current-control circuit that limits the load current to an appropriate level (I_{TRIP}). Initially, a diagonal pair of source and sink DMOS outputs are enabled, and current flows through the motor winding and the current-sense resistor, R_S. When the voltage across R_S rises to the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source driver (in slow-decay mode) or the sink and source drivers (in fast- or mixed-decay mode).

The maximum level of current limiting is set by the selection of R_S and the voltage at the VREF input with a transconductance function approximated by:

$$I_{TRIP}max = V_{REF} / (8 \times R_S)$$

The DAC output reduces the VREF output to the current-sense comparator in precise steps (see Table 2 for % I_{TRIP}max at each step).

$$I_{TRIP} = (\%\, I_{TRIP}max / 100) \times I_{TRIP}max$$

It is critical to ensure that the maximum rating on the SENSE terminal is not exceeded (0.5 V). For full-step mode, V_{REF} can be applied up to the maximum rating of V_{DD}, because the peak sense value is $0.707 \times V_{REF} / 8$. In all other modes, V_{REF} should not exceed 4 V.

Fixed Off-Time

The internal PWM current-control circuitry uses a one-shot to control the time that the drivers remain off. The one-shot off-time, t_{OFF}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected between the RC timing terminal and ground. The off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ is approximated by:

$$t_{OFF} = R_T \times C_T$$

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RC Blanking

In addition to the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false overcurrent detection due to reverse-recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. The blank time, t_{BLANK}, can be approximated by:

$$t_{BLANK} = 1400 \times C_T$$

Step Input (STEP)

A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS1 and MS2 (see Table 1).

Microstep Select (MS1 and MS2)

Input terminals MS1 and MS2 select the microstepping format per Table 1. Changes to these inputs do not take effect until the STEP command.

Direction Input (DIR)

The state of the DIR input will determine the direction of rotation of the motor.

DECAY Input

DECAY is a logic input that determines how the decay mode is selected when stepping the motor. If the DECAY input is high and a step is made such that new output levels of the DACs are higher than or equal to their levels during the previous step, then the decay mode for that full-bridge is set to slow. If the DECAY input is high and a step is made such that new output levels of the DACs are lower than their levels during the previous step, then the decay mode for that full-bridge is determined by the PFD input (see PFD input description). If the DECAY input is low, then the decay mode is always determined by the PFD input (see PFD input description).

Percent Fast-Decay Input (PFD)

Slow-, fast-, or mixed-decay is selected according to the voltage level at the PFD input, for control steps when the output current decay is user-selectable (see DECAY Input section). If the voltage at the PFD input is greater than $0.6 \times V_{DD}$, then slow-decay is selected. If the voltage on the PFD input is less than $0.21 \times V_{DD}$, then fast-decay is selected. Mixed-decay is selected when the voltage on the PFD input is between these two levels. This terminal should be decoupled with a 0.1 µF capacitor.

Mixed-Decay Operation

If the voltage on the PFD input is between $0.6 \times V_{DD}$ and $0.21 \times V_{DD}$, the bridge will operate in mixed-decay mode for control steps when the output current decay is user-selectable (see DECAY Input section). As the trip point is reached, the bridge will go into fast-decay mode until the voltage on the RC terminal decays to the voltage applied to the PFD terminal. The time the bridge remains in fast decay is approximated by:

$$t_{FD} = R_T \times C_T \times I_n \, (0.6 \times V_{DD} / V_{PFD})$$

After this fast-decay portion, t_{FD}, the bridge will switch to slow-decay mode for the remainder of the fixed off-time period.

Reset Input (RESETn)

The RESETn input (active low) sets the translator to a predefined home state (see figures for home state conditions) and turns off all of the DMOS outputs. All STEP inputs are ignored until the RESETn input goes high.

Fault Output (FAULTn)

The FAULTn terminal is an open-drain output which is pulled low when an OCP condition exists. An OCP is latched until the device is reset via the RESETn terminal or the voltage on VBB is cycled.

Synchronous Rectification

When a PWM off-cycle is triggered by an internal current control, load current will recirculate according to the decay mode selected by the control logic. The A5976 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay and effectively short out the body diodes with the low $R_{DS(ON)}$ driver. This will reduce power dissipation significantly and eliminate the need for external Schottky diodes for most applications. Reversal of the current in the motor winding is prevented when using this mode by turning off synchronous rectification if the current in the winding decays to zero.

Enable Input (ENABLEn)

This active-low input enables all of the DMOS outputs. When logic-high, the outputs are disabled. Inputs to the translator (STEP, DIR, MS1, MS2) are all active independent of the ENABLEn input state.

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Sleep Mode (SLEEPn)

This active-low input is used to minimize power consumption when the device is not in use. Sleep mode disables much of the internal circuitry, including the output DMOS, regulator, and charge pump. A logic-high allows normal operation and a rising edge on this input resets the translator to the home position. When coming out of sleep mode, 1 ms is required before issuing a STEP command, to allow the charge pump to stabilize.

Charge Pump (CP1 and CP2)

The charge pump is used to generate a gate supply greater than V_{BB} to drive the source-side DMOS gates. A 0.22 µF ceramic capacitor is required between CP1 and CP2, and a 0.22 µF ceramic capacitor is required between VCP and VBB. VCP is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

VREG

This internally generated voltage is used to operate the sink-side DMOS gates. The VREG terminal should be decoupled with a 0.22 µF capacitor to ground. VREG is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

Shutdown

In the event of a fault (excessive junction temperature, or low voltage on VCP or VREG), the outputs of the device are disabled until the fault condition is removed. At power-up, and in the event of low V_{DD}, the undervoltage lockout (UVLO) circuit disables the drivers and resets the translator to the home position.

Overcurrent Protection (OCP)

If any FET's current exceeds I_{OCP} for longer than the blank time, all FETs are disabled and remain latched off until the device is reset via the RESETn input or the voltage on VBB is cycled. The FAULTn output is pulled low when an overcurrent condition exists. R_{SENSE} is not required for low-side OCP to function and the OCP threshold is independent of the R_{SENSE} value.

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PHASE CURRENT DIAGRAMS

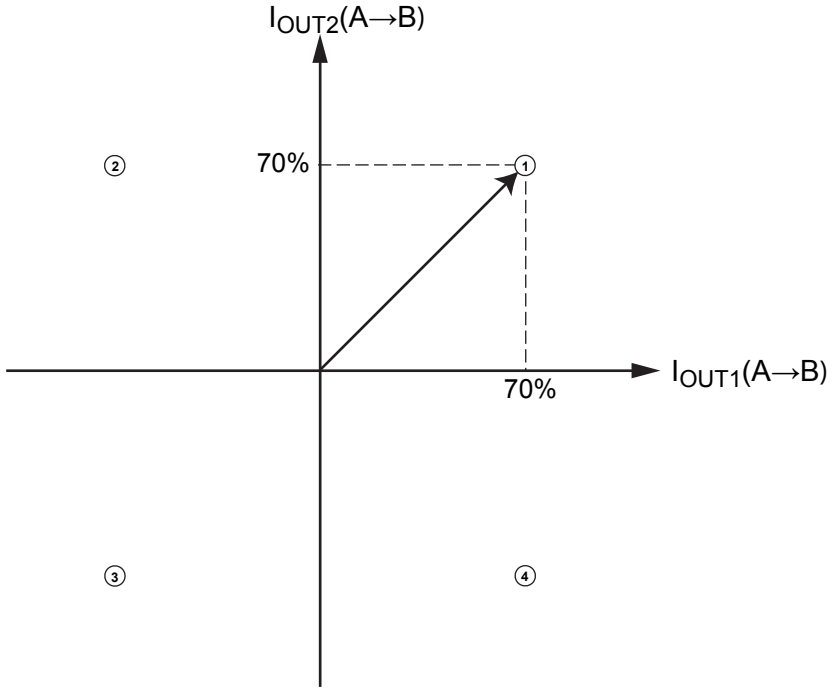

Figure 2: Full Step
MS2 = L, MS1 = L, DIR = H. See Table 2 for step number detail.

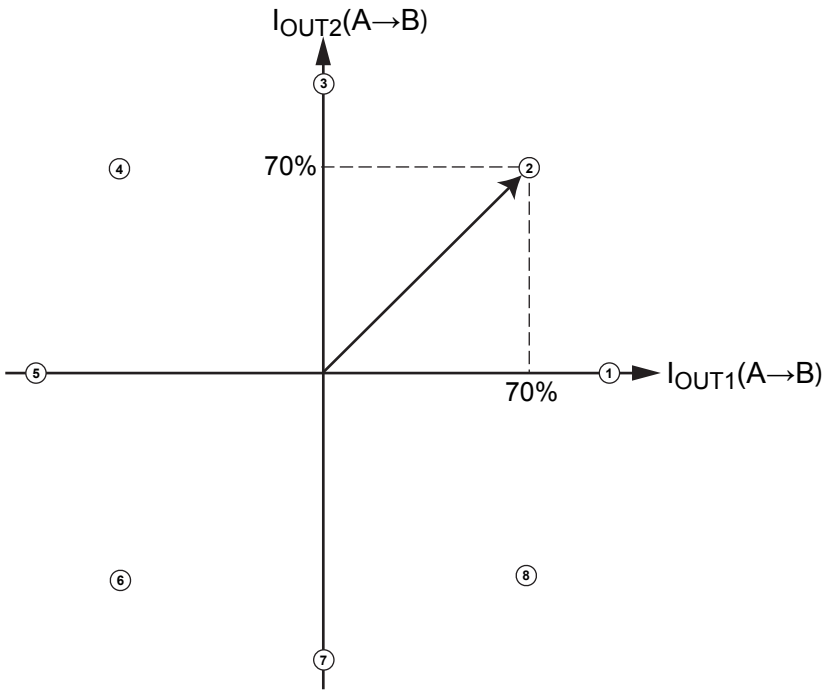

Figure 3: Half Step
MS2 = L, MS1 = H, DIR = H. See Table 2 for step number detail.

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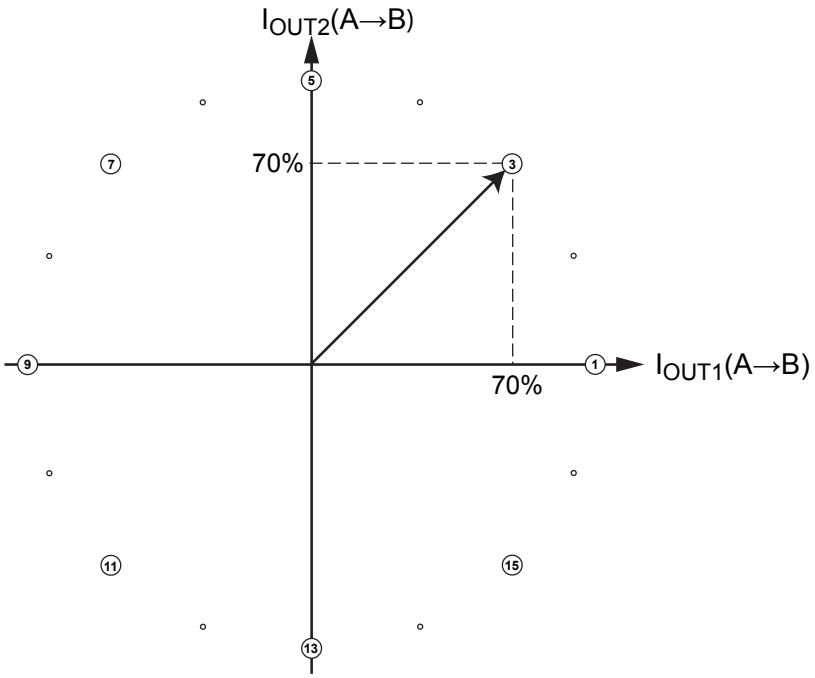

Figure 4: Quarter Step
MS2 = H, MS1 = L, DIR = H. See Table 2 for step number detail.

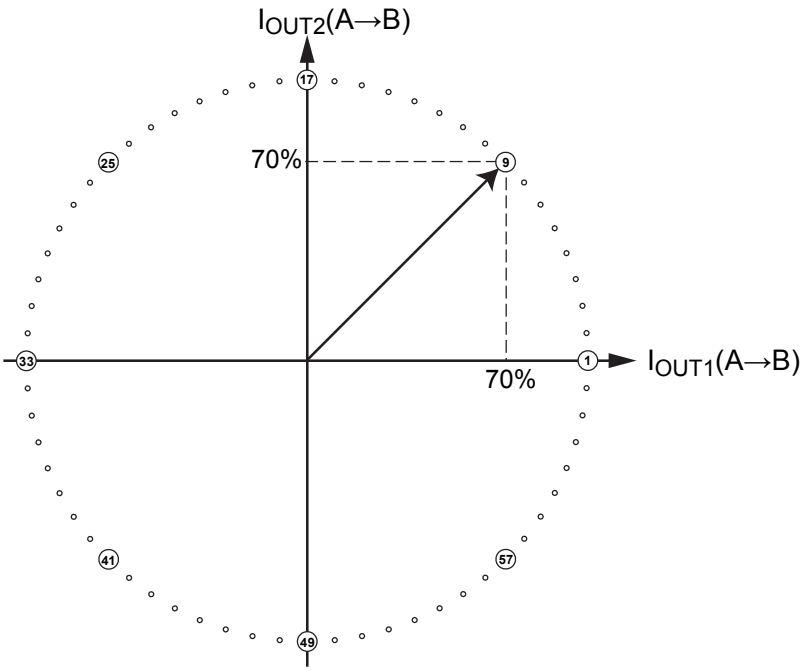

Figure 5: Sixteenth Step
MS2 = H, MS1 = H, DIR = H. See Table 2 for step number detail.

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Table 2: Step Sequencing Settings

Home microstep position at Step Angle 45º, DIR = H, 360° = 4 full steps

Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (º)	Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (º)
	1	1	1	100.0	0.0	0.0		5	9	33	-100.0	0.0	180.0
			2	99.5	9.8	5.6				34	-99.5	-9.8	185.6
			3	98.1	19.5	11.3				35	-98.1	-19.5	191.3
			4	95.7	29.0	16.9				36	-95.7	-29.0	196.9
		2	5	92.4	38.3	22.5			10	37	-92.4	-38.3	202.5
			6	88.2	47.1	28.1				38	-88.2	-47.1	208.1
			7	83.1	55.6	33.8				39	-83.1	-55.6	213.8
			8	77.3	63.4	39.4				40	-77.3	-63.4	219.4
1*	**2***	**3***	**9***	**70.7***	**70.7***	**45.0***	3	6	11	41	-70.7	-70.7	225.0
			10	63.4	77.3	50.6				42	-63.4	-77.3	230.6
			11	55.6	83.1	56.3				43	-55.6	-83.1	236.3
			12	47.1	88.2	61.9				44	-47.1	-88.2	241.9
		4	13	38.3	92.4	67.5			12	45	-38.3	-92.4	247.5
			14	29.0	95.7	73.1				46	-29.0	-95.7	253.1
			15	19.5	98.1	78.8				47	-19.5	-98.1	258.8
			16	9.8	99.5	84.4				48	-9.8	-99.5	264.4
	3	5	17	0.0	100.0	90.0		7	13	49	0.0	-100.0	270.0
			18	-9.8	99.5	95.6				50	9.8	-99.5	275.6
			19	-19.5	98.1	101.3				51	19.5	-98.1	281.3
			20	-29.0	95.7	106.9				52	29.0	-95.7	286.9
		6	21	-38.3	92.4	112.5			14	53	38.3	-92.4	292.5
			22	-47.1	88.2	118.1				54	47.1	-88.2	298.1
			23	-55.6	83.1	123.8				55	55.6	-83.1	303.8
			24	-63.4	77.3	129.4				56	63.4	-77.3	309.4
2	4	7	25	-70.7	70.7	135.0	4	8	15	57	70.7	-70.7	315.0
			26	-77.3	63.4	140.6				58	77.3	-63.4	320.6
			27	-83.1	55.6	146.3				59	83.1	-55.6	326.3
			28	-88.2	47.1	151.9				60	88.2	-47.1	331.9
		8	29	-92.4	38.3	157.5			16	61	92.4	-38.3	337.5
			30	-95.7	29.0	163.1				62	95.7	-29.0	343.1
			31	-98.1	19.5	168.8				63	98.1	-19.5	348.8
			32	-99.5	9.8	174.4				64	99.5	-9.8	354.4

* Home state

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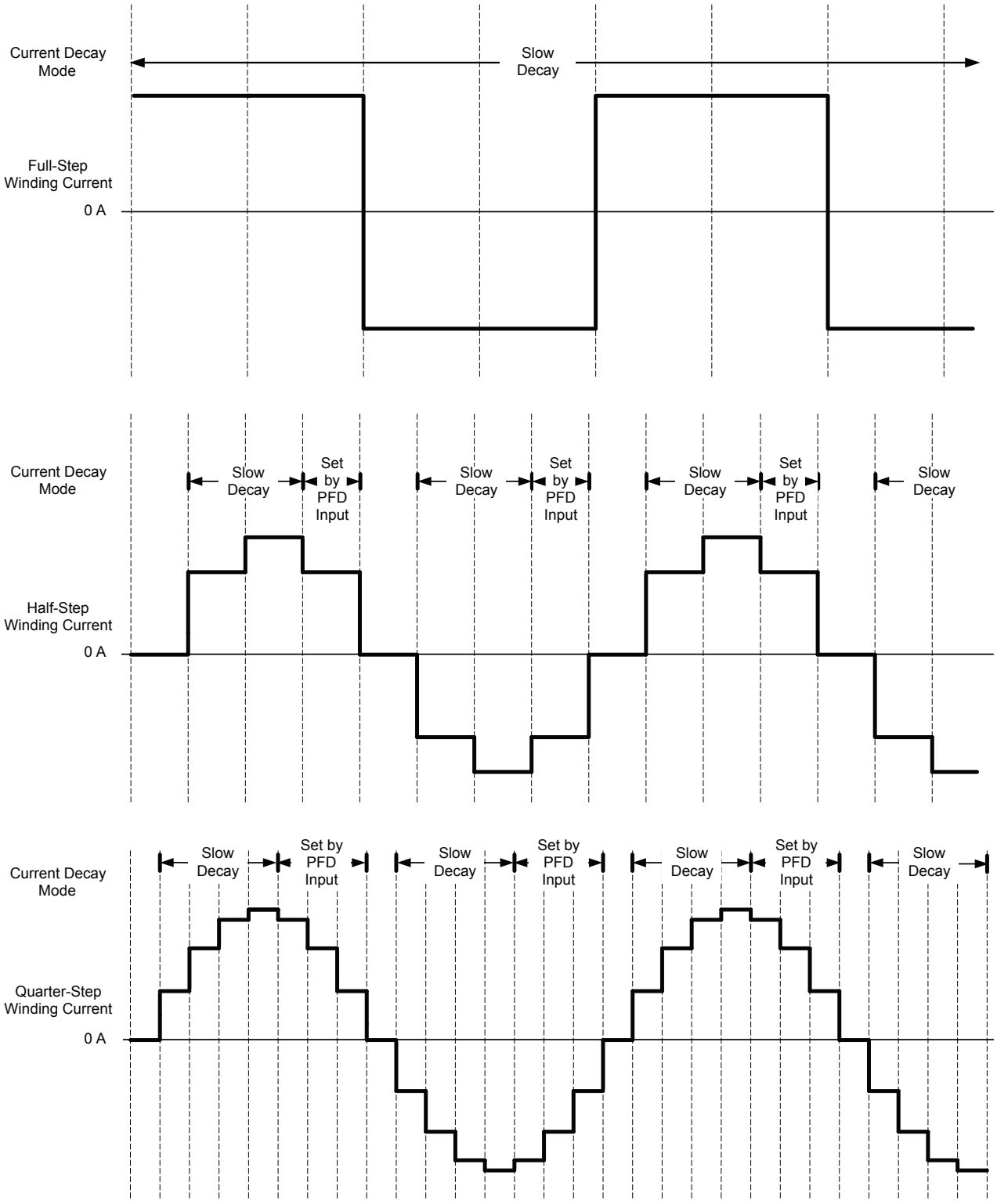

Figure 6: DECAY = H, Automatic Decay Mode

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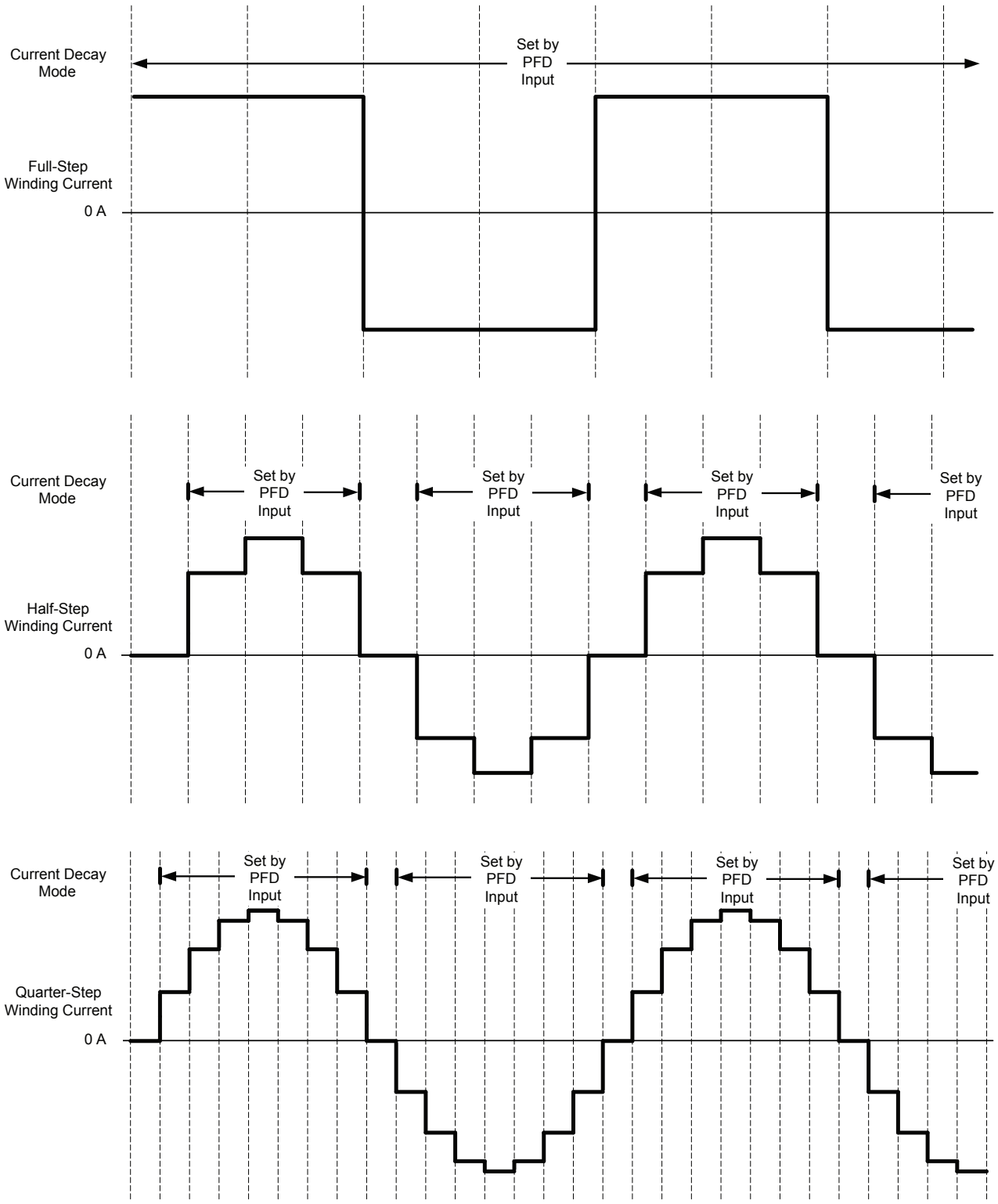

Figure 7: DECAY = L, PFD-Controlled Decay Mode

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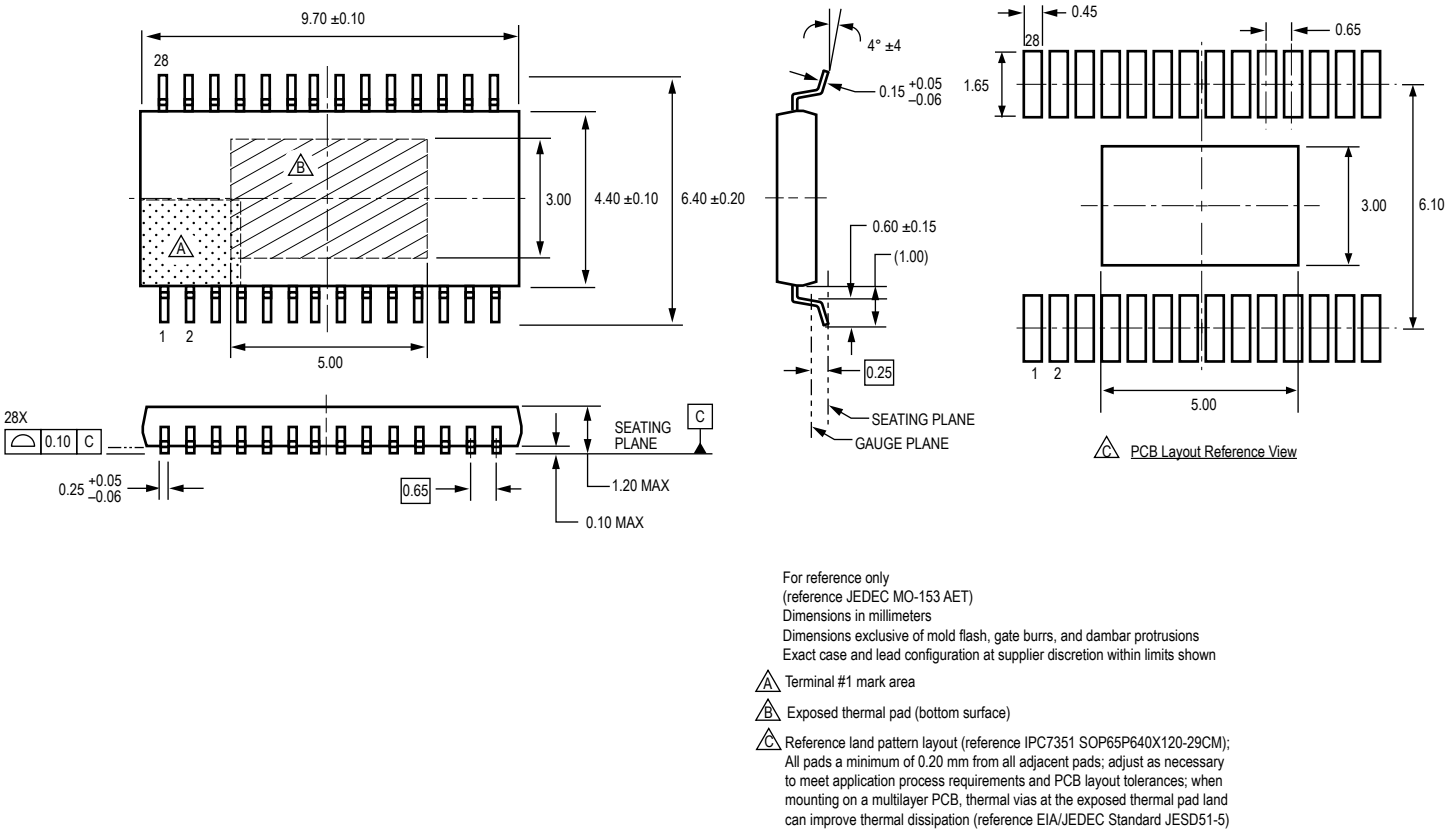
PACKAGE OUTLINE DRAWING



For reference only
(reference JEDEC MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 8: LP Package, 28-pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	December 21, 2015	Initial release
1	January 21, 2016	Corrected formula on page 7
2	May 31, 2016	Corrected setup and hold time units on page 6
3	June 12, 2020	Minor editorial updates

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