Fully Integrated PMIC for Safety-Related Systems with Buck-Boost PreRegulator, 5× Linear Regulators, and SPI

FEATURES AND BENEFITS

- ASIL-Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Automotive AEC-Q100 Grade 0 qualified
- Wide input range: 3.2 to 36 V V_{IN} operating, 40 V V_{IN} maximum
- 2.2 MHz synchronous buck-boost preregulator (VREG: 5.35 V) with internal compensation
- Five internal linear regulators with fold-back short-circuit protection
  - □ VUC: 3.3 V or 5 V (selectable by a pin) regulator for microcontroller
  - □ VLDOA: 5 V (or 3.3 V factory option) general-purpose low-dropout (LDO) regulator
  - □ VLDOB: 5 V or 3.3 V (selectable by a pin) always-on LDO regulator
  - □ VLDOP1 and VLDOP2: Two programmed (5 V or 3.3 V) and enabled via serial-port-interface (SPI) LDO regulators with short-to-battery protection for remote sensors
- Pulse-width watchdog (PWWD), window watchdog

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APPLICATIONS

Provides system power for microcontroller/DSP, CAN, sensors, etc. in automotive-control modules, such as:

- Power steering
- Braking
- Transmission
- Onboard charger (OBC)/ DC-to-DC/inverter
- Other automotive applications

A2 SiL ISO 26262 ASIL Compliant

DESCRIPTION

The A81411 is a power-management integrated circuit (IC) that integrates a buck-boost preregulator, five LDOs, and many safety features. The preregulator uses a buck-boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the preregulator supplies a 600 mA linear regulator that can output 5 V or 3.3 V (VUC), a 5 V (or 3.3 V factory option) 200 mA linear regulator (VLDOA), and two 5 V or 3.3 V/150 mA linear regulators (VLDOP1 and VLDOP2) that are protected when shorted to battery. Designed to supply power for microprocessors, sensors, and CAN transceivers, the A81411 is ideal for under-the-hood applications. A fifth always-on LDO (VLDOB) can supply 50 mA at either 5 V or 3.3 V.

Two automotive-battery-rated enable inputs are available on the A81411. An additional logic-level enable is also available for control via a microcontroller unit (MCU).

Diagnostic outputs from the A81411 include watchdog fault (WD_Fn), power-on reset (NPOR), fault flag (FFn) to alert the microprocessor that a fault has occurred, and gate-driver enable (POE)

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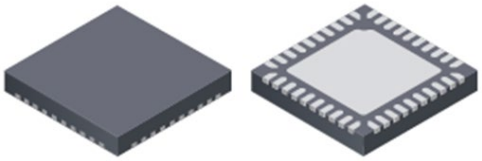
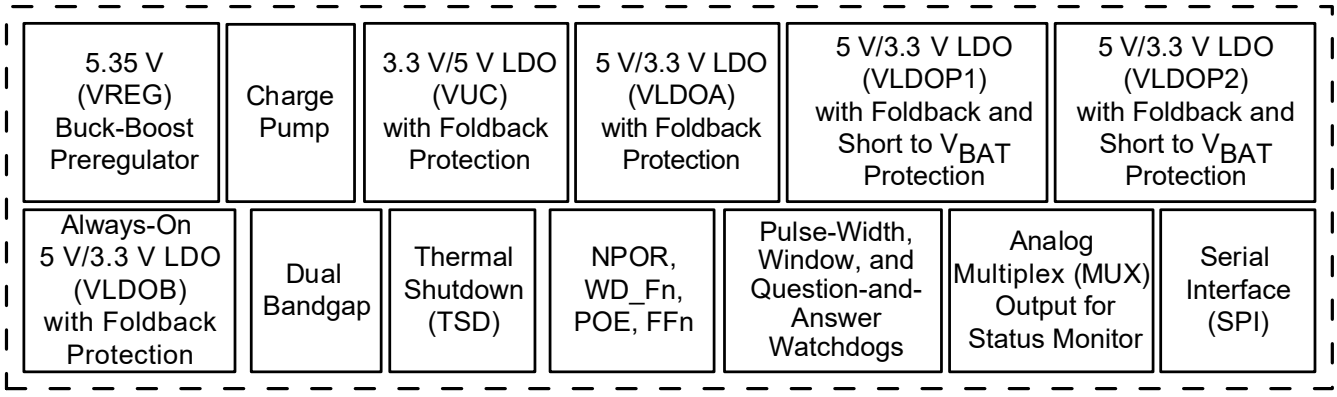
PACKAGE



40-pin QFN (suffix EV) 6 mm × 6 mm
Not to scale



Simplified Functional Block Diagram

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FEATURES AND BENEFITS

(WWD), and question-and-answer watchdog (QAWD)
- Control and diagnostic reporting through secure SPI
  - □ 16-bit data transfers
  - □ 5-bit cyclic redundancy check (CRC)
  - □ 3-bit frame counter
  - □ 5-bit request register identification (ID)
  - □ Read-back register
  - □ Chip ID
- Two high-voltage enable inputs (ENBAT and ENCAN)
- Frequency dithering and controlled slew rate help reduce electromagnetic interference (EMI) and improve electromagnetic compatibility (EMC)
- Undervoltage protection for all output rails
- Thermal shutdown protection

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DESCRIPTION

The microprocessor can read fault registers through SPI.

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the A81411.

The A81411 contains three types of watchdog timers: pulse-width watchdog (PWWD), window watchdog (WWD), and question-and-answer watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

The A81411 is supplied in a low-profile 40-pin quad-flat no-lead (QFN) package (suffix EV) with exposed power pad and wettable flanks.

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SPECIFICATIONS

SELECTION GUIDE

Part Number	VLDOA Output Voltage	Package	Packing [1]	Lead Frame
A81411KEVGTR	5 V	40-pin QFN with thermal pad	1500 pieces per reel	100% matte tin
A81411KEVGTR-1	3.3 V			

[1] For additional packing options, contact Allegro.

ABSOLUTE MAXIMUM RATINGS [2][3]

Characteristic	Symbol	Notes	Rating	Unit
VIN, VINP	AMR_VIN, AMR_VINP		−0.3 to 40	V
VREG, VREGLDO, VUCIN	AMR_VREG, AMR_VREGLDO, AMR_VUCIN		−0.3 to 40	V
ENBAT, ENCAN	AMR_ENBAT, AMR_ENCAN		−0.3 to 40	V
	AMR_I_ENBAT, AMR_I_ENCAN		±75	mA
VUCSEL, VLDOBSEL	AMR_VUCSEL, AMR_VLDOBSEL		−0.3 to 40	V
LX1	AMR_LX1		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
LX2	AMR_LX2		−0.3 to V_{VREG} + 0.3	V
		t < 250 ns	−1.5	V
CP1	AMR_CP1		– 0.3 to V_{VREG} + 0.3	V
CP2	AMR_CP2		V_{VREG} – 0.3 to 40	V
VCP	AMR_VCP		V_{VREG} – 0.6 to 40	V
BOOT1	AMR_BOOT1		V_{LX1} – 0.3 to V_{LX1} + 7	V
BOOT2	AMR_BOOT2		V_{LX2} – 0.3 to V_{LX2} + 7	V
VLDOP1, VLDOP2	AMR_VLDOPx		−0.3 to 40	V
PGND	AMR_PGND		−0.3 to 0.3	V
All Other Pins			−0.3 to 7	V
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only. Functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] All absolute maximum ratings (AMRs) shall be measured with respect to the GND pin.

ESD CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min	Typ.	Max.	Unit
ESD HBM Robustness	$V_{ESD,HBM}$	ESD susceptibility to GND on all pins	–2	–	2	kV
ESD CDM Robustness	$V_{ESD,CDM}$	ESD susceptibility to GND on all pins	–500	–	500	V
	$V_{ESD,CDM,CORNER}$	ESD susceptibility to GND on corner pins	–750	–	750	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN, 40 pin (EV) package, 4-layer printed circuit board (PCB) based on JEDEC standard	27	°C/W

[4] Additional thermal information is available on the Allegro website.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

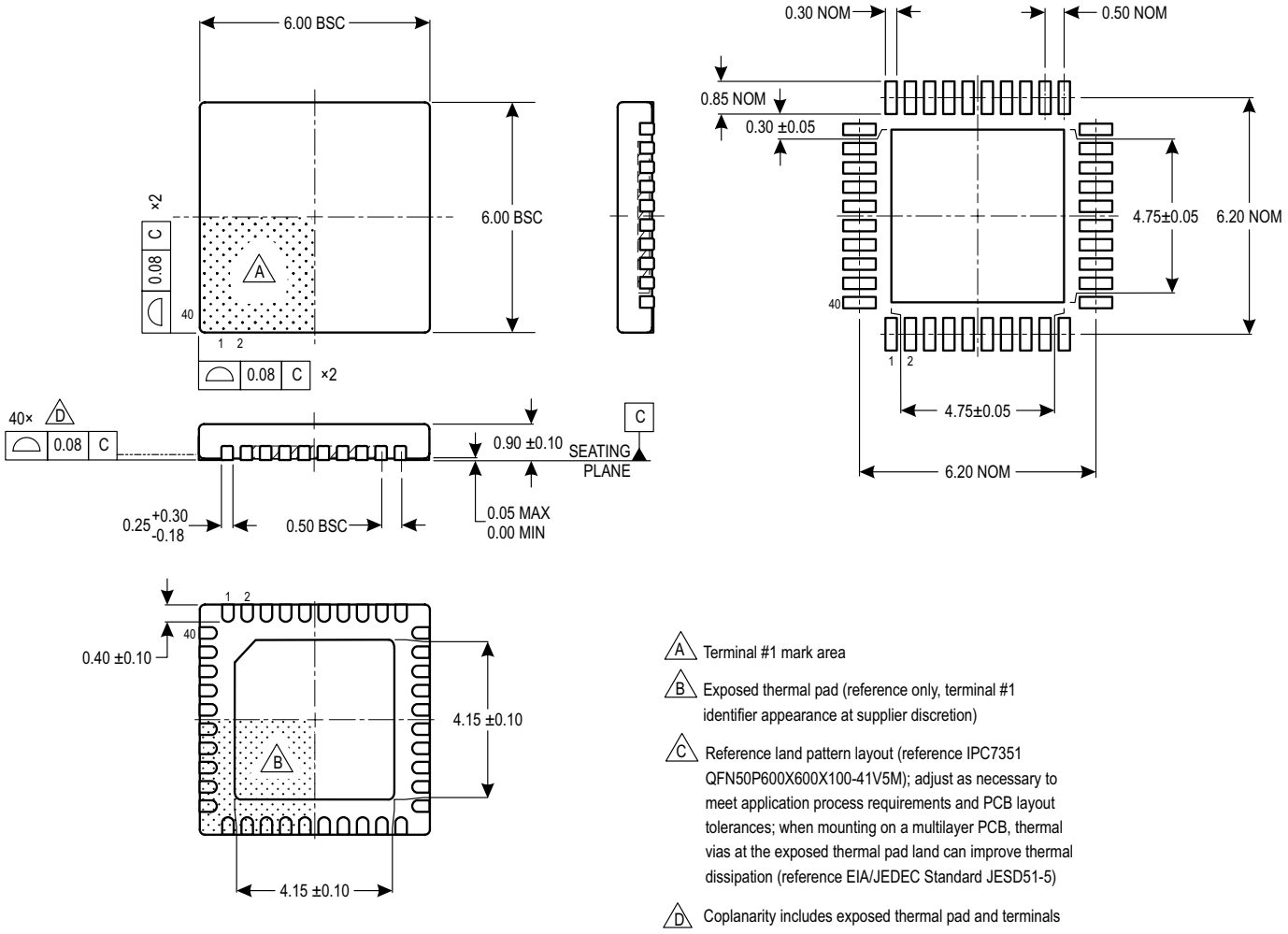

Figure 1: EV Package, 40-pin QFN

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Revision History

Number	Date	Description
–	January 13, 2025	Initial release
1	January 21, 2025	Removed confidentiality watermark (all pages), Updated Application and Features and Benefits sections (page 1), added ESD Characteristics table (page 3)
2	January 31, 2025	Updated ASIL logo (page 1), updated Electrical Characteristics table (page 7, page 12)
3	February 10, 2025	Created short-form datasheet variant of long-form datasheet
4	July 2, 2025	Reference long-form (complete) datasheet for revision description

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