A81412

Fully Integrated PMIC for Safety-Related Systems with Buck-Boost Preregulator, 6× Linear Regulators, and SPI

FEATURES AND BENEFITS

- ASIL-Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Automotive AEC-Q100 Grade 0 qualified
- VIN input range: 3.2 to 36 V operating, 40 V maximum
- 2.2 MHz synchronous buck-boost preregulator (VREG: 5.35 V) with internal compensation
- Six internal linear regulators with fold-back short-circuit protection
  - VUC: 3.3 V or 5 V (selectable by part number) regulator for microcontroller
  - VLDOA: 5 V (selectable by part number) general-purpose low-dropout (LDO) regulator, normally used to supply one or two CAN transceivers
  - VLDOB: 5 V always-on or 3.3 V / 5 V SPI-controlled (selectable by a pin) LDO regulator
  - VLDOC: 5 V, 1% accuracy LDO regulator for microcontroller unit (MCU) A/D input
  - VLDOP1 and VLDOP2: Two programmed (5 V or 3.3 V) and enabled via serial-port-interface (SPI) LDO regulators with short-to-battery protection for remote sensors
- Low-power battery-disconnect switch (VSW)

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APPLICATIONS

Provides system power for microcontroller/DSP, CAN, sensors, etc. in automotive-control modules, such as:

- Power steering
- Onboard charger (OBC)/ DC-to-DC/inverter
- High-voltage inverter

A2 SiL ISO 26262 ASIL Compliant

DESCRIPTION

The A81412 is a power management IC that integrates a buck boost pre-regulator, six LDOs, and many safety features. The pre-regulator uses a buck-boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the pre-regulator supplies a 600 mA linear regulator which can deliver 5 V or 3.3 V (VUC), a 5 V (or 3.3 V factory option) 200 mA linear regulator (VLDOA), a 5 V 100 mA linear regulator (VLDOC), and two 5 V or 3.3 V or tracking 160 mA linear regulators (VLDOP1 and VLDOP2) that are protected when shorted to battery. Designed to supply power for microprocessors, sensors, and CAN transceivers, the A81412 is ideal for under-the-hood applications.

A sixth LDO (VLDOB) can be configured to be always-on at 5 V with a sleep/active current capability of 50 mA, or a 3.3 V / 5 V LDO programed and enabled via SPI.

Two automotive-battery-rated enable inputs are available on the A81412. An additional logic-level enable is also available for control via an MCU.

Diagnostic outputs from the A81412 include a power-on reset (RESETn), a fault flag (FFn) to alert the microprocessor that a

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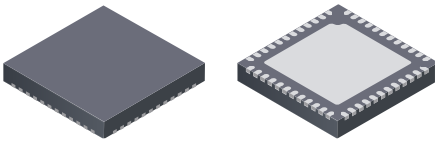
PACKAGE



48-pin QFN (suffix EV) 7 mm × 7 mm with exposed pad and wettable flank
Not to scale

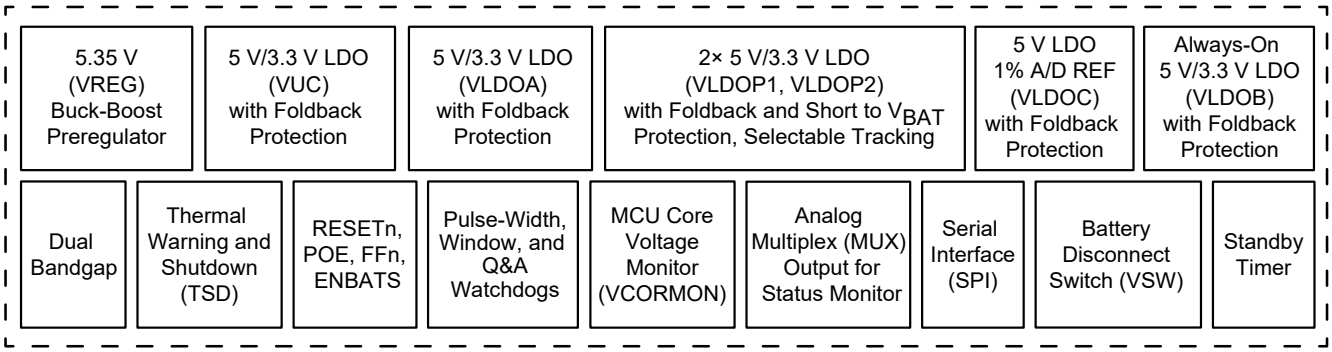


Figure 1: A81412 Simplified Block Diagram

FEATURES AND BENEFITS (continued)

- Standby timer with wake-up feature
- Pulse-width watchdog (PWWD), window watchdog (WWD), and question-and-answer watchdog (QAWD)
- Control and diagnostic reporting through secure SPI
- Two high-voltage enable inputs (ENBAT and ENCAN)
- PWM frequency dithering and LX1/LX2 controlled slew rate help reduce electromagnetic interference (EMI) and improve electromagnetic compatibility (EMC)
- Undervoltage and overvoltage protection for all outputs
- Thermal warning and shutdown protection

DESCRIPTION (continued)

fault has occurred, and a gate driver enable (POE). The microprocessor can read fault registers through SPI.

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the A81412.

The A81412 contains three types of watchdog timers: pulse-width watchdog (PWWD), window watchdog (WWD), and Q&A watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

A voltage monitor function (VCORMON) is available to verify the voltage of an external DC-DC regulator.

A standby timer is also available when the device is off and the battery line is applied. It is configurable and readable by SPI after the first power-up in normal mode and it allows also to wake up when the timer expires.

The A81412 is supplied in a low profile 48-pin QFN package with exposed power pad and wettable flanks.

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SELECTION GUIDE

Part Number	V_{VUC} (V)	V_{VLDOA} (V)	Package	Packing [1]	Lead Frame
A81412KEVGTR	3.3	5	48-pin QFN with thermal pad	1000 pieces per reel	100% matte tin
A81412KEVGTR-1	3.3	3.3			
A81412KEVGTR-2	5	5			
A81412KEVGTR-3	5	3.3			

[1] For additional packing options, contact Allegro.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating [2]	Unit
VIN, VINP	V_{VIN}, V_{VINP}		−0.3 to 40	V
VLDOBSEL	$V_{VLDOBSEL}$		−0.3 to 40	V
VSW	V_{VSW}		−0.3 to V_{VIN} + 0.3	V
VREG, VUCIN	V_{VREG}, V_{VUCIN}		−0.3 to 20	V
ENBAT, ENCAN	V_{ENBAT}, V_{ENCAN}		−0.3 to 40	V
	I_{ENBAT}, I_{ENCAN}		±75	mA
VCORMON_EN	$V_{VCORMON\_EN}$		−0.3 to 20	V
VCORMON	$V_{VCORMON}$		−0.3 to 6	V
LX1	V_{LX1}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
LX2	V_{LX2}		−0.3 to V_{VREG} + 0.3	V
		t < 250 ns	−1.5	V
CP1	V_{CP1}		– 0.3 to V_{VIN} + 0.3	V
CP2	V_{CP2}		V_{VREG} – 0.3 to V_{VCP} + 0.3	V
VCP	V_{VCP}		V_{VIN} – 0.3 to V_{VIN} + 7	V
BOOT1	V_{BOOT1}		V_{LX1} – 0.3 to V_{LX1} + 7	V
BOOT2	V_{BOOT2}		V_{LX2} – 0.3 to V_{LX2} + 7	V
VLDOP1, VLDOP2	V_{VLDOP1}, V_{VLDOP2}		−1 to 40	V
		t < 1 µs	−2	V
PGND1, PGND2	V_{PGND1}, V_{PGND2}		−0.3 to 0.3	V
All other pins			−0.3 to 7	V
Junction Temperature Range	T_J		−40 to 175	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only. Functional operation of the device at these conditions or any conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	QFN, 48-pin package, 4-layer PCB based on JEDEC standard	27	°C/W

[3] Additional thermal information is available on the Allegro website.

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ESD CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min	Typ.	Max.	Unit
ESD HBM Robustness	$V_{ESD(HBM)}$	ESD susceptibility to GND on all pins	–2	–	2	kV
ESD CDM Robustness	$V_{ESD(CDM)}$	ESD susceptibility to GND on all pins	–500	–	500	V
	$V_{ESD(CDM,CORNER)}$	ESD susceptibility to GND on corner pins	–750	–	750	V

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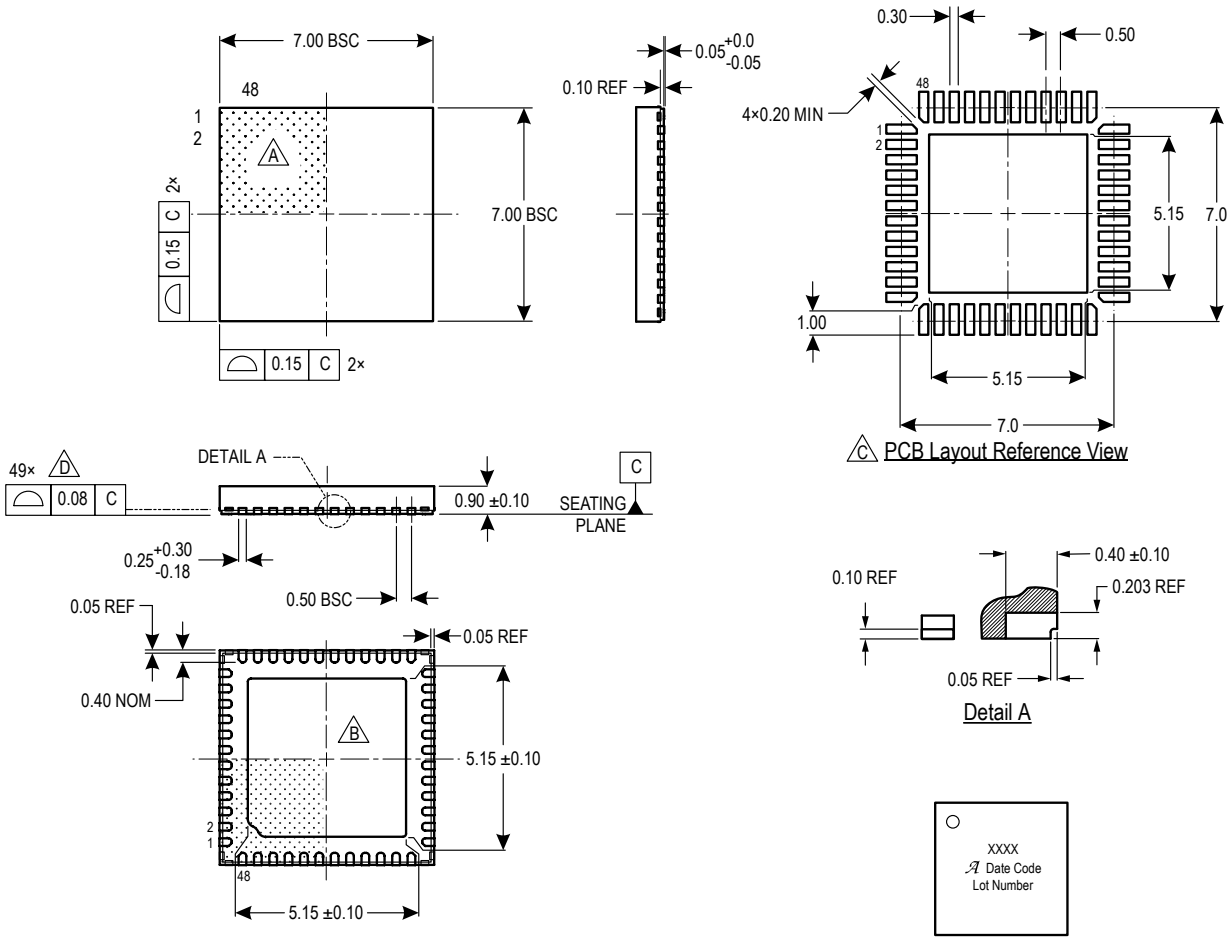
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

E Standard Branding Reference View
Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 25: Package EV, 48-Pin QFN with exposed pad and wettable flank

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Revision History

Number	Date	Description
–	March 2, 2026	Initial release
1	March 24, 2026	Initial release to Allegro website

For the latest version of this document, visit our website:
www.allegromicro.com

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